Patch-Panel ASIC

24 March 2004 SOS

1. Overview

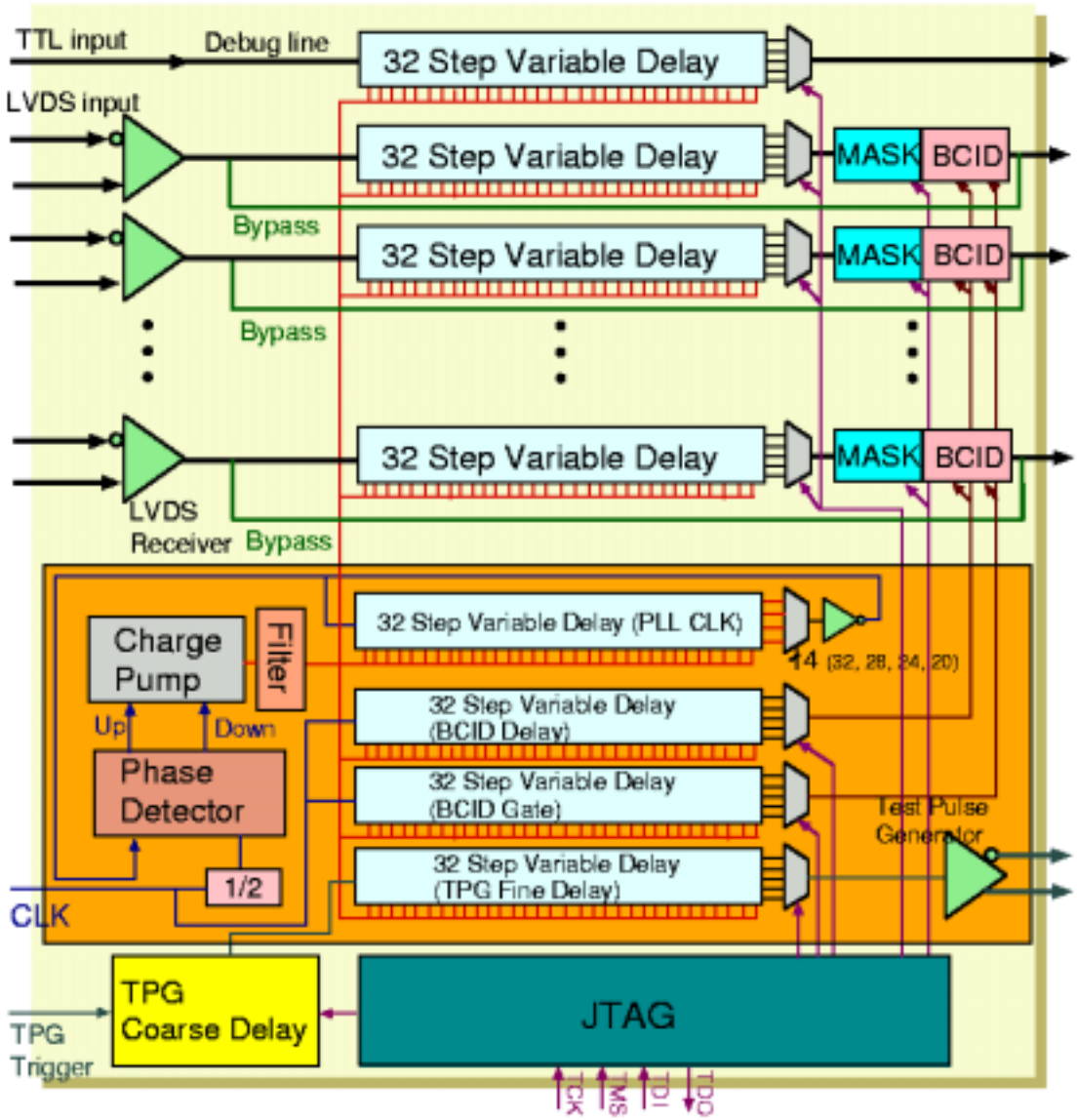


Figure 1 Block diagram of the Patch-Panel ASIC.

The Patch-Panel ASIC is a full custom CMOS IC to be implemented on a PS-Board of the PS-Pack. The IC, Figure 1, receives discriminator output signals from two 16-ch TGC ASD Boards by LVDS receivers and performs bunch-crossing identification (BCID). The signals from the ASD Board are transmitted with the LVDS level via twisted-pair cables. Prior to the BCID, variable delays are introduced to all signals from ASD Boards in order to adjust the delay difference from TOF and cable length, and to adjust the phase difference between LHC 40 MHz clock and signals from an ASD Board. The BCID circuit contains two variable delays that are used to adjust for the phase difference between the clock and hit signals from and to provide effectively

wider gate width than 25 ns to the BCID circuit. The BCID circuit also can mask individual channels. The IC can generate two channels of the test pulses, which are initiated by the Test Pulse Trigger signal from a TTC receiver and are provided to two ASD Boards. The amplitude and its delay from the Trigger signal are programmable for each ASD Board. The adjustable delay can change from 0 to 25 ns range with sub-nanosecond resolution. Additional coarse delays are also introduced to the Test Pulse generators.

The IC is sub-divided to two parts; Port-A and Port-B. Each port corresponds to a single 16-ch ASD Board. Setting of the delay is common to group of signals that come from the same ASD Board. The JTAG protocol is adopted to the control of the IC.

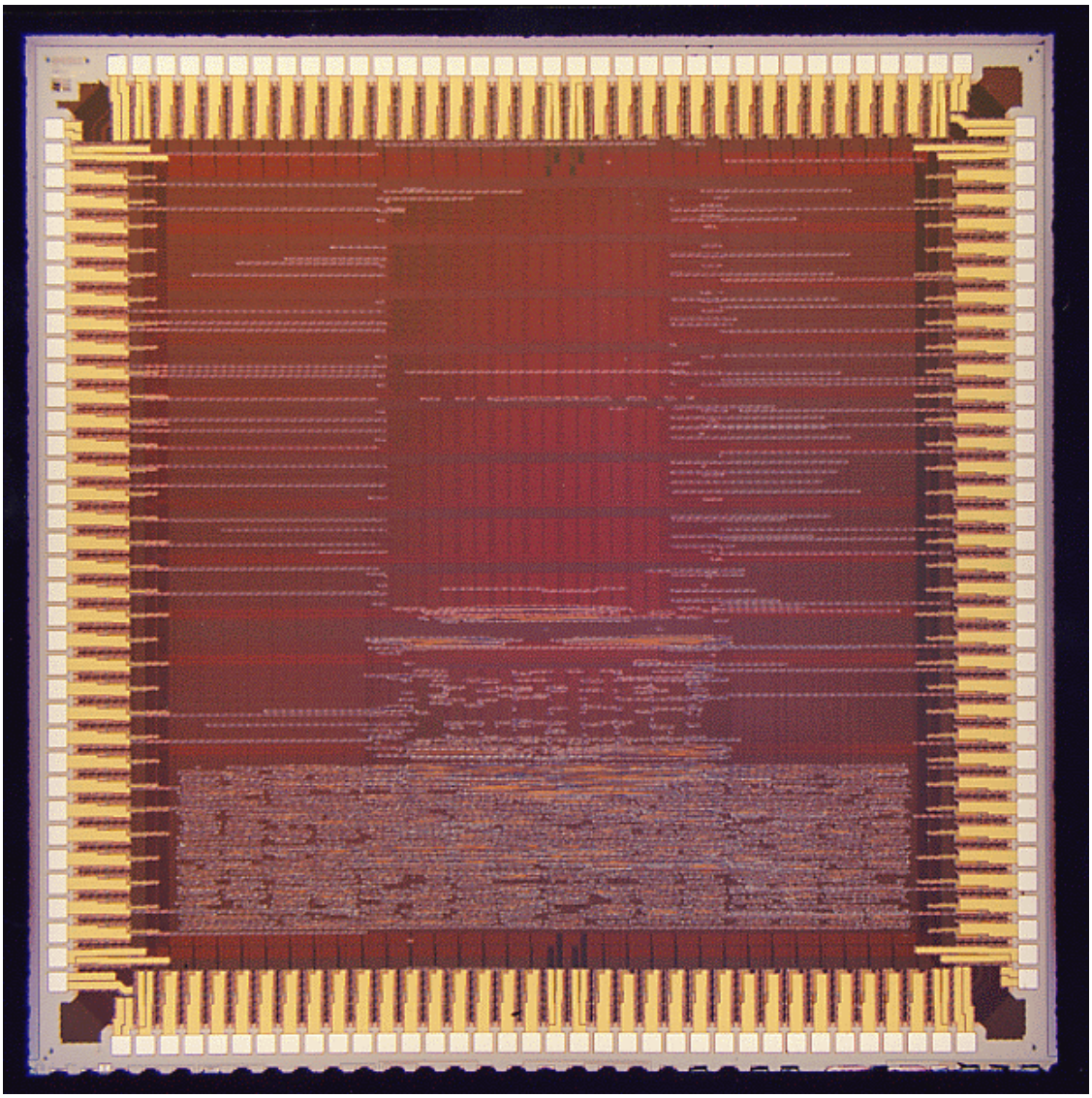


Figure 2 Photograph of Patch-Panel ASIC. The size is 5mm x 5mm.

2. Process

We have developed the Patch-Panel ASIC using 0.35 μm full custom CMOS technology of Rohm Co. with support of VLDAC (Venture LSI Design Assist Center, Rohm) and VDEC (VLSI Design and Education Center, University of Tokyo). The IC is fabricated on 5mm x 5mm die

as shown in Figure 2. We used the library (named "Passport Library") provided from Rohm for I/O pads and random logic circuits. We designed circuits and layouts of an LVDS receiver, a PLL, a variable delay and a pulse generator by ourselves. In the design we used only transistors with the gate length of 0.4 μm in order to make the layout less complicated.

3. LVDS Receiver

Figure 3 shows the schematics of the LVDS receiver, which consists of a differential amplifier and two stages of inverter circuits. We have measured performance of the receiver. Figure 4 shows propagation delays changing amplitude and offset voltage of the input differential signals. The offset voltage is defined to be the center voltage of "low" and "high" levels of input differential signals. The amplitude and the offset voltage of the differential signals from the ASD Board are 400 mV and 1.2 V, respectively. The dependence on the supply voltage shows in Figure 5. The propagation delays shown in figures are sums of the delays of the receiver and the output buffer. We can anticipate that the variation of the propagation delay due to the change of the operation conditions is less than 1 nsec. The data shows that the receiver is not fully compatible with the LVDS receiver specification (IEEE 1596.3).

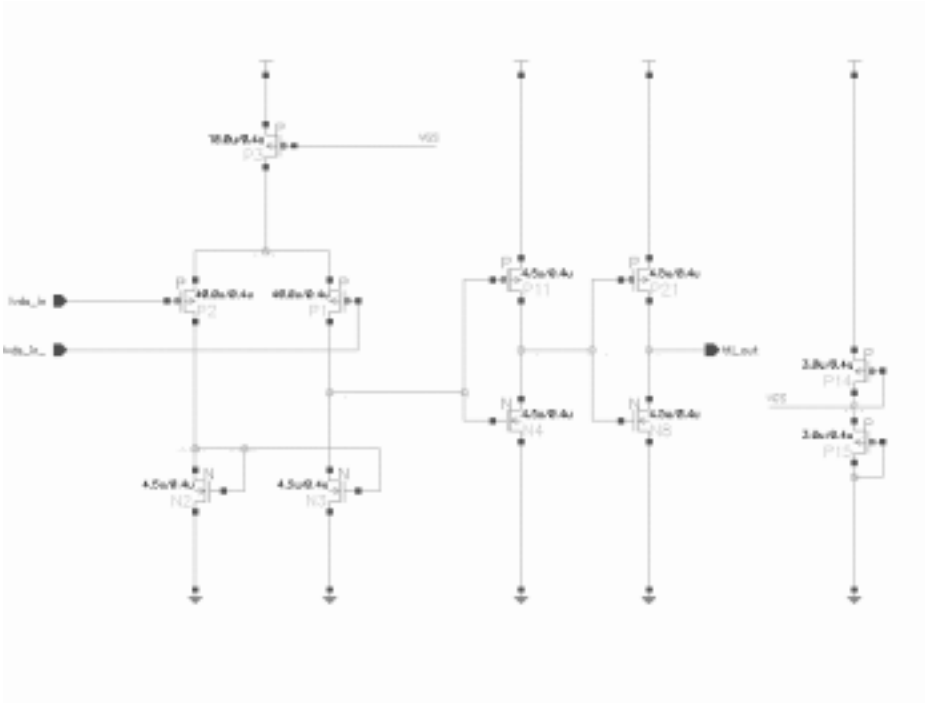


Figure 3 Circuit schematic of the LVDS receiver.

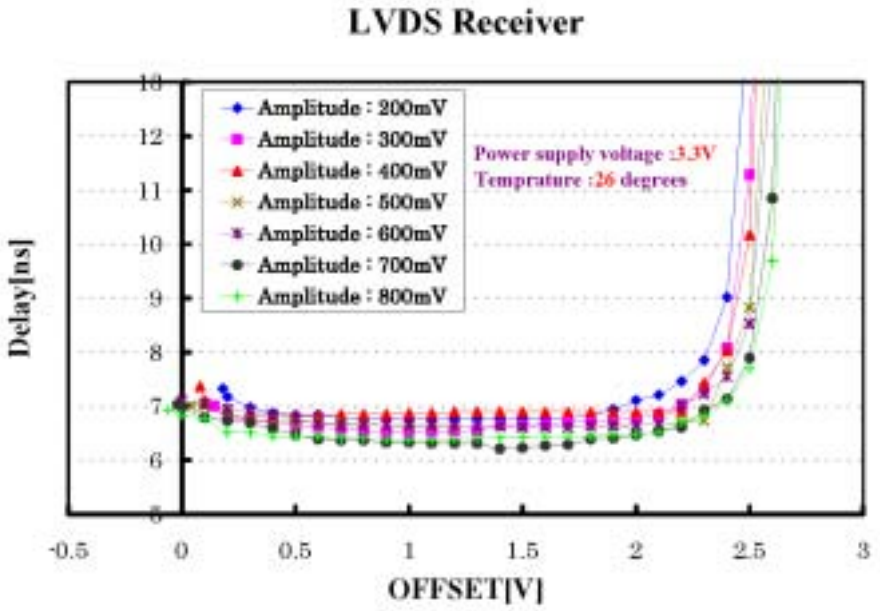


Figure 4 Propagation delays changing offset voltage and input amplitude.

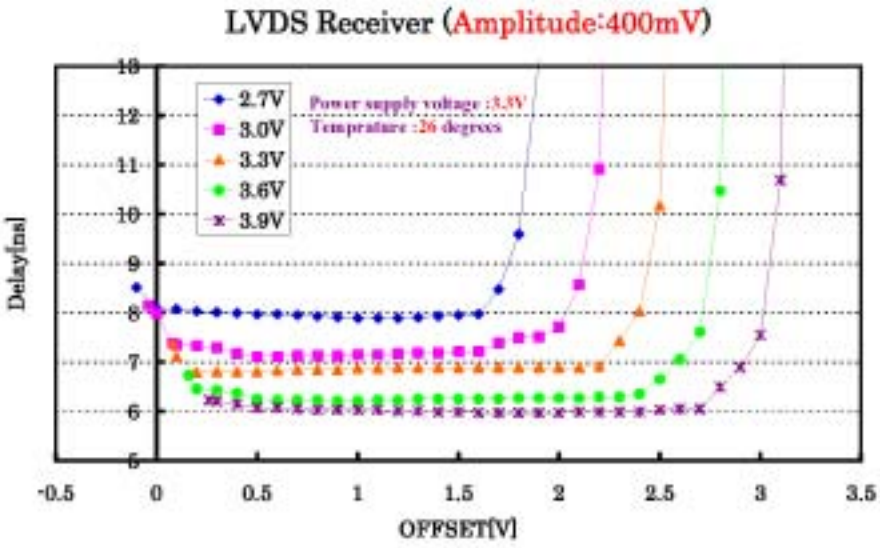


Figure 5 Propagation delays vs. supply voltage.

4. Variable Delay

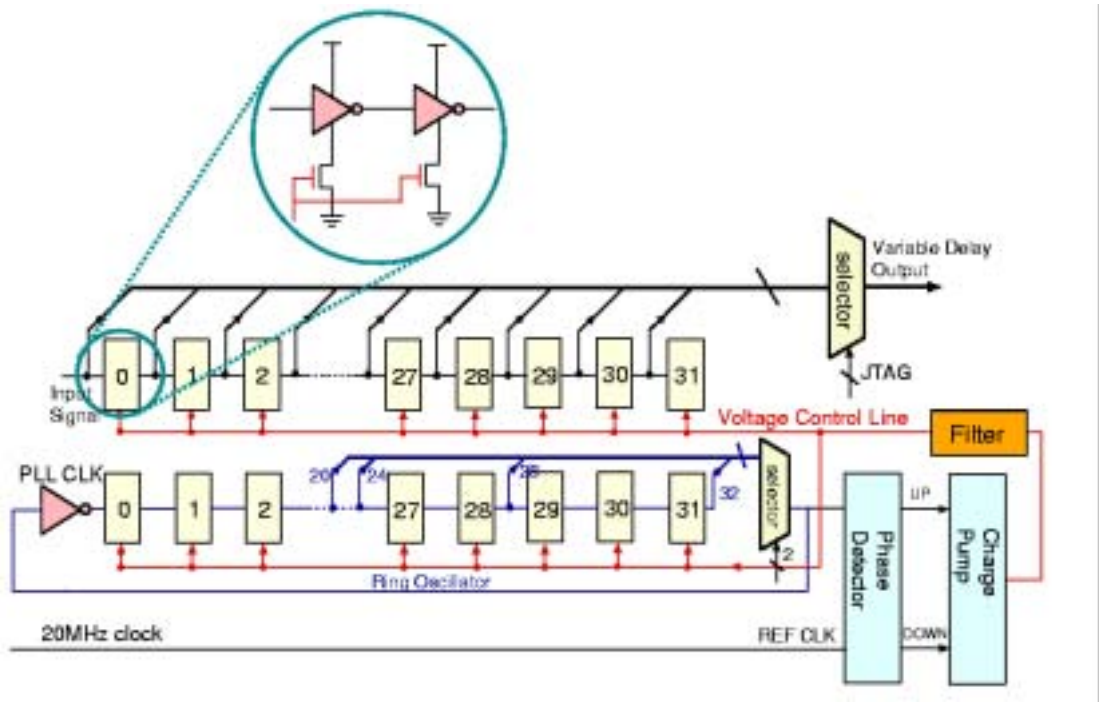


Figure 6 Block diagram of PLL and Variable Delay

In order to implement variable delay circuits with the precision of sub-nano second, we employed a PLL technique in order to stabilize the delay against changes of IC operation conditions as shown in Figure 6.

The PLL circuit consists of Voltage Controlled Ring Oscillator (VCRO), Phase Detector, Charge Pump and Low Pass Filter circuits. The VCRO is formed with 32 stages of delay units and an inverter gate. A selector is incorporated in the VCRO in order to change the number of the delay units (20, 24, 28 or 32) in the ring. The selector can adapt fluctuation of the IC production process and also can change the dynamic range of the variable delay. Each delay unit contains two inverter gates, the propagation delay of which is controlled by the Voltage Control (**VCON**) line in Figure 6. Since a signal passes around the ring is inverted, the ring works as an oscillator. When a signal takes 25 nsec to pass around on the ring, the frequency of the VCRO is 20 MHz. The Phase Detector compares the output from the VCRO with a reference clock. When the phase of the VCRO clock is going forward (backward) against the reference clock, the Charge Pump decreases (increases) the voltage of **VCON**. This loop works as negative feedback and stabilizes the frequency of the VCRO. In the other word, the negative feedback circuit will keep the signal propagation delay around the ring at 25 nsec, which is a half of a period of the reference clock.

The schematics of the delay unit, the Phase Detector, the Charge Pump and the Low-Pass Filter are shown in Figure 7, where the capacitor of the Low-Pass Filter is not implemented on the chip. In the operation we used a 100 pF capacitor outside the chip. We employ exactly same circuits of 32 stages of the delay units with the same layout in the PLL circuit as a Variable Delay, where the voltage to the delay units is fed from the PLL circuit. As far as the PLL circuit is being at the locked state and all the delay units behave equally, the propagation delay of the Variable Delay will be kept constant against any changes of the operation conditions (e.g. supply voltage, temperature). One can set the signal delay of the Variable Delay in accordance with 5-bit data written via JTAG as shown in Figure 6.

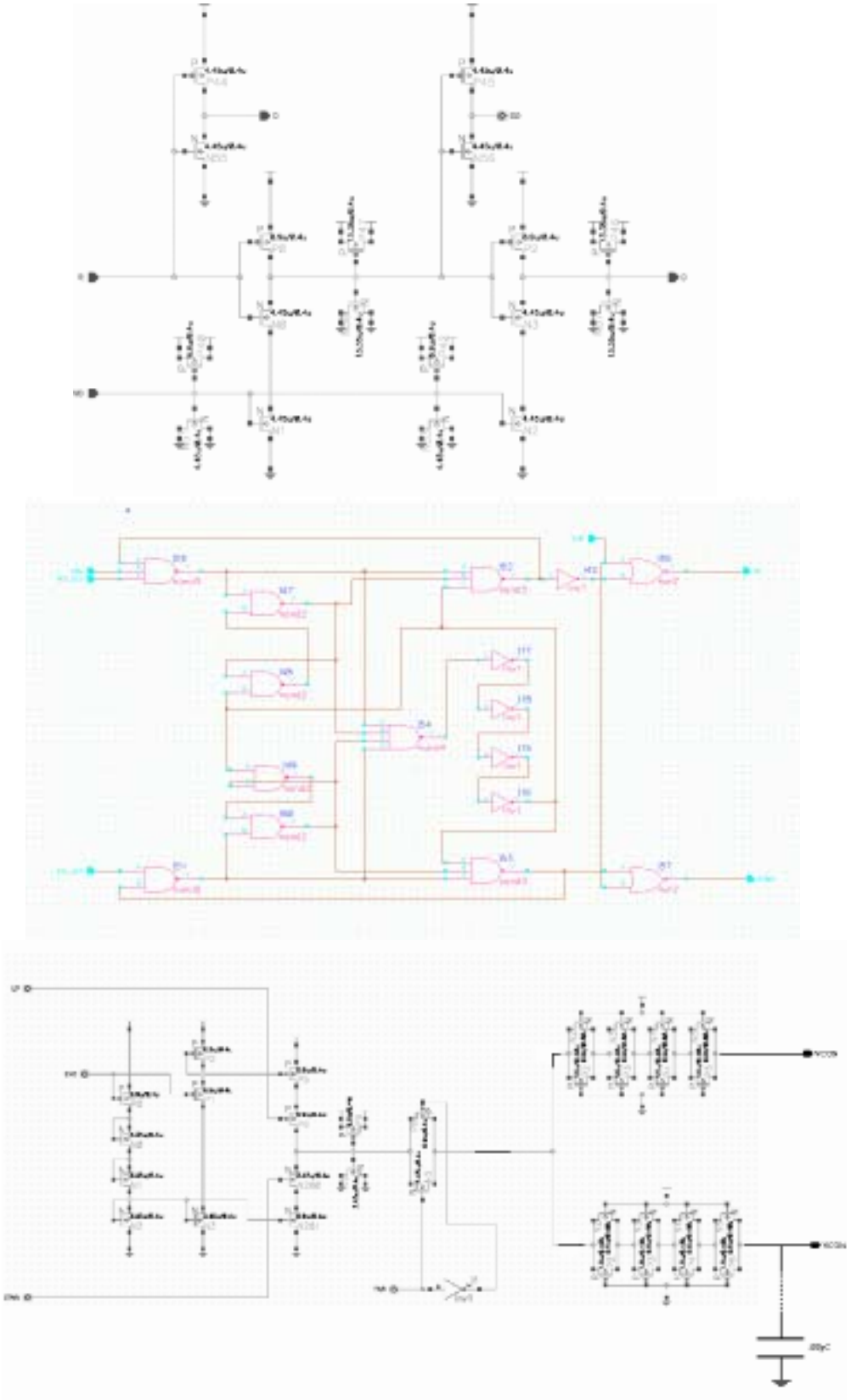


Figure 7 Schematics of delay unit, phase detector, charge pump and low pass filter.

One channel of a bare Variable Delay with an input buffer and an output buffer is implemented on the chip for debug purpose. We measured the propagation delays of the signals that pass through the 32 stages of the delay units as a function of **VCON** in Figure 8. The figure shows that the propagation delay can be changed from 12 nsec to longer than 60 nsec. Figure 9 shows the measurements of the variable delay changing the 5-bit data setting. By changing the number of the delay units in the VCRO of the PLL ("PLL Step" in figures), we can change the dynamic range (the resolution) of the Variable Delay. The resolutions of the Variable Delay are 0.74 nsec (PLL STEP32), 0.84 nsec (PLL STEP28), 0.98 nsec (PLL STEP24) and 1.2 nsec (PLL STEP20). The dynamic ranges are [the resolution] x 31 (5-bit). The measurement shows that the Variable Delay can set longer than 25 nsec delay with the resolution of sub-nano second. Figure 10 shows chip variations of the delay. Figure 11a to 11d are measurements of the delay changing the supply voltage to the IC. The data show the dependence of the delay on the supply voltage is very small. The dependence on ambient temperature is also measured in Figure 12.

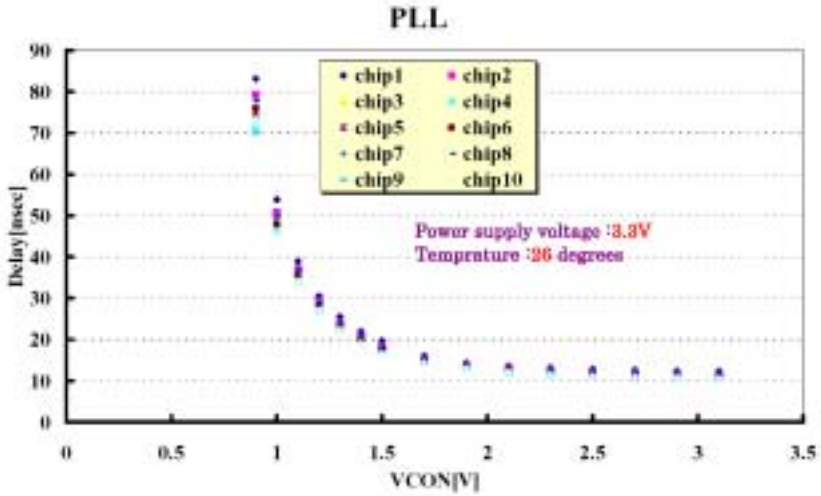


Figure 8 Propagation delay through 32 stages of delay units as a function of VCON. 10 chips were measured.

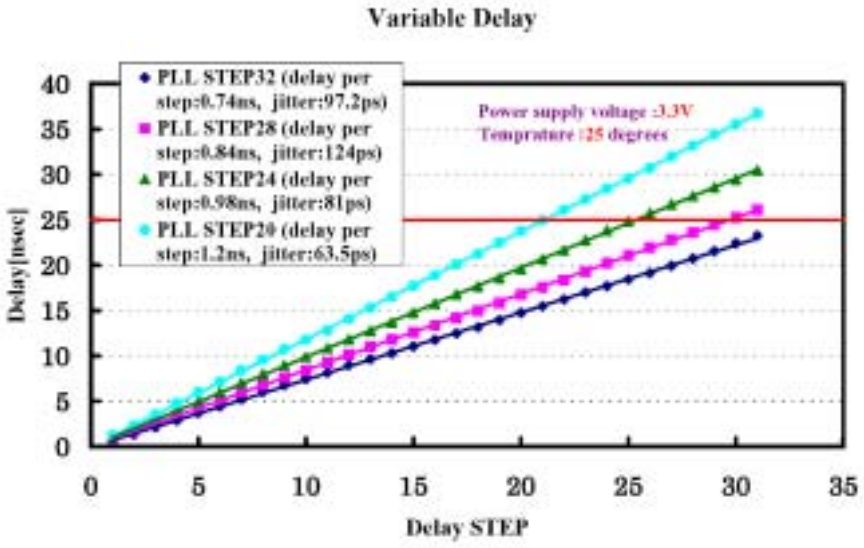


Figure 9 Measurement of the Variable Delay.

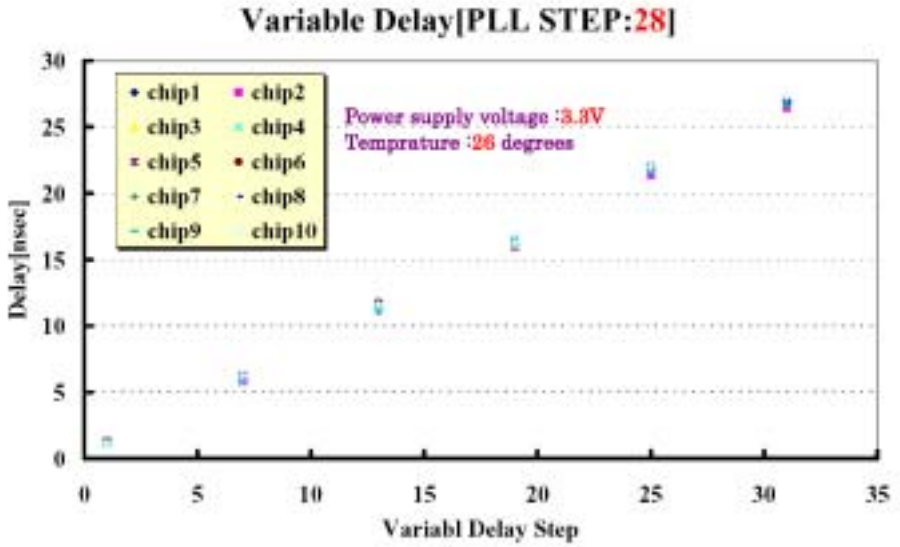
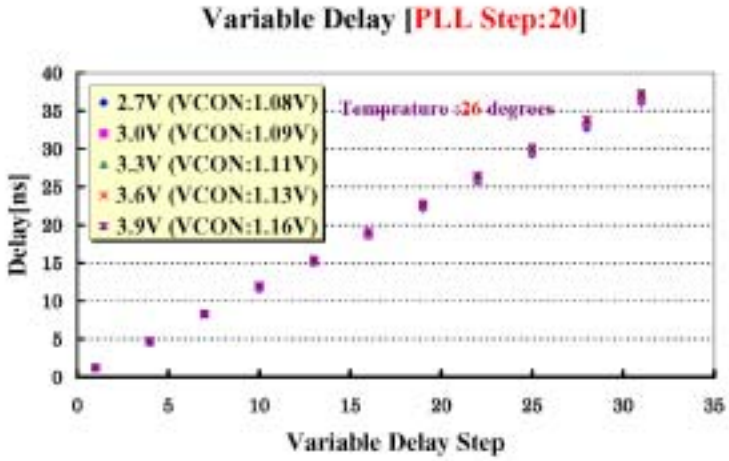


Figure 10 Chip variation of the Variable Delays



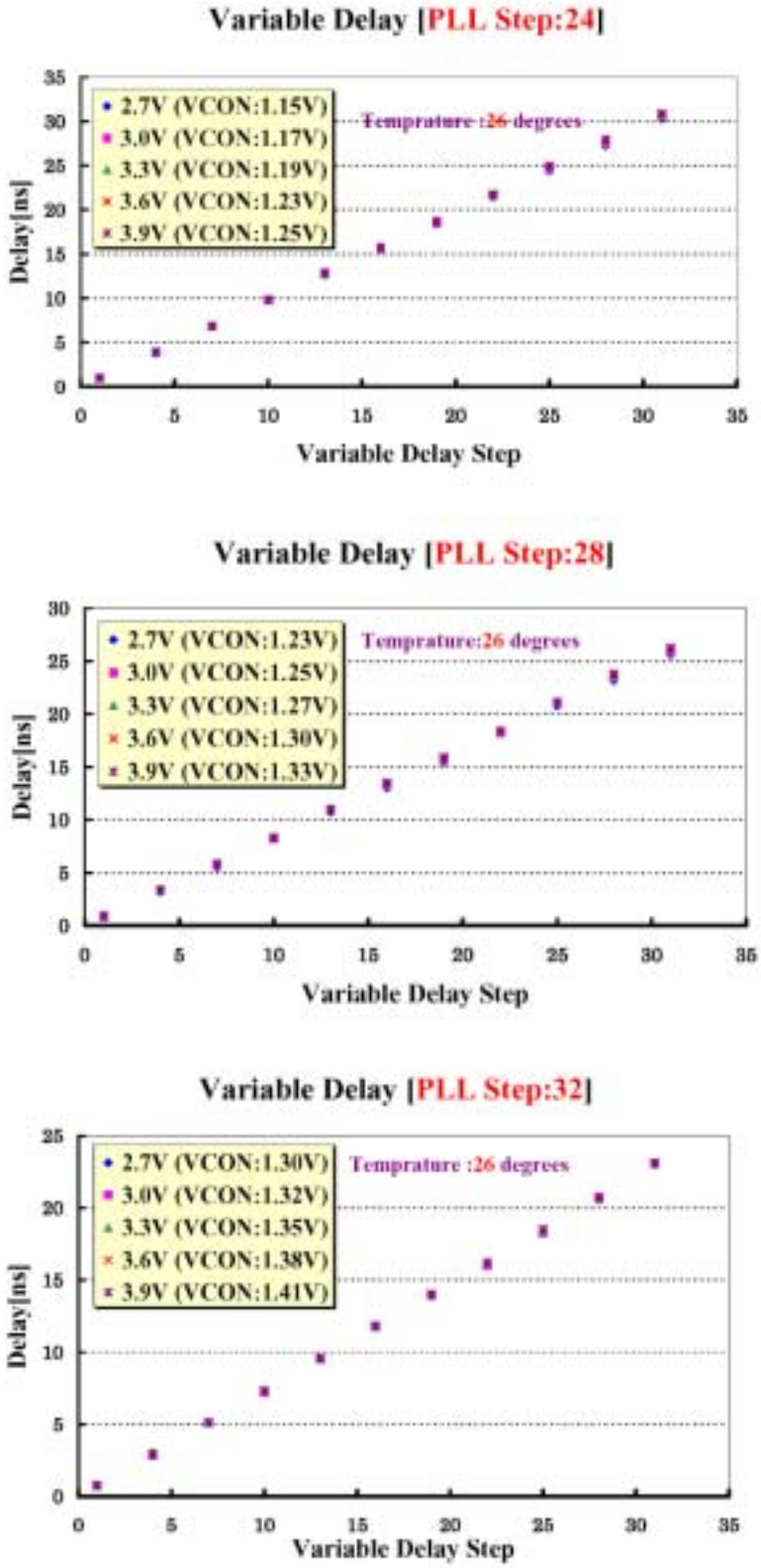


Figure 11 Measurements of the delays changing supply voltage and the number of delay units in PLL (PLL Step:20,24,28,32).

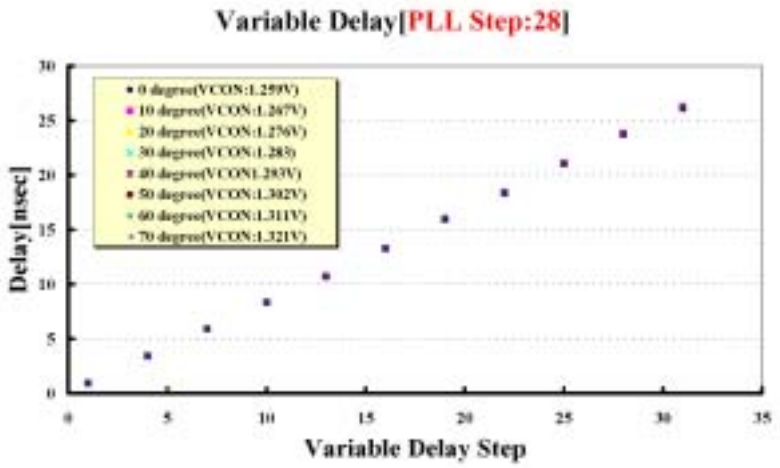


Figure 12 Temperature dependence of the Variable Delay.

5. BCID

Figure 13 shows the conceptual design of the BCID circuit. It contains two Variable Delays, described above. The first delay is used to adjust for the phase difference between the 40 MHz clock on the PS-Board and the earliest arrival times of signals from the ASD Board. The second delay is used to adjust the effective gate width to be longer than 25 nsec. Set values for each delay are common to a group of 16-ch signals from an ASD Board. The BCID circuit has an input ENABLE / Mask function, which can be set via JTAG. Figure 14a to 14d show the result of the check, where the input pulse timings are plotted at the corresponding clock numbers of the output of a channel, for a clock frequency of 40 MHz and effective gate width of 26 nsec to 48 nsec. We could set the effective gate width from 26 nsec to 48 nsec (not 25 nsec to 50 nsec).

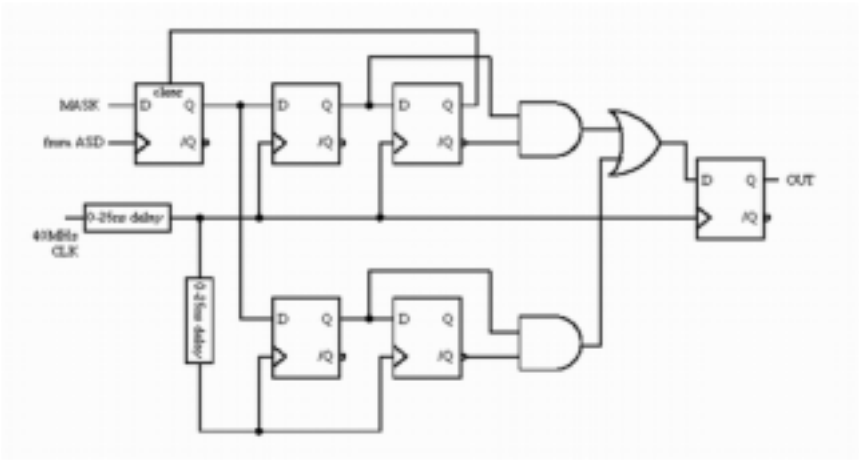
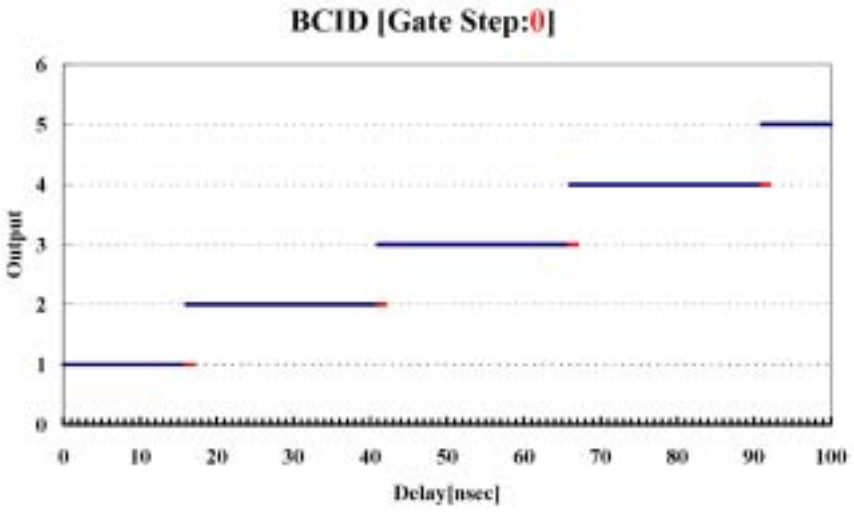
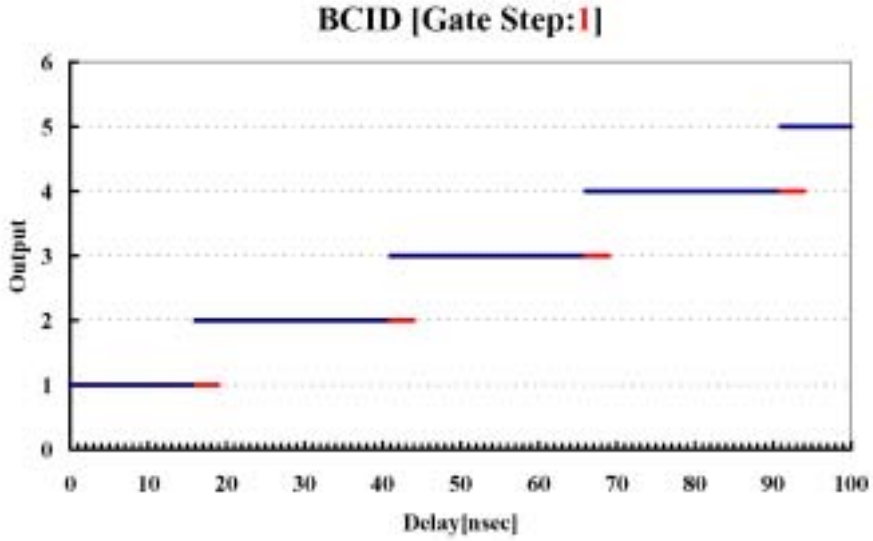


Figure 13 BCID circuit schematic


BCID [Gate Step:0]
Output
Delay[nsec]
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
80
90
100


BCID [Gate Step:1]
Output
Delay[nsec]
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
80
90
100

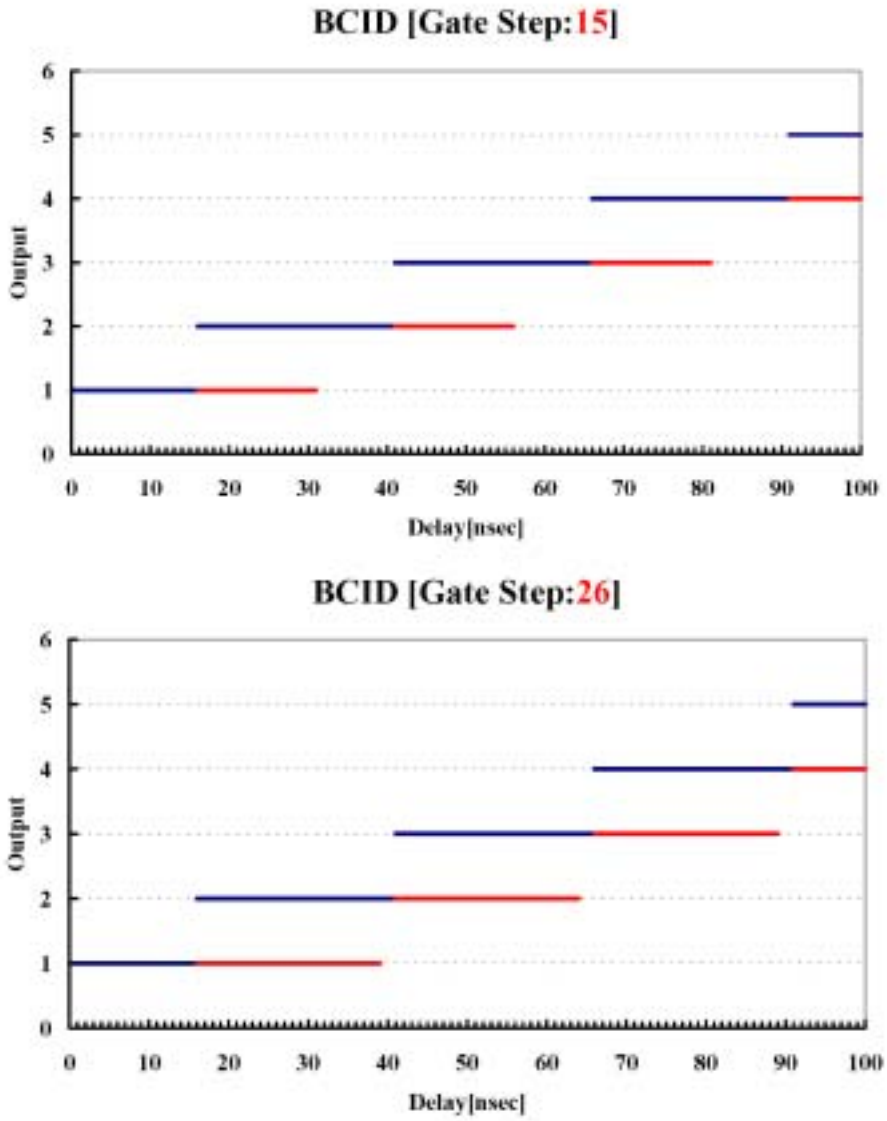


Figure 14 Scatter plots of the input pulse timing to the BCID circuit versus the corresponding clock number of the output.

6. Test Pulse Generator

When the IC receives a Test Pulse Trigger signal, the Test Pulse Generator outputs a differential square pulse with 3 μsec width. The amplitude can be set by 4-bit data (0 to 15) written via JTAG. The signal of **POL** defines the polarity of the test pulse. The Test Pulse Trigger signal from outside of the IC can is taken with either a rising edge or a falling edge (programmable) of the 40 MHz clock in the IC. The delay of the test pulse after receiving a Test Pulse Trigger can be programmed by setting a coarse delay (0 to 8 clocks) and a fine delay (0 to 25 nsec). Figure 15 shows the schematics of the pulse generator part. The amplitude versus setting data shows in Figure 16, where the data were measured with a 25 ohm load for each output. The Test Pulse Generator drives a twisted-pair cable, pair-wires of which are terminated to ground with 51 ohm resistors at both ends. Figure 17 and 18 show dependence of the amplitude on the ambient temperature and supply voltage. The data indicate that the amplitude largely depends on supply voltage. The delay changing the fine delay (Variable Delay) is shown in Figure 19.

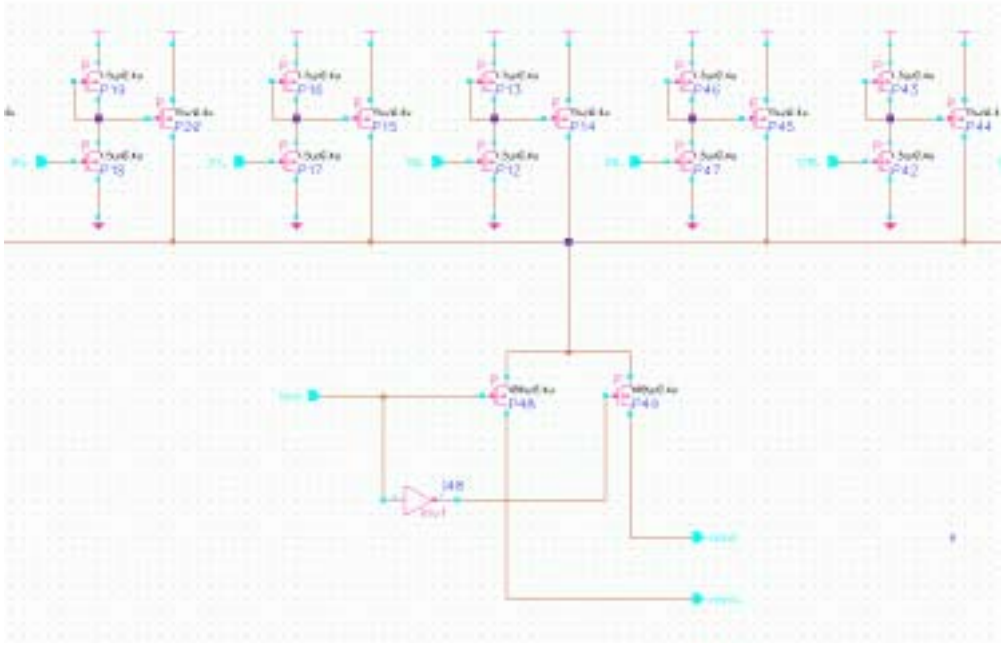


Figure 15 Schematic of the Pulse Generator. In the figure only 5 current sources are drawn, but 15 current sources are implemented in the real circuit.

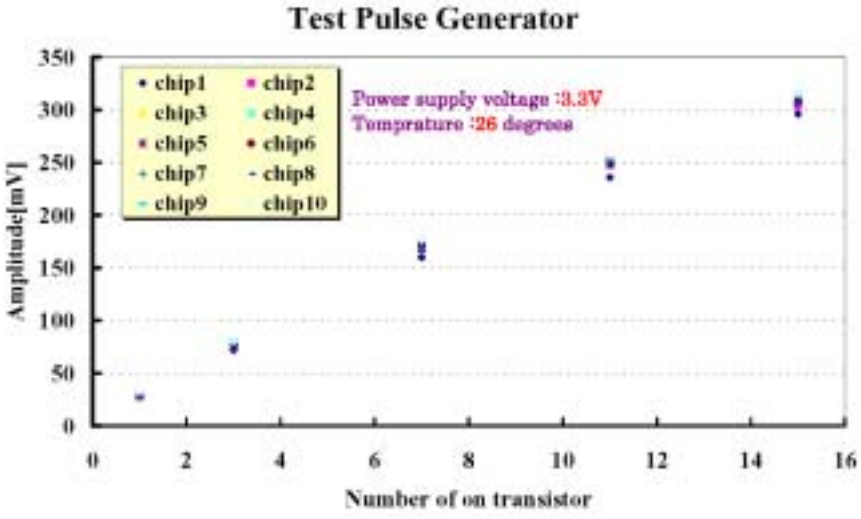


Figure 16 Amplitude of the differential output with 25 ohm loads for each output pins.

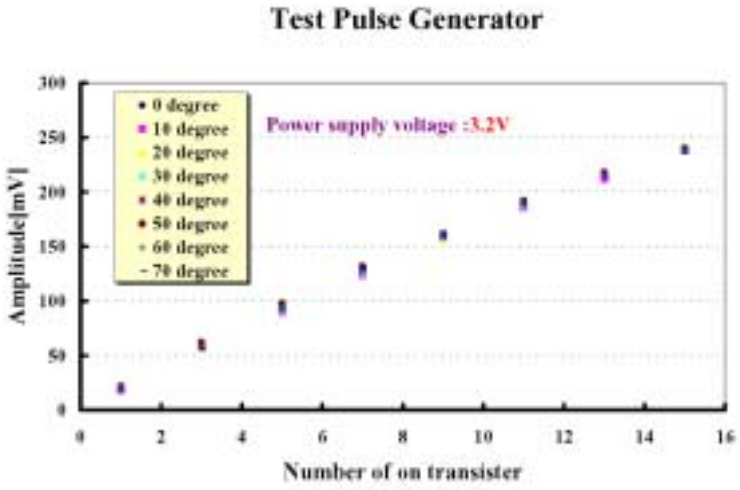


Figure 17 Amplitudes changing ambient temperature

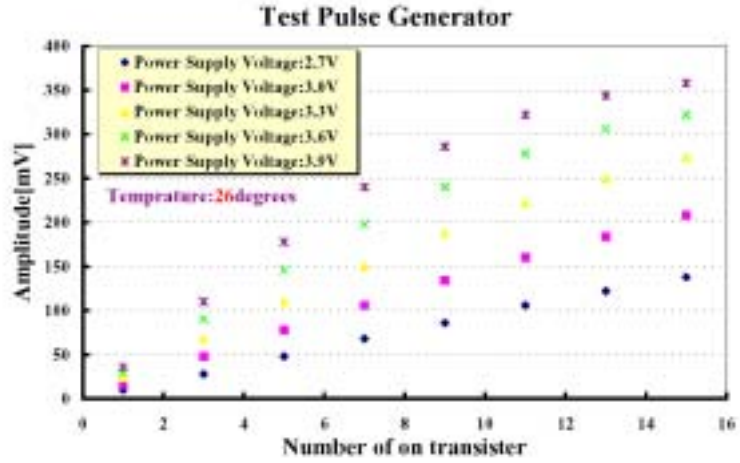


Figure 18 Amplitudes changing supply voltage

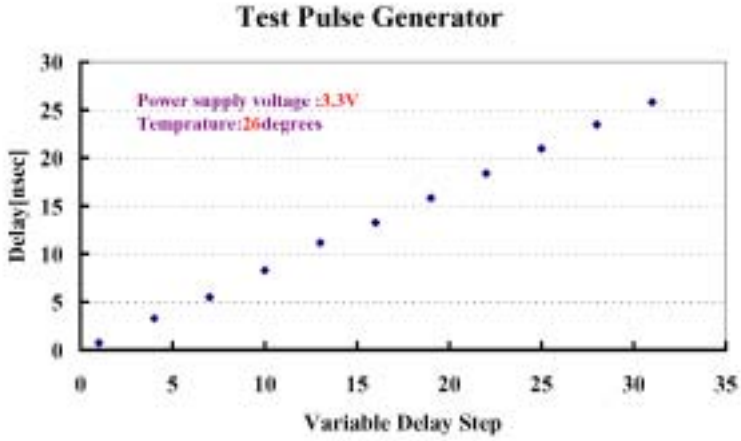


Figure 19 Fine Delay of the Test Pulse Generator

7. Signal I/O Definition

Signals and pin-assignment are summarized in Table 1 and Figure 20.

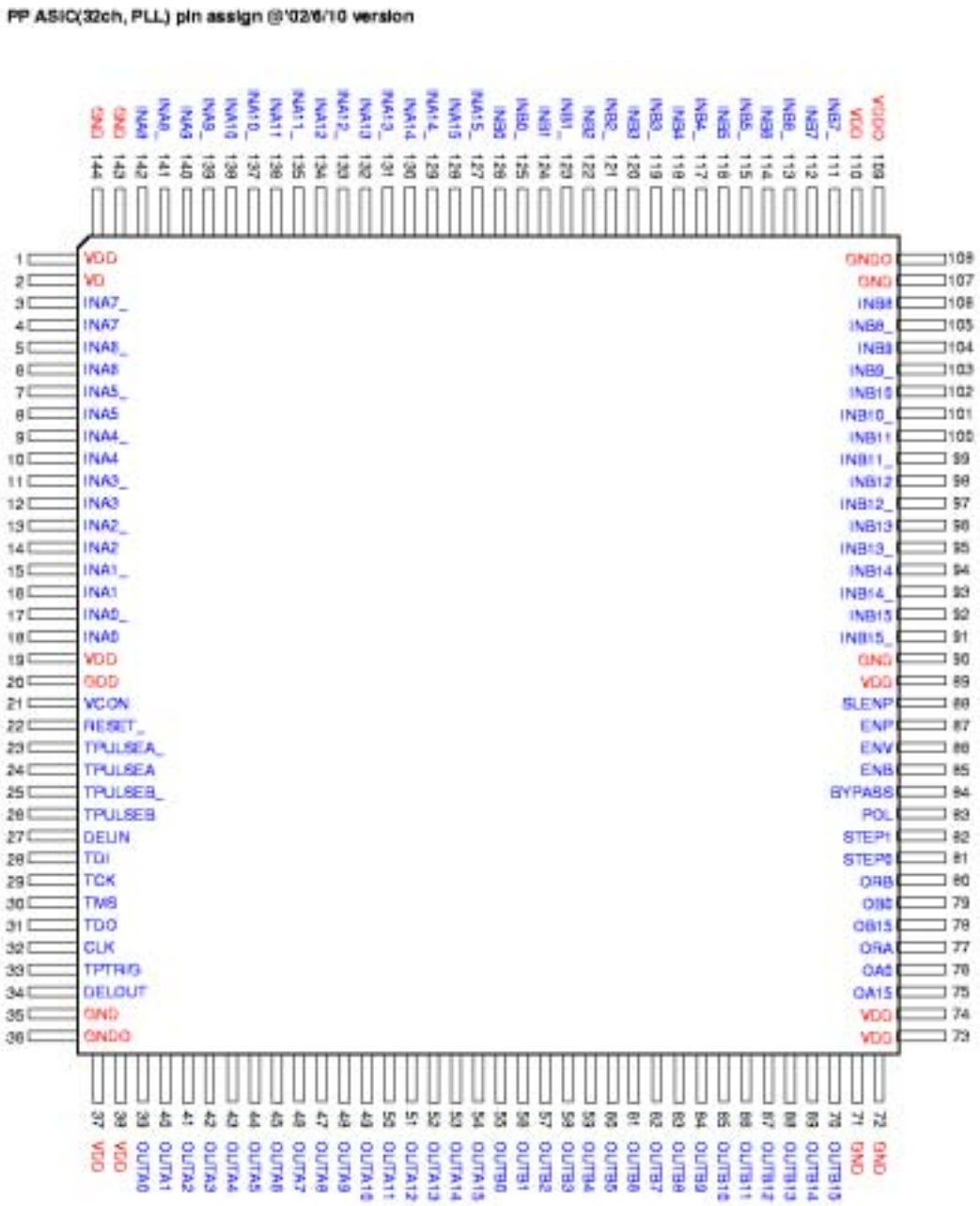


Figure 20 Pin-assignment of the Patch-Panel ASIC

Table 1 Signal I/O Definition of Patch-Panel ASIC

Name	Pin	Type	Signal
Port-A			
INA0 INA 0_ INA1 INA1_ INA2 INA2_ INA3 INA3_ INA4 INA4_ INA5 INA5_ INA6 INA6_ INA7 INA7_ INA8 INA8_ INA9 INA9_ INA10 INA10_ INA11 INA11_ INA12 INA12_ INA13 INA13_ INA14 INA14_ INA15 INA15_	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 142 141 140 139 138 137 136 135 134 133 132 131 130 129 128 127	LVDS IN	Raw LVDS Signals from an ASD Board: 16-channel raw LVDS signals from an ASD Board are received by LVDS receivers and are converted to CMOS level. Further signal processing is decided by POL and BYPASS signals. Signal from anode: INA receives a positive logic signal (hit=H). INA_ receives a negative logic signal (hit=L). Signal from cathode: INA receives a negative logic signal (hit=L). INA_ received a positive logic signal (hit=H). POL = L Raw signals from anode wires. Output signals from LVDS receivers are not inverted. POL = H Raw signals from strips Output signals from LVDS receivers are inverted. BYPASS = L Signals are fad to variable delay circuits and then bunch-identification circuits. BYPASS = H Signals are fad to outputs as OUTA signals directly. Neither variable delay circuit nor bunch-identification circuit.
OUTA0 OUTA1 OUTA2 OUTA3 OUTA4 OUTA5 OUTA6 OUTA7 OUTA8 OUTA9 OUTA10 OUTA11 OUTA12 OUTA13 OUTA14	39 40 41 42 43 44 45 46 47 48 49 50 51 52 53	CMOS OUT	Hit Signals: 16-bit hit signals are output. Positive logic. BYPASS=L Bunch-identified hit signals are output. BYPASS=H Asynchronous hit signals are output.

OUTA15	54		
OA0 OA15	76 75	CMOS OUT	Hit Signals from 0 and 15-channel: Hit signals of 0 and 15-channel are output. The signals are not bunch-identified. Positive logic
ORA	77	CMOS OUT	Hit OR Signal: ORed signal of hit signals from 16 channels. The signal is not bunch-identified. Positive logic.
TPULSEA TPULSEA_	24 23	Open-Drain OUT	Test Pulse Output Signal to a ASD Board: Test pulse is output to a ASD Board. The signal is differential. The amplitude and the delay from TPTRG can be set via JTAG. The pulse width is 3 usec. POL=L (anode) TPULSEA is a positive logic signal. TPULSEA_ is a negative logic signal. POL=H (cathode) TPULSEA is a negative logic signal. TPULSEA_ is a positive logic signal.
Port-B			
INB0 INB0_ INB1 INB1_ INB2 INB2_ INB3 INB3_ INB4 INB4_ INB5 INB5_ INB6 INB6_ INB7 INB7_ INB8 INB8_ INB9 INB9_ INB10 INB10_ INB11 INB11_ INB12 INB12_ INB13 INB13_ INB14 INB14_ INB15	126 125 124 123 122 121 120 119 118 117 116 115 114 113 112 111 106 105 104 103 102 101 100 99 98 97 96 95 94 93 93	LVDS IN	Raw LVDS Signals from an ASD Board: 16-channel raw LVDS signals from an ASD Board are received by LVDS receivers and are converted to CMOS level. Further signal processing is decided by POL and BYPASS signals. Signal from anode: INB receives a positive logic signal (hit=H). INB_ receives a negative logic signal (hit=L). Signal from cathode: INB receives a negative logic signal (hit=L). INB_ received a positive logic signal (hit=H). POL = L Raw signals from anode wires. Output signals from LVDS receivers are not inverted. POL = H Raw signals from strips Output signals from LVDS receivers are inverted. BYPASS = L Signals are fad to variable delay circuits and then bunch-identification circuits. BYPASS = H Signals are fad to outputs as OUTA signals directly. Neither variable delay circuit nor bunch-identification circuit.

INB15_	91		
OUTB0 OUTB1 OUTB2 OUTB3 OUTB4 OUTB5 OUTB6 OUTB7 OUTB8 OUTB9 OUTB10 OUTB11 OUTB12 OUTB13 OUTB14 OUTB15	55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70	CMOS OUT	Hit Signals: 16-bit hit signals are output. Positive logic. BYPASS=L Bunch-identified hit signals are output. BYPASS=H Asynchronous hit signals are output.
OB0 OB15	79 78	CMOS OUT	Hit Signals from 0 and 15-channel: Hit signals of 0 and 15-channel are output. The signals are not bunch-identified. Positive logic
ORB	80	CMOS OUT	Hit OR Signal: ORed signal of hit signals from 16 channels. The signal is not bunch-identified. Positive logic.
TPULSEB TPULSEB_	26 25	Open-Drain OUT	Test Pulse Output Signal to a ASD Board: Test pulse is output to a ASD Board. The signal is differential. The amplitude and the delay from TPTRG can be set via JTAG. The pulse width is 3 usec. POL=L (anode) TPULSEA is a positive logic signal. TPULSEA_ is a negative logic signal. POL=H (cathode) TPULSEA is a negative logic signal. TPULSEA_ is a positive logic signal.
CONTROL (COMMON)			
DELIN	27	CMOS IN	Input Signal to Variable Delay: The input signal is delayed in the Variable Delay circuit. The delay can be set via JTAG.
DELOUT	34	CMOS OUT	Output Signal from Variable Delay: The delayed signal from the Variable Delay circuit. The delay can be set via JTAG.
POL	83	CMOS IN	Signal Polarity: Polarity selection of raw input signals. POL = L Raw LVDS signals from a wire ASD Board. POL = H Raw LVDS signals from a strip ASD Board.
BYPASS	84	CMOS IN	Bypass of Variable Delay and BCID: Selection of bunch-identification mode or bypass mode.

			BYPASS = L Signals are fad to variable delay circuits and then bunch-identification circuits. BYPASS = H Signals are fad to outputs as OUTA signals directly. Neither variable delay circuit nor bunch-identification circuit.
CLK	32	CMOS IN	System Clock: 40 MHz system clock from TTC Rx.
TPTRIG	33	CMOS IN	Test Pulse Trigger: Test Pulse Trigger signal from TTC Rx. Positive logic. The signal is taken at a rising edge or a falling edge of CLK. It can be set via JTAG.
RESET_	22	CMOS IN	System Reset: System Reset signal from TTC Rx. Negative logic. The signal sets all registers defaults.
SLENP ENB ENV ENP	88 85 86 87	CMOS IN	PLL Enable Signals: Signals to control phase detector circuit of the PLL. SLENP=H : The initial voltage of VCON is VDD when the PLL lock sequence starts by RESET_ signal. When SLENP=H is selected, ENP signal is not effective. SLENP=L : Initial voltage of VCON is not defined. ENB=H : The charge pump is connected to VCON line. Normal state. ENB=L : The charge pump is disconnected from VCON line. VCON shall be supplied from the outside. ENV=H : Enable the phase detector. Normal state. ENV=L : Disable the phase detector. ENP=H : VCON is set at maximum voltage (VDD). ENP=L : Enable the charge pump controlled by the phase detector. Normal state.
STEP0 STEP1	81 82	CMOS IN	PLL Depth: Setting of the number of delay units in ring oscillator of the PLL STEP=0: 32 STEP=1: 28 STEP=2: 24 STEP=3: 20
VCON	21		Control Voltage: DC voltage to control delay units. A capacitor (a few 100 pF) for the low pass filter shall be connected to the pin.
TDI	28	CMOS IN	Test Data Input: Test Data Input signal of JTAG.
TMS	30	CMOS IN	Test Mode Select: Test Mode Select signal of JTAG.
TCK	29	CMOS IN	Test Clock: Test Clock signal of JTAG.
TDO	31	CMOS OUT	Test Data Output: Test Data Output signal Of JTAG.
GND	20		Ground: 0 volts.

	35 36 71 72 90 107 108 143 144		
VDD	1 2 19 37 38 73 74 89 109 110		Power: 3.3 volts.

8. Power Consumption

The power consumption was measured as a function of the input rate of hit signals from the ASD Board as shown in Figure 21. It is shown that the IC consumes approximately 130 mW (4 mW/ch) under the expected nominal condition of Atlas.

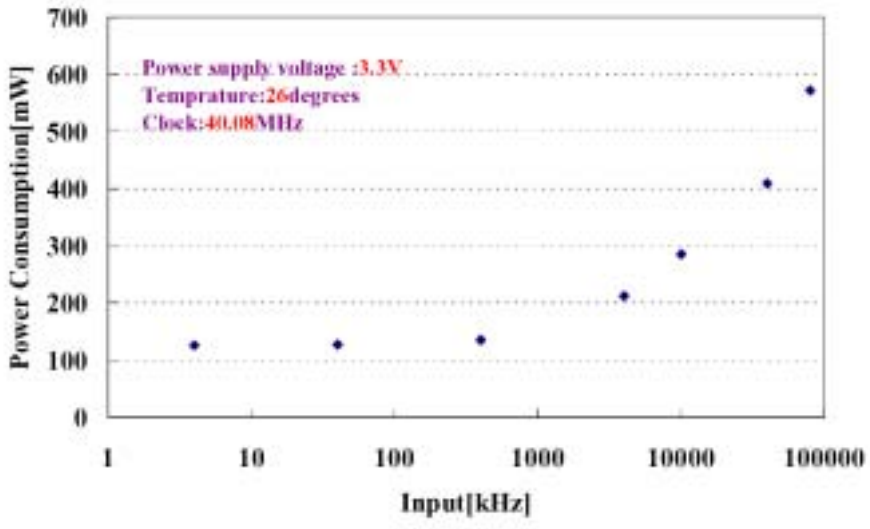


Figure 21 Power consumption as a function of input rate of hit signals.

9. Control

Most of the control will be done by JTAG protocol, where the chip does not support **TRST_** signal. The instruction length of the IC is 8 bits, and the data is fed in from LSB to MSB. The instruction is shown in Table 2. The boundary scan is not supported. When the chip receives a command other than listed on the table, the IC interprets the command as BYPASS. Since the Patch-Panel ASIC can take care of two 16-ch ASD Boards (A-part and B-part), one can separately set parameters for each part independently. The voting logic is introduced to instruction registers and the data registers in order to cope with the radiation immunity against SEU that would be induced by charged particle irradiation.

Table 2 Patch-Panel ASIC JTAG Instructions

Register Name	Instruction Code MSB LSB	Comments
INSTRUCTION		[7:0] Instruction register (R/W)
BYPASS	****_****	[0] Bypass register (R/W) Instruction codes that do not defined in this table are interpreted as BYPASS.
BCID_MASKA	0000_010x	[15:0] BCID Mask register (Port-A) (R/W) "0" signal masks an input signal and "1" signal un-masks an input signal. LSB corresponds to INA0 and MSB corresponds to INA15. Default is all "1".
BCID_MASKB	0000_011x	[15:0] BCID Mask register (Port-B) (R/W) "0" signal masks an input signal and "1" signal un-masks an input signal. LSB corresponds to INB0 and MSB corresponds to INB15. Default is all "1".
TPG_AMPA	0000_101x	[3:0] Test Pulse Amplitude register (Port-A) (R/W) Data=0 sets no signal output. Data=15 sets a test pulse signal maximum. Default is data=15.
TPG_AMPB	0000_110x	[3:0] Test Pulse Amplitude register (Port-B) (R/W) Data=0 sets no signal output. Data=15 sets a test pulse signal maximum. Default is data=15.
TPG_FINEA	0001_000x	[4:0] Fine-Delay register for Test Pulse (Port-A) (R/W) Data=0 sets no fine delay. Data=31 sets the delay maximum. Sub-nano second step and longer than 25 nsec dynamic range. Default is data=31.
TPG_FINEB	0001_001x	[4:0] Fine-Delay register for Test Pulse (Port-B) (R/W) Data=0 sets no fine delay.

		Data=31 sets the delay maximum. Sub-nano second step and longer than 25 nsec dynamic range. Default is data=31.
TPG_COARSEA	0001_011x	[4:0] Test Pulse Coarse-Delay register (Port-A) (R/W) MSB[4] defines the timing when the Test Pulse Trigger signal is taken. Data[4]=0: The Test Pulse Trigger signal is taken at a falling edge of the clock. Data[4]=1: The Test Pulse Trigger signal is taken at a rising edge of the clock. Data[3:0] sets the Coarse -Delay. The delay is 25 nsec step and from 0 to 200 nsec (8 clocks). Default is Data[4]=1 and Data[3:0]=15.
TPG_COARSEB	0001_100x	[4:0] Test Pulse Coarse-Delay register (Port-B) (R/W) MSB[4] defines the timing when the Test Pulse Trigger signal is taken. Data[4]=0: The Test Pulse Trigger signal is taken at a falling edge of the clock. Data[4]=1: The Test Pulse Trigger signal is taken at a rising edge of the clock. Data[3:0] sets the Coarse-Delay. The delay is 25 nsec step and from 0 to 200 nsec (8 clocks). Default is Data[4]=1 and Data[3:0]=15.
SIGNAL_DELA	0001_110x	[4:0] Hit Signal Delay register (Port-A) (R/W) Data=0 sets no delay. Data=31 sets the delay maximum. Sub-nano second step and longer than 25 nsec dynamic range. Default is data=31.
SIGNAL_DELB	0001_111x	[4:0] Hit Signal Delay register (Port-B) (R/W) Data=0 sets no delay. Data=31 sets the delay maximum. Sub-nano second step and longer than 25 nsec dynamic range. Default is data=31.
BCID_DELA	0010_001x	[4:0] Delay register for BCID clock (Port-A) (R/W) Data=0 sets no delay. Data=31 sets the delay maximum. Sub-nano second step and longer than 25 nsec dynamic range. Default is data=31.
BCID_DELB	0010_010x	[4:0] Delay register for BCID clock (Port-B) (R/W) Data=0 sets no delay. Data=31 sets the delay maximum. Sub-nano second step and longer than 25 nsec dynamic range.

		Default is data=31.
BCID_GATEA	0010_100x	[4:0] Delay register for BCID gate width (Port-A) (R/W) Data=0 sets no delay. Data=31 sets the delay maximum. The delay is sub-nano second step and longer than 25 nsec dynamic range. The effective gate width can be set at approximately from 26 nsec to 48 nsec. Default is data=31.
BCID_GATEB	0010_101x	[4:0] Delay register for BCID gate width (Port-B) (R/W) Data=0 sets no delay. Data=31 sets the delay maximum. The delay is sub-nano second step and longer than 25 nsec dynamic range. The effective gate width can be set at approximately from 26 nsec to 48 nsec. Default is data=31.
DEBUG_DEL	0010_111x	[4:0] Delay register for debug signal (R/W) Data=0 sets no delay. Data=31 sets the delay maximum. Sub-nano second step and longer than 25 nsec dynamic range. Default is data=31.
SEU	0011_0000	[0] Monitoring SEU flag (Read only) Data=1 means SEU of the registers is observed. By re-writing the register, the flag is reset.

Instruction Code x=1: write mode, x=0: read mode

10. Radiation Tolerance (TID)

The Patch-Panel ASICs must have adequate radiation tolerance to use in ATLAS environment. Actual Radiation Tolerance Criteria (RTC) is calculated from Simulated Radiation Level (SRL) with following equations.

RTC = SRL•SFsim•SFldr•SFlot

Here,

SFsim: Represents safety factor for SRL inaccuracies.
SFldr: Represents safety factor for low dose rate effects.
SFlot: Represents safety factor for the variation of radiation tolerance from lot to lot and within a lot.

SFlot for the pre-selection of COTS will be '2' if the final chips are produced in homogeneous batches. If the batches of the chip are unknown, SFlot must be '4'. Since the number of the chips at the mass-production is approximately 15k chips, we can request homogeneous batch to the fabrication companies. So we can use SFlot=2.

Gamma Irradiation tests using a ^{60}Co source were done on 26 Nov. 2002 at Research Center for Nuclear Science and Technology (RCNST) in University of Tokyo. We could not follow the test method shown in the reference because of lack of the samples and lack of the annealing and aging time. Therefore we have to use SFldr = '5'.

Simulated Radiation Levels for total ionizing dose (SRLtid) for the Patch-Panel ASIC are 0.3 Gray/year at the worst locations at 10^{34} luminosity, and SFsim is '3.5' for the muon system. Thus the maximum values of the RTCtid for 10 years operation are;

(RTCtid)max = 0.3 (Gray) x 3.5 x 5 x 2 x 10 (years) = 105 Gray = 10.5 krad.

Although the (RTCtid)max is 10.5 krad、we irradiated the chips more than 30 krad(Si) for the safety margin.

We irradiated three chips up to 30 krad and one chip up to 85 krad. The rate of the irradiation was 0.954 krad/min. We measured DC supply current feeding 40 MHz clock during irradiation. We also measured functions of the chips before and after the irradiation. Figure 22 shows the supply current vs. dose. The increase of the current can be observed at more than 30 krad. Any function defect was not observed in the chips after the irradiation.

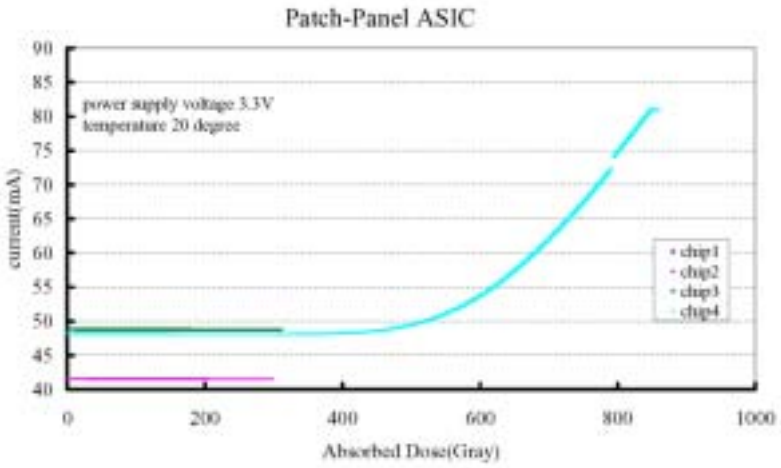


Figure 22 Measurement of the supply current during the irradiation

11. Radiation Tolerance (SEE)

12. Mass-production and Inspection

The number of the Patch-Panel ASICs to be used in the TGC System is 10,368 except for spares. We mass-produced 25,000 un-tested chips in 2003. We are developing the dedicated inspection station, which consists of hardware and its control software. We measure the DC parameters of the chips and check JTAG control functions. The system generates test pulses and feeds to input ports of the chip. The BCID hit signals are read and checked by the system. Since the failure rate of the chips after the above tests is expected to be very low, the comprehensive test will be done as a PS-Board after the assembling.

13. Package

The package of the IC is LQFP144. Figure 23 shows mechanical dimensions.

LQFP, 144
FPT-144P-M08

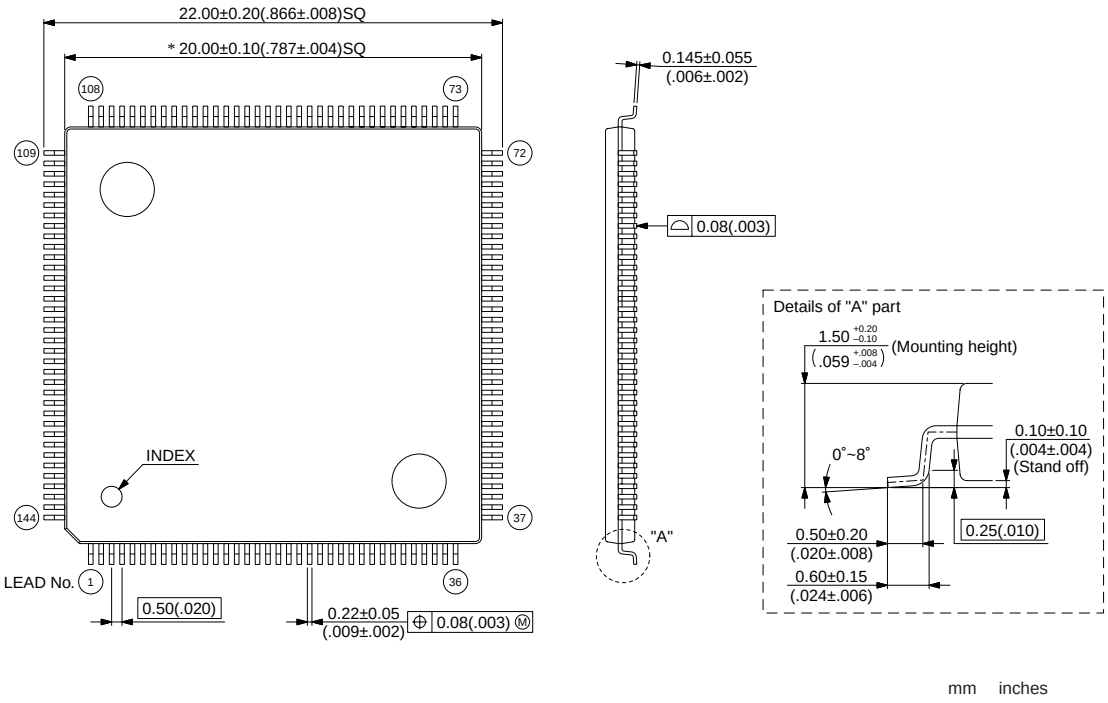


Figure 23 Mechanical Dimensions of Patch-Panel ASIC (LQFP144). The unit is mm (inch).