AMT-TEG Manual

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1. Introduction

AMT-TEG is a low-power and high-resolution multi-hit Time-to-Digital Converter LSI produced with Toshiba's 0.3 μm CMOS Sea-of-Gate Technology (TC220G).

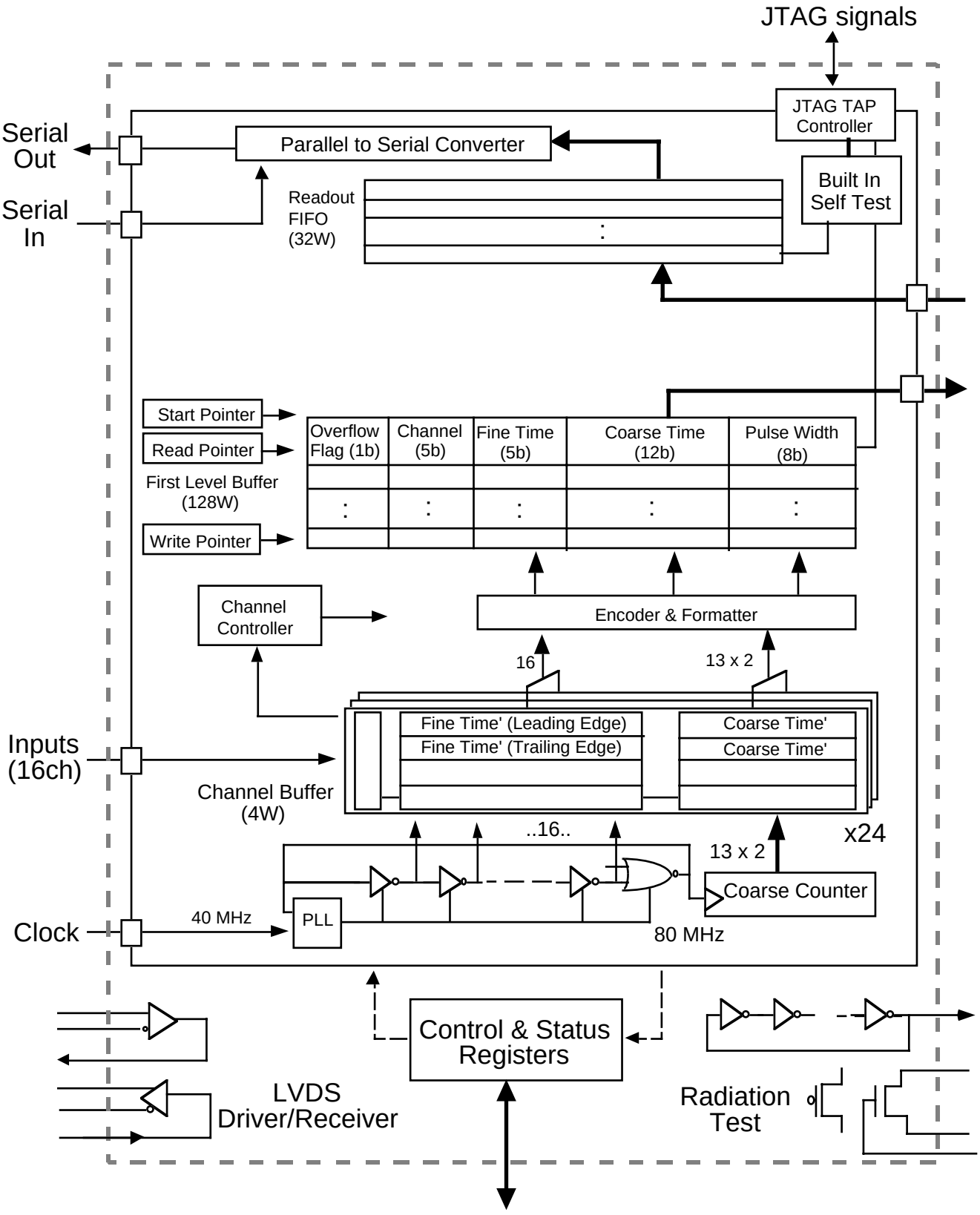


Fig. 1-1 Block diagram of the AMT-TEG

2.Circuit Description

Fig. 1-1 shows a block diagram of the AMT-TEG chip. There are 24 channels and 16 inputs of which are selectably connected to input pins.

Table. 1 summarizes the main features of the AMT-TEG chip.

Table. 1 AMT-TEG MAIN FEATURES (@40MHz System Clock)
(TDC related parameters only.)

• Least Time Count	0.78 ns/bit (rising edge) 0.78-100ns/bit (falling edge)
• Time Resolution	RMS = 250 ps (rising edge) RMS = 250ps - 29ns (falling edgez)
• Integral Non Linearity	< 80 ps
• Differential Non Linearity	< 60 ps
• Stability	< 0.1 LSB (3.0 - 3.6 V. 0 - 70 ˚C)
• Input Clock Frequency	80 MHz(x1), 40 MHz(x2), 20MHz(x4), 10 MHz (x8 mode)
• Internal System Clock Frequency	40 MHz
• PLL Oscillation Frequency	40 - 120 MHz
• No. of Channels	24 Channels (16 channels inputs)
• Level 1Buffer	128 words
• Double Hit Resolution	<5 ns
• L1B Readout mode	Asynchronous, auto increment address.
• Supply Voltage	3.0 ~ 3.6V
• Process	0.3 μm CMOS Sea-of-Gate (TC220G)
• Power Dissipation	~ ? mW/Channnel
• Package	0.5 mm lead pitch, 144 pin plastic QFP

2.1. Fine Time Measurement

The idea of time memory cell (AMT) was born in 1986, and it utilizes a voltage-controlled delay elements which comprise ring oscillator and memories. The ring oscillation is controlled with Phase Locked Loop (PLL) to attain high precision.

A new ring oscillator, asymmetric ring oscillator, is implemented, and the oscillation frequency of the oscilltor is 80 MHz. To obtaine <1 ns timing resolution, 16 taps are extracted from the oscillator. Fig. 2-1 shows a simplified schematics and its timing diagram of the asymmetric ring oscillator. Fig. 2-1 only shows 8 stages but the actual chip implements 16 stages. The asymmetric ring oscilator was invented to get equally spaced even number (16) of timing signals.

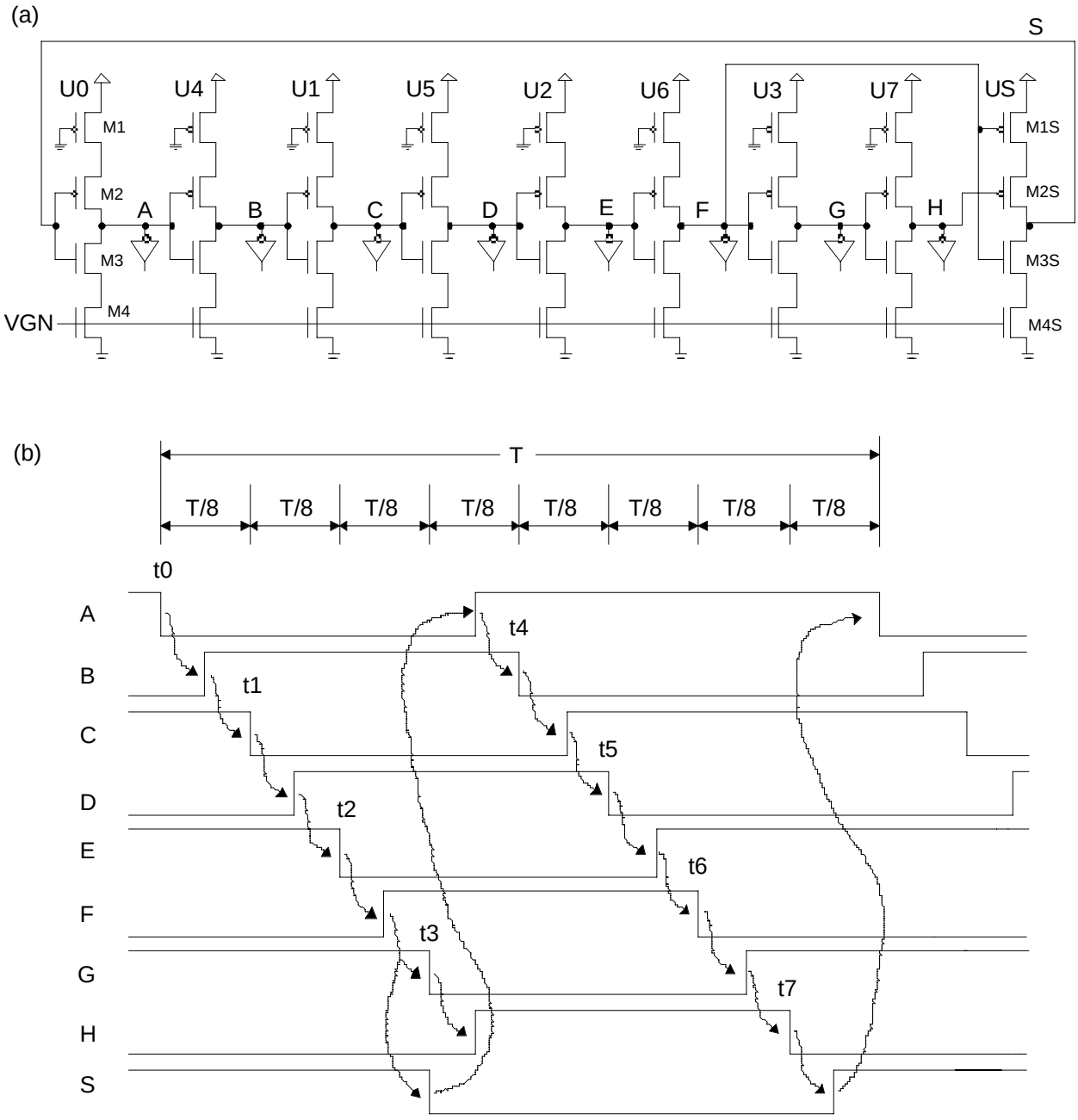


Fig. 2-1 (a) Asymmetric ring oscillator, (b) extracted timing signal.

2.2. Data Recording

2.3. PLL circuit

The PLL circuit comprises a phase frequency detector (PFD), a charge pump, a loop filter (LPF), and a voltage-controlled oscillator (VCO; asymmetric ring oscillator in this case). An external capacitor (Cvg) is required in the loop filter.The PLL has "divide by 2, 4, and 8" counter , thus the frequency of the VCO can be either the same or the “multiplied by 2, 4, or 8 ” of the input frequency.

The propagation delay of the delay elements that determine the oscillation frequency of the VCO is controlled through a control voltage (VGN).

2.4.CSR Registers

There are 8 CSR registers and the bit assignment is shown in

Table. 2 CSR registers bit assignment

bit	7	6	5	4	3	2	1	0
CSR0	enable force reject	enable trailing	enable leading	enable pair	select upper channel	width select		
CSR1	enable clk160	enable 80	l1 buffer full	serial parity error	serial state error	vernier error	coarse error	channel select error
CSR2	-	l1 buffer read address [6:0]						
CSR3	count roll over [7:0]							
CSR4	PLL clock divide 1	PLL clock divide 0	Enable Serial	Reset TDC	count roll over [11:8]			
CSR5	token delay [3:0]				serial delay [3:0]			
CSR6	serial master	keep token	strobe type 1	strobe type 0	tdc ID			
CSR7	(not used)							

(Readable/Writable : Initial value)

2.4.1. CSR0 :

• width select [read/write]

Select with resolution of the output data for the pair measurement.

width select	width output	width resolution
0	full_width[7:0]	1 bit
1	full_width[8:1]	2 bit
2	full_width[9:2]	3 bit
3	full_width[10:3]	4 bit
4	full_width[11:4]	5 bit
5	full_width[12:5]	6 bit
6	full_width[13:6]	7 bit
7	full_width[14:7]	8 bit

• select upper channel [read/write]

This chip has 24 channels circuit, but only has 16 input pins (HIT0..HIT15). Thus the upper 16 channels are multiplexed by this bit. The connections are shown below.

Select upper channel	HIT0 .. HIT7	HIT8 .. HIT15
0	Chnnel 0 ..7	Channel 8 ..15
1	Channel 0 .. 7	Channel 16 .. 23

• enable pair [read/write]

Enable pair measurement.

- enable leading [read/write]

  Enable leading edge timing measurement.

- enable trailing [read/write]

  Enable trailing edge timing measurement.

- enable force reject[read/write]

  Enable force reject. If this bit is set, dummy hit is generated after rejected hit occur.

2.4.2. CSR1 :

- channel select error [read/wite]
  Cleared by writing 0.
- coarse error [read/write]
  Cleared by writing 0.
- vernier error [read/write]
  Cleared by writing 0.
- serial state error [read/write]
  Cleared by writing 0.
- serial parity error [read/write]
  Cleared by writing 0.
- L1 buffer full [read/write]
  This bit is set when the L1 buffer becomes full. Cleared by writing 0.
- enable 80 [read/write]
  Frequency of the system clock will be half of the PLL oscillation when this bit is cleared. This system clock frequency becomes same as that of the PLL when this bit is set. For example, if the PLL is oscillating at 80 MHz, the system clock will be 40 MHz when “enable 80”=0, and 80 MHz when “enable 80”=1.
  (Present chip does not work properly at "enable 80"=1 and system clock = 40MHz. So please set to '0')
- enable clk160 [read/write]
  Enable 160 MHz clock line. 160MHz clock is used only in the serial readout circuit.

2.4.3. CSR2 :

- L1 buffer read address[read/write]: This address is automatically count up when the L1 buffer is not empty and L1BRCLK is asserted.

2.4.4. CSR3 : Count Preset Register

- Bit 7-0 of Count roll over [read/write]:

Count roll over value of the coarse time counter. This define the maximum time of the data as shown below.

Count roll over definition.

16 15 14 13	12 11 10 9 8 7 6 5	4 3 2 1 0
Bit 11 .. 8 (CSR4)	Bit 7 .. 0 (CSR3)	0

2.4.5. CSR4 :

- Bit 11-8 of Count roll over [read/write]
  See CSR3.
- Reset TDC [read/write]
  Reset TDC circuit.
- Enable Serial [read/write]
  Enable serial interface circuit.
- PLL clock divide:
  DIV (= [divide1, divide0]) : Frequency of ring oscillator is determined as show below. The period of oscillating frequency divided by 16 will be the least time count.

divide 1	divide 0	Input frequency : Ring Osc frequency
0	0	1 : 2
0	1	1 : 4
1	0	1 : 8
1	1	1 : 1

2.4.6. CSR5 : Miscellaneous control.

- serial delay [read/write]
  Set serial interface delay. This is used in daisy chain mode.
- token delay [read/write]
  Set token passing delay. This is used in daisy chain mode.

2.4.7. CSR6 : Test register.

- TDC ID [read/write]
  TDC chip ID number. This ID is appended to the data header.
- strobe_type
  Determine the serial signal strobe format. 0 = no strobe, 1 = DS strobe, 2 = leading and trailing edge strobe, 3 = leading edge strobe (clock).
- keep token [read/write]
  Don’t pass the token to next chip when this bit is set.
- serial master [read/write]

2.5. Data Format

2.5.1.Channel Buffer

[first data]

45	44	43	42 41 40 ... 32 31 30	29	28 27 26 ... 18 17 16	15 14 13 ... 3 2 1 0
rejected	edge	coarse2 parity	coarse2	coarse1 parity	coarse1	vernier

[second data]

91	90	89	88 87 86 ... 74 75 76	75	74 73 72 ... 60 61 62	61 60 59 ... 44 45 46
rejected	edge	coarse2 parity	coarse2	coarse1 parity	coarse1	vernier

if enable_pair = 0 : edge = 0 (trailing edge), edge = 1 (leading edge),

if enable_pair = 1 : edge = 0 (trailing edge found), edge = 1 (trailing edge not found)

2.5.2.Level 1 Buffer

[enable_pair = 0] (edge = 0 (trailing edge), edge = 1 (leading edge))

31	30	29 28 27 26 25	24 23 22 21 20 19 18	17	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
hit_error	reject_out	channel	0	edge	edge time

[enable_pair =1, normal data]

31	30	29 28 27 26 25	24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
hit_error	reject_out	channel	width	leading edge time

[enable_pair =1, over_flow]

31	30	29 28 27 26 25	24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
hit_error	reject_out	channel	1 1 1 1 1 1 1 1	leading edge time

[enable_pair =1, under_flow]

31	30	29 28 27 26 25	24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
hit_error	reject_out	channel	0 0 0 0 0 0 0 0	leading edge time

2.5.3.Readout FIFO (Serial Interface)

Group header

31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 0 0 1	fifo[27:0]

Group trailer

31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
1 0 1 1	fifo[27:12]	global_word_count

TDC data

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
fifo[27:24]	tdc ID	fifo[23:0]

TDC trailer

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
fifo[27:24]	tdc ID	fifo[23:12]	local_word_count

Errors

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
0 1 1 0	tdc ID	0	1 0 0 0

2.6.Data Output Sequence

3.PIN DESCRIPTION

[I = Input, DI = LVDS Differential Input, O = Normal Output, DO = LVDS Differential Output, TO = Three State Output; OD = Open drain output, AO = analog output, PU = with internal pull-up resistor, PD = with internal pull-down resistor, * = negative logic]

- CLK [I] : System clock inputs.
- RST [I] : All reset.
- CIO0~CIO7 [I,TO] : These I/O pins are data lines for control bus which read and write the CSR registers.
- CS* [I] : This signal is a strobe signal for the control bus.
- RA0~2 [I] : These pins are used as address line to the control bus.
- WR* [I] : This pin is a Read/Write* select signal in the control bus.
- VGN1 [O] : Control voltage line of the PLL circuit for the TDC. It is recommended to connect this pin to an external capacitor of 6800 pF.
- VGN2 [O] : Control voltage line of the PLL circuit for the PLLTEST. It is recommended to connect this pin to an external capacitor of 6800 pF.
- HIT0-HIT15[I]:Hit signal inputs. Hit8-15 inputs are connected to channel 8-15 or channel 16-23

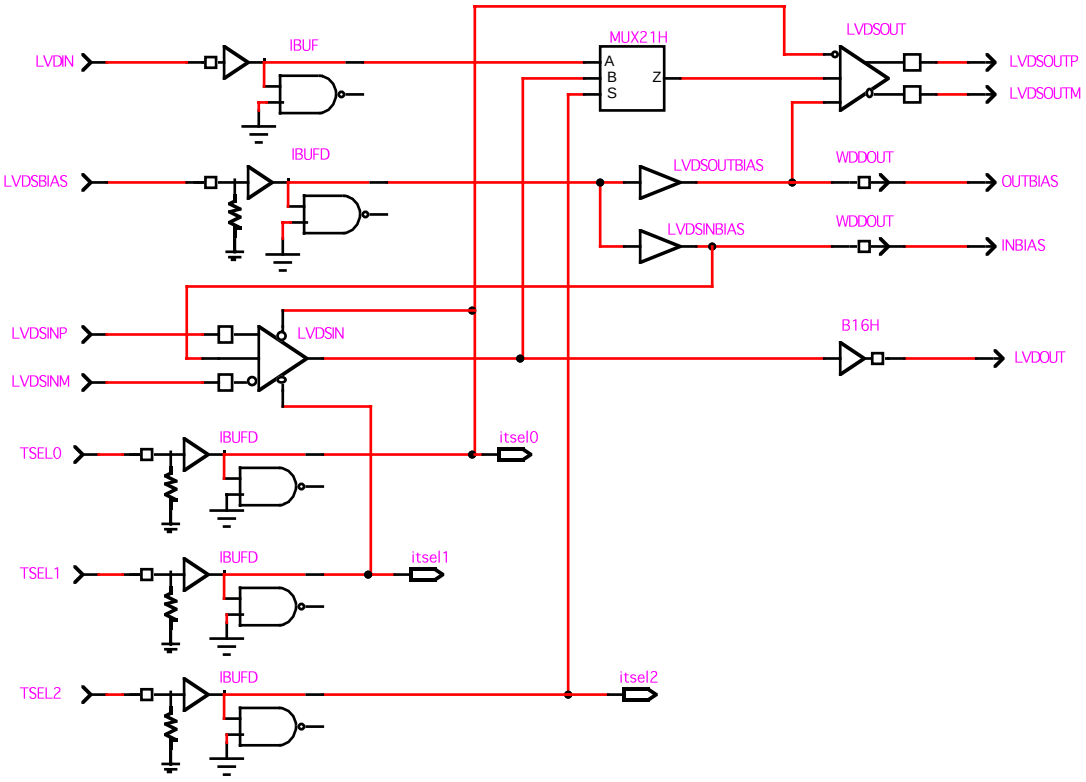
depend on the "select upper channel" bit.

- ENRO1 [I]: Enable Ring Oscillator for the TDC circuit.
- ENRO2 [I]: Enable Ring Oscillator for the PLLTEST.
- LVDSBIAS [I] : Supply bias voltage to LVDS driver and receiver when this input is high.
- LVDSOUTP [DO] : LVDS normal output.
- LVDSOUTM [DI] : LVDS complementary output.
- LVDIN [I] : input of the LVDS driver..
- LVDSINM [DI] : LVDS differential input (complementary).
- LVDSINP [DI] : LVDS differential input (normal).
- INBIAS [AO] : check pin for the LVDSINBIAS.
- OUTBIAS [AO] : check pin for the LVDSOUTBIAS.
- LVDOUT [O] : output of the LVDS receiver.
- TOUT0-TOUT3
- L1BRCLK
- L1BEMPTY
- L1BFULL
- B0-B3
- SELCLK
- TSEL0-TSEL2
- SYSCLK
- DIO0-DIO31[I,TO] : Data output and input pins.

<table>
<tr><td colspan="3"></td><td colspan="32">DIO</td></tr>
<tr><td>ENOUT</td><td>TSEL1</td><td>TSEL0</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>token_in</td><td colspan="31">- data_in[28:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td colspan="32">data_out[31:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td colspan="7">l1b_radr[6:0]</td><td>idown</td><td>iupb</td><td>0</td><td colspan="11">coarse_count[12:0]</td><td>0</td><td colspan="7">l1b_wadr[6:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td colspan="32">l1buf_out[31:0]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>word_detect</td><td>have_token</td><td colspan="20">0</td><td colspan="5">fifo_radr[4:0]</td><td>0</td><td colspan="3">fifo_wadr[4:0]</td></tr>
</table>

- TOKENOUT
- STROBE
- SERIOUT

- LOADFIFO
- SCLK
- SERIIN
- ERROR
- ENCOA
- ENRADOSC
- OSCOUT
- ENOUT
- ENCP
- RESETB
- IPD
- IPS
- IPG
- IPBG
- IND
- INS
- ING
- INBG
- TRSR
- TDO
- TMS
- TDI
- TCK
- CLK



LVDS circuit connections.

3.1. Pin Assignment

Pin No.	Signal Name	Related Block
1	VDD3	
2	VSS1	
3	HIT0	TDCCHAN
4	HIT1	TDCCHAN
5	HIT2	TDCCHAN
6	HIT3	TDCCHAN
7	HIT4	TDCCHAN
8	HIT5	TDCCHAN
9	HIT6	TDCCHAN
10	HIT7	TDCCHAN
11	HIT8	TDCCHAN
12	HIT9	TDCCHAN
13	HIT10	TDCCHAN
14	HIT11	TDCCHAN
15	HIT12	TDCCHAN
16	HIT13	TDCCHAN
17	HIT14	TDCCHAN
18	VDD	
19	HIT15	TDCCHAN
20	RA0	CSR
21	RA1	CSR
22	RA2	CSR
23	CSB	CSR
24	WRB	CSR
25	CIO0	CSR
26	CIO1	CSR
27	CIO2	CSR
28	CIO3	CSR
29	CIO4	CSR
30	CIO5	CSR
31	CIO6	CSR
32	CIO7	CSR
33	ENRO1	TDCCHAN
34	ENRO2	PLLTEST
35	VDD1	
36	N.C.	

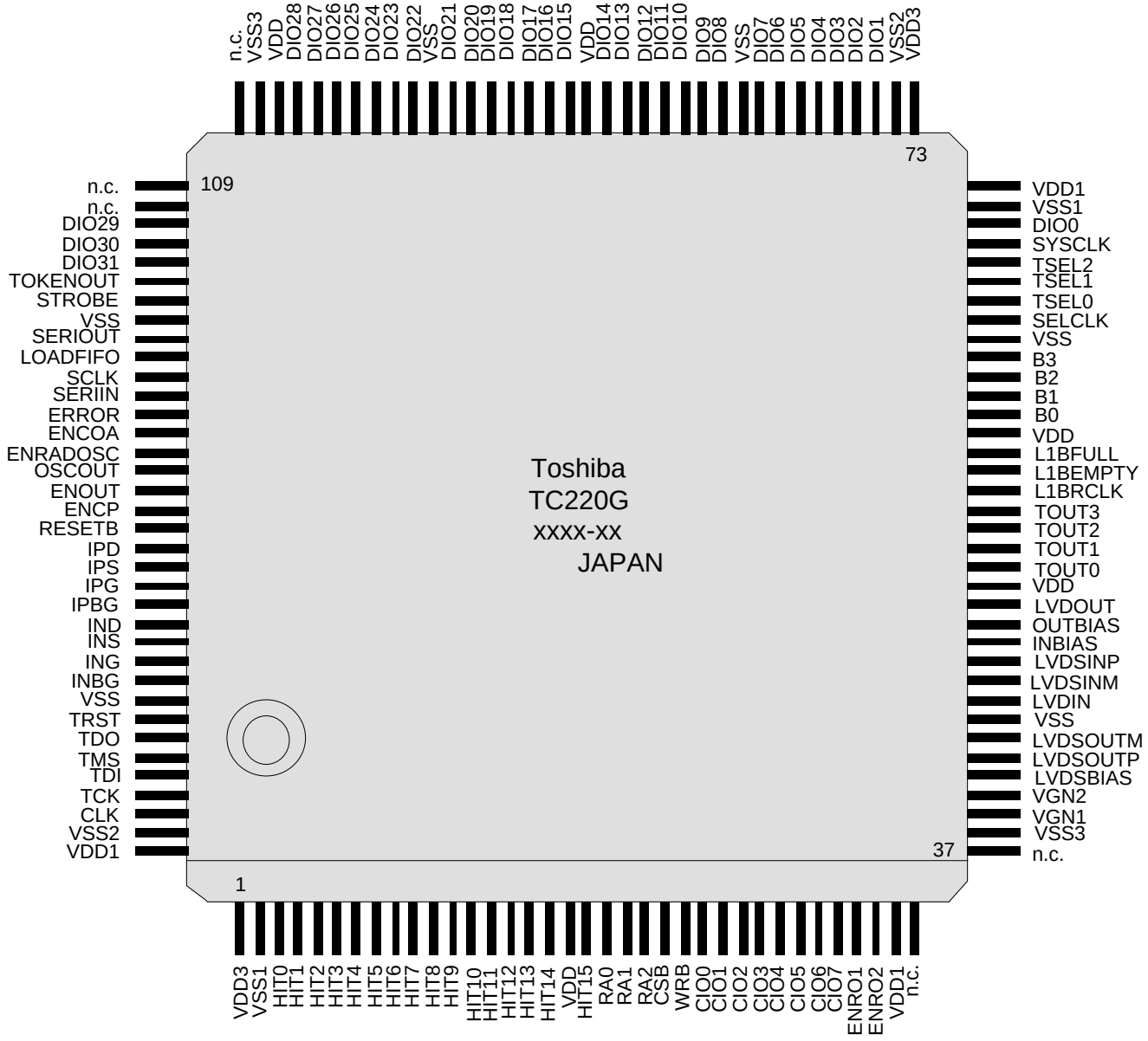
Pin No.	Signal Name	Related Block
37	N.C.	
38	VSS3	
39	VGN1	TDCCHAN
40	VGN2	PLLTEST
41	LVDSBIAS	LVDS
42	LVDSOUTP	LVDS
43	LVDSOUTM	LVDS
44	VSS	
45	LVDIN	LVDS
46	LVDSINM	LVDS
47	LVDSINP	LVDS
48	INBIAS	LVDS
49	OUTBIAS	LVDS
50	LVDOUT	LVDS
51	VDD	
52	TOUT0	TDCCHAN, READOUT
53	TOUT1	READOUT
54	TOUT2	READOUT
55	TOUT3	TDCCHAN
56	L1BRCLK	TDCCHAN
57	L1BEMPTY	TDCCHAN
58	L1BFULL	TDCCHAN
59	VDD	
60	B0	PLLTEST
61	B1	PLLTEST
62	B2	PLLTEST
63	B3	PLLTEST
64	VSS	
65	SELCLK	TDCCHAN
66	TSEL0	-
67	TSEL1	-
68	TSEL2	-
69	SYSCLK	TDCCHAN
70	DIO0	-
71	VSS1	
72	VDD1	

Pin No.	Signal Name	Related Block
73	VDD3	
74	VSS2	
75	DIO1	-
76	DIO2	-
77	DIO3	-
78	DIO4	-
79	DIO5	-
80	DIO6	-
81	DIO7	-
82	VSS	
83	DIO8	-
84	DIO9	-
85	DIO10	-
86	DIO11	-
87	DIO12	-
88	DIO13	-
89	DIO14	-
90	VDD	
91	DIO15	-
92	DIO16	-
93	DIO17	-
94	DIO18	-
95	DIO19	-
96	DIO20	-
97	DIO21	-
98	VSS	
99	DIO22	-
100	DIO23	-
101	DIO24	-
102	DIO25	-
103	DIO26	-
104	DIO27	-
105	DIO28	-
106	VDD	
107	VSS3	
108	N.C.	

Pin No.	Signal Name	Related Block
109	N.C.	
110	N.C.	
111	DIO29	-
112	DIO30	-
113	DIO31	-
114	TOKENOUT	READOUT
115	STROBE	READOUT
116	VSS	
117	SERIOUT	READOUT
118	LOADFIFO	READOUT
119	SCLK	READOUT
120	SERIIN	READOUT
121	ERROR	TDCCHAN, READOUT
122	ENCOA	TDCCHAN
123	ENRADOSC	RADOSC
124	OSCOUT	RADOSC, PLLTEST
125	ENOUT	-
126	ENCP	TDCCHAN
127	RESETB	-
128	IPD	RADOSC
129	IPS	RADOSC
130	IPG	RADOSC
131	IPBG	RADOSC
132	IND	RADOSC
133	INS	RADOSC
134	ING	RADOSC
135	INBG	RADOSC
136	VSS	
137	TRST	JTAG
138	TDO	JTAG
139	TMS	JTAG
140	TDI	JTAG
141	TCK	JTAG
142	CLK	-
143	VSS2	
144	VDD1	

(*) VDD = VDD1 = VDD3,
VSS = VSS2 = VSS3,
N.C. --- non connection

4 .Package



n.c.=non connection

98.9.1 Y.A.

AMT-TEG1 Pin Assignment (Top View)

QFP144 : 144-pin Plastic Flat Package

5.**Electrical Characteristics**

5.1.Maximum Ratings

Symbol	Parameter	Value
V_{DD}	DC Supply Voltage	-0.3 to +4.6 V
V_{IN}	Input Voltage	-0.3 to VDD+0.3 V
I_{IN}	Input Current	±10 mA
T_{STG}	Storage Temperature	-40 to +125 ˚C

5.2. Recommended Operating Condition

(V_{SS} = 0V)

Symbol	Parameter	Value
V_{DD}	DC Supply Voltage	3.3 to 3.8 V
Ta	Ambient Temperature	0 to +60 ˚C

5.3.DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input High Voltage		V_{DD} x 0.8		
V_{IL}	Input Low Voltage		V_{DD} x 0.2		
I_{IH}	Input High Current	$V_{IN} = V_{DD}$	-10	10	µA
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$	-10	10	µA
V_{OH}	High-Level Output Voltage	I_{OH} = -4 mA (B4)	2.4		V
		ERROR, L1BEMPTY, L1BFULL, TOUT0, TOUT1, CIO0-7, DIO0-31; I_{OH} = -8 mA (B8)	2.4		V
		IOH = -16 mA (B16)	2.4		V
		IOH = -16 mA (B16H)	2.4		V
VOL	Low-Level Output Voltage	IOH = 4 mA (B4)		0.4	V
		ERROR, L1BEMPTY, L1BFULL, TOUT0, TOUT1, CIO0-7, DIO0-31; IOH = -8 mA (B8)		0.4	V
		IOH = 16 mA (B16)		0.4	V
		IOH = 16 mA (B16H)		0.4	V
IOZ	3-state Output Leakage Current		-10	10	µA
IDDS	Quiescent Device Current	VIN = VDD or VSS		60	µA

5.4.AC Characteristics

(VDD=3.3V, Ta=25C, Cload=50pF)

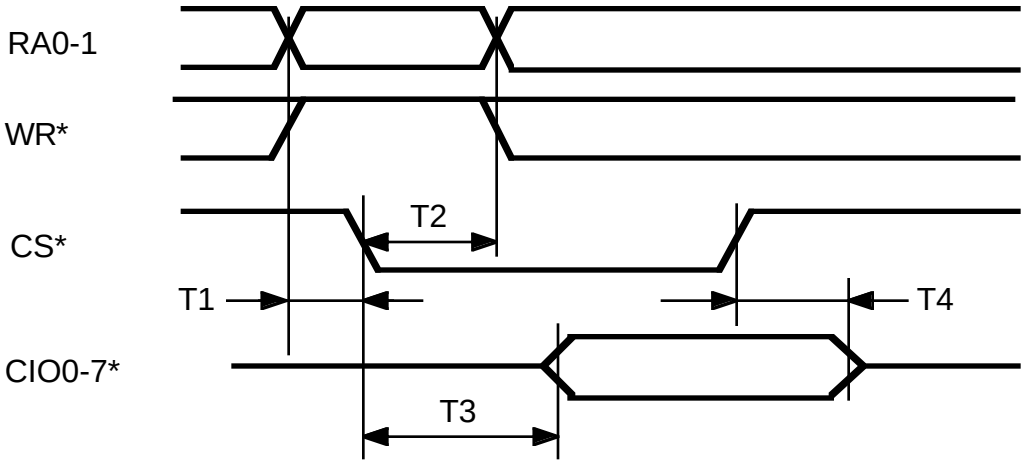
5.4.1.Clock Signal Characteristics

Synbol	Characteristics	Condition	Min	Typ	Max	Unit
f0	CLK frequency					
T1	CLK rise and fall time					
T2L/T2H	CLK duty factor					
ΔV/T3	CLK rise and fall rate					
T4L/T4H	CLK duty factor					
T5	External clock and PLL clock phase offset					
T6	External clock and PLL clock phase offset					ns
T7	Rising edge delay between OSCOUT and PLL clock					ns
T8	Falling edge delay between OSCOUT and PLL clock					ns

5.4.2.CSR Access Timing

Symbol	Characteristics	Min	Max	Unit
T1	RA, WR* setup time			ns
T2	RA, WR* hold time			ns
T3	CS* asserted to CIOx asserted			ns
T4	CS* negated to CIOx negated			ns
T5	CIO0-7 setup time			ns
T6	CIO0-7 hold time			ns
T7	Cycle time			ns
T8	CS* pulse width			ns

[CSR Read Cycle Timing Diagram]



[CSR Write Cycle Timing Diagram]