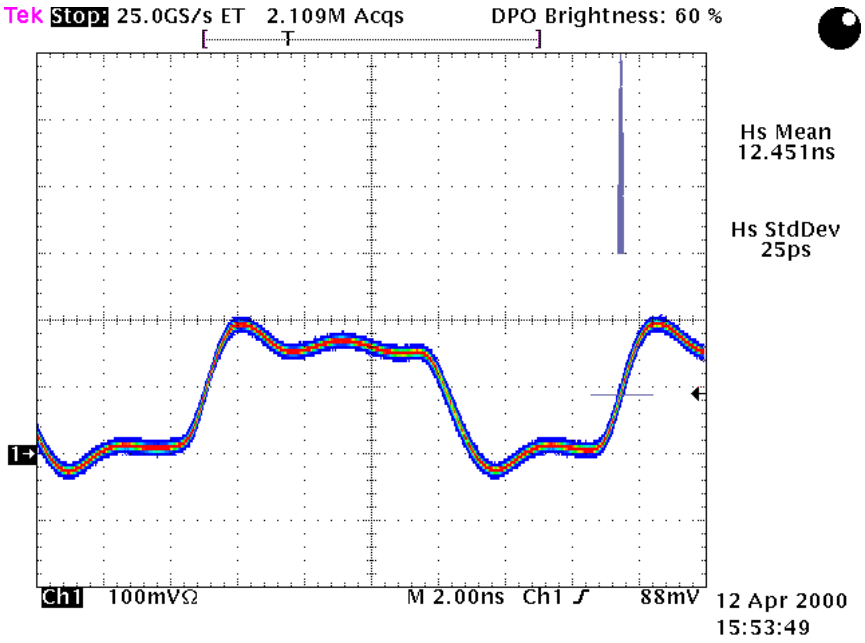
AMT-1
(ATLAS Muon TDC version 1)
Data Sheets

Yasuo Arai

KEK, National High Energy Accelerator Research Organization
1-1 Oho, Tsukuba, Ibaraki 305, Japan
yasuo.arai@kek.jp, http://atlas.kek.jp/~araiy/
Tel : +81-298-64-53
66, Fax : +81-298-64-2580

Chip designed on Mar, 2000

Rev. 0.1 Oct. 10, 2000.



Contents

1. Signal, Package and Pin Assignment

1.1. Signal description

Table. 1. Signal description.

Name	I/O	Description
RESETP / $\overline{\text{RESETM}}$	LVI	Reset signal.
ENCCONTP / $\overline{\text{ENCCONTM}}$	LVI	Encoded Control Signal.
HITP0 - 23 / $\overline{\text{HITM0 - 23}}$	LVI	Hit inputs.
BUNCHRSTP / $\overline{\text{BUNCHRSTM}}$	LVI	Bunch Count Reset signal.
EVENTRSTP / $\overline{\text{EVENTRSTM}}$	LVI	Event Count Reset signal.
TRIGP / $\overline{\text{TRIGM}}$	LVI	Trigger signal.
CLKP / $\overline{\text{CLKM}}$	LVI	System clock input.
CDIO0 - 11	I, TO	CSR data lines and Parallel data output[11:0]
CDIO12 - 31	TO	Parallel data output[31:12]
DREADY	O	Data Ready signal.
ERROR	O	Error signal
CLKOUT	O	PLL Clock, Start and Carry output signal. Controlled by clkout_mode bits.
TEST0 - 1	I, PD	Test mode select inputs. TEST=0 : Normal MOde TEST=1 : Toshiba standard test mode, TEST=2 : IDDS test mode, TEST=3 : Test clock mode.
TDO	TO	JTAG TDO.
TMS	I, PU	JTAG TMS.
TDI	I, PU	JTAG TDI.
TCK	I	JTAG TCK.
$\overline{\text{TRSTB}}$	I, PU	JTAG $\overline{\text{TRSTB}}$.
GETDATA	I	Get Data signal.
START	I	Start signal. Start coarse counter and enable channel inputs.
SERIOUTP / $\overline{\text{SERIOUTM}}$	LVO	Serial data output.
STROBEP / $\overline{\text{STROBEM}}$	LVO	Serial strobe output.
DSPACE	I	Data Space select signal. DSPACE = 1 : Parallel data, DSPACE = 0 : CSR space.
WR	I	CSR write signal.
CS	I	Chip Select signal.
RA0 - 4	I	CSR address signal
VGN	analog	PLL loop filter terminal. This pin should be connected to external capacitors of 6800 pF.

[I = CMOS Input, LVI = LVDS Input, O = CMOS Output, TO = Three State Output, LVO = LVDS Output; PU = with internal pull-up resistor, PD = with internal pull-down resistor, $\overline{\text{xxx}}$ = negative logic]

* LVDS input has a internal 100 ohm termination resistor.

1.2. Pin Assignment

Pin #	Name	Interface
1=	RESETM	WLVDSIN
2=	RESETP	WLVDSIN
3=	ENCCONTM	WLVDSIN
4=	ENCCONTP	WLVDSIN
5=	VDD	
6=	VSS	
7=	HITM0	WLVDSIN
8=	HITP0	WLVDSIN
9=	HITM1	WLVDSIN
10=	HITP1	WLVDSIN
11=	HITM2	WLVDSIN
12=	HITP2	WLVDSIN
13=	HITM3	WLVDSIN
14=	HITP3	WLVDSIN
15=	HITM4	WLVDSIN
16=	HITP4	WLVDSIN
17=	VSS	
18=	VDD	
19=	HITM5	WLVDSIN
20=	HITP5	WLVDSIN
21=	HITM6	WLVDSIN
22=	HITP6	WLVDSIN
23=	HITM7	WLVDSIN
24=	HITP7	WLVDSIN
25=	HITM8	WLVDSIN
26=	HITP8	WLVDSIN
27=	HITM9	WLVDSIN
28=	HITP9	WLVDSIN
29=	VDD	
30=	VSS	
31=	HITM10	WLVDSIN
32=	HITP10	WLVDSIN
33=	HITM11	WLVDSIN
34=	HITP11	WLVDSIN
35=	HITM12	WLVDSIN
36=	HITP12	WLVDSIN

Pin #	Name	Interface
37=	HITM13	WLVDSIN
38=	HITP13	WLVDSIN
39=	HITM14	WLVDSIN
40=	HITP14	WLVDSIN
41=	VDD	
42=	HITM15	WLVDSIN
43=	HITP15	WLVDSIN
44=	VSS	
45=	HITM16	WLVDSIN
46=	HITP16	WLVDSIN
47=	HITM17	WLVDSIN
48=	HITP17	WLVDSIN
49=	HITM18	WLVDSIN
50=	HITP18	WLVDSIN
51=	HITM19	WLVDSIN
52=	HITP19	WLVDSIN
53=	VDD	
54=	VSS	
55=	HITM20	WLVDSIN
56=	HITP20	WLVDSIN
57=	HITM21	WLVDSIN
58=	HITP21	WLVDSIN
59=	HITM22	WLVDSIN
60=	HITP22	WLVDSIN
61=	HITM23	WLVDSIN
62=	HITP23	WLVDSIN
63=	VDD	
64=	VSS	
65=	BUNCHRSTM	WLVDSIN
66=	BUNCHRSTP	WLVDSIN
67=	EVENTRSTM	WLVDSIN
68=	EVENTRSTP	WLVDSIN
69=	TRIGM	WLVDSIN
70=	TRIGP	WLVDSIN
71=	CLKM	WLVDSIN
72=	CLKP	WLVDSIN

Pin #	Name	Interface
73=	VSS	
74=	VDD	
75=	CDIO0	BD8RC
76=	CDIO1	BD8RC
77=	CDIO2	BD8RC
78=	CDIO3	BD8RC
79=	CDIO4	BD8RC
80=	CDIO5	BD8RC
81=	CDIO6	BD8RC
82=	VSS	
83=	CDIO7	BD8RC
84=	CDIO8	BD8RC
85=	CDIO9	BD8RC
86=	CDIO10	BD8RC
87=	CDIO11	BD8RC
88=	DIO12	BT8R
89=	DIO13	BT8R
90=	VDD	
91=	DIO14	BT8R
92=	DIO15	BT8R
93=	DIO16	BT8R
94=	DIO17	BT8R
95=	DIO18	BT8R
96=	DIO19	BT8R
97=	DIO20	BT8R
98=	VSS	
99=	DIO21	BT8R
100=	DIO22	BT8R
101=	DIO23	BT8R
102=	DIO24	BT8R
103=	DIO25	BT8R
104=	DIO26	BT8R
105=	DIO27	BT8R
106=	VDD	
107=	DIO28	BT8R
108=	DIO29	BT8R

Pin #	Name	Interface
109=	DIO30	BT8R
110=	DIO31	BT8R
111=	DREADY	B4R
112=	ERROR	B4R
113=	CLKOUT	B8R
114=	TEST0	IBUFD
115=	TDO	BT4
116=	VSS	
117=	VDD	
118=	TMS	IBUFU
119=	TDI	IBUFU
120=	TCK	IBUF
121=	TRSTB	IBUFU
122=	GETDATA	IBUF
123=	START	IBUF
124=	VSS	
125=	SERIOUTP	WLVDSOUT
126=	SERIOUTM	WLVDSOUT
127=	STROBEP	WLVDSOUT
128=	STROBEM	WLVDSOUT
129=	VDD	
130=	TEST1	IBUFD
131=	DSPACE	IBUF
132=	WR	IBUF
133=	CS	IBUF
134=	RA0	IBUF
135=	RA1	IBUF
136=	VSS	
137=	RA2	IBUF
138=	RA3	IBUF
139=	RA4	IBUF
140=	VDD	
141=	VSS	
142=	VGN	WDOUT
143=	VSS	
144=	VDD	

1.3.Package

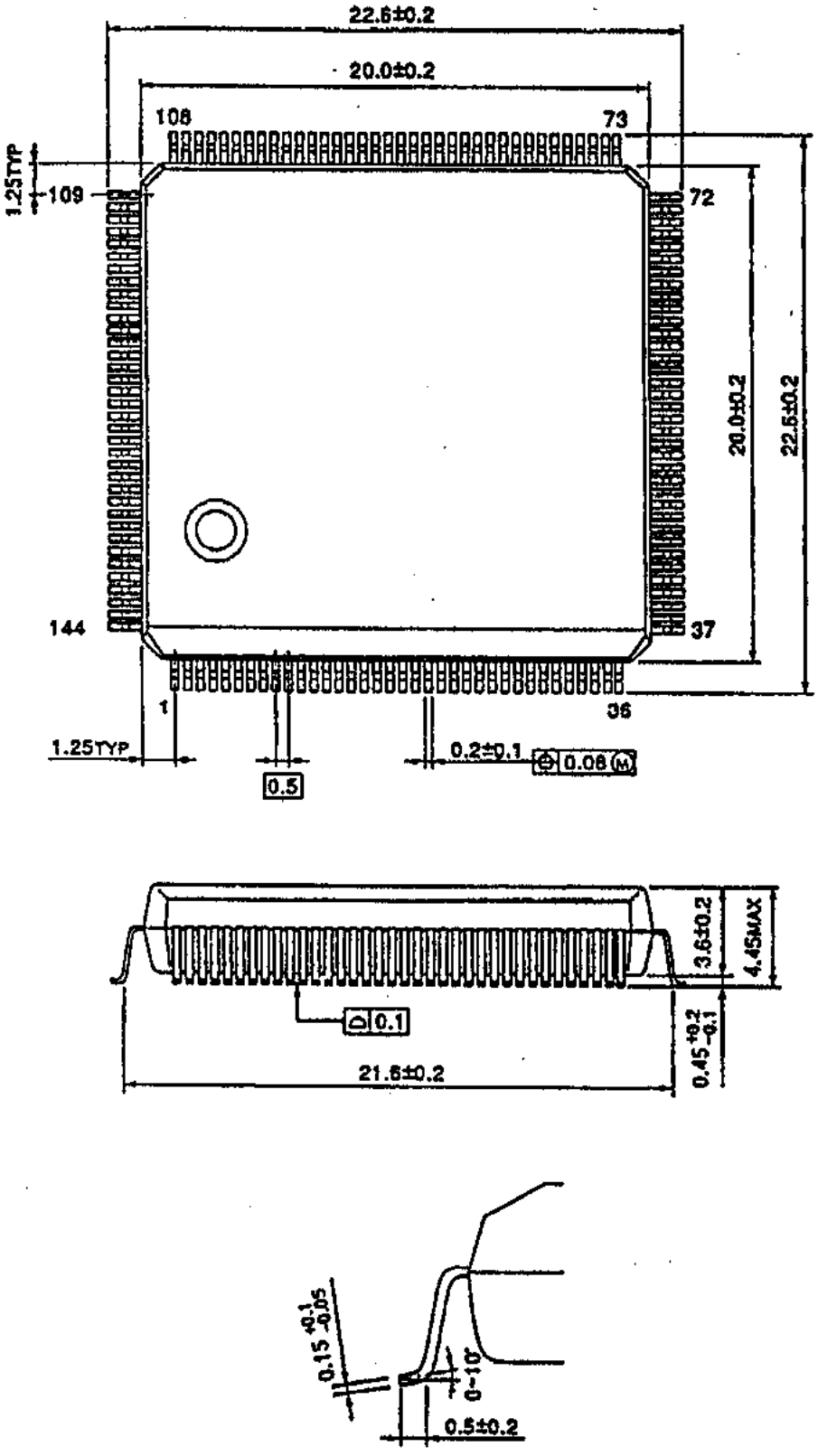


Fig. 1 QFP144 : 144-pin Plastic Flat Package

2.Electrical Characteristics

2.1.Maximum Ratings

Symbol	Parameter	Value
VDD	DC Supply Voltage	-0.3 to +5.0 V
VIN	Input Voltage	-0.3 to VDD+0.3 V
IIN	Input Current	±10 mA
T_{STG}	Storage Temperature	-40 to +125 ˚C

2.2. Recommended Operating Condition

(VSS = 0V)

Symbol	Parameter	Value
VDD	DC Supply Voltage	3.3 to 3.8 V
VIN	Input Voltage	VDD
Ta	Ambient Temperature	0 to +85 ˚C

2.3.DC Characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IH}	Input High Voltage		V_{DD} x 0.8		
V_{IL}	Input Low Voltage			V_{DD} x 0.2	
I_{IH}	Input High Current	$V_{IN} = V_{DD}$	-10	10	µA
	(with pull down resistor)		-10	200	µA
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$	-10	10	µA
	(with pull up resistor)		-200	10	µA
V_{OH}	High-level output voltage	I_{OH} = -4mA (B4: DREADY, ERROR, CLKOUT, TDO)	2.4		V
		I_{OH} = -8mA (B8: CDIO0-31)	2.4		V
V_{OL}	Low-level output voltage	I_{OH}=4mA (B4: DREADY, ERROR, CLKOUT, TDO)		0.4	V
		I_{OH} = 8mA (B8: CDIO0-31)		0.4	V
I_{OZ}	3-state output leakage current	$V_{OUT} = V_{DD}$ or V_{SS}	-10	10	µA
I_{DDS}	Quiescent device current(*)	$V_{IN} = V_{DD}$ or V_{SS} (TEST0 = 0, TEST1 = 1)		400	µA

(*) At present design, charge pump circuit in PLL is not cut off in the IDDS mode (TEST=2).

LVDS Input & Output

Symbol	Parameter	Condition	Min	Max	Unit
V_{OD}	Differential output voltage	R_L=100Ω	200	400	mV
V_{OC}	Common-mode output voltage	R_L=100Ω	0.9	1.4	V
V_I	Input voltage range		0	1.9	V

$\|V_{ID}\|$	Differential input voltage	(*)	200		mV
V_{ICM}	Input common mode voltage		50	1800	mV

(*) LVDS receiver contains an internal 100 ohm termination resistor.

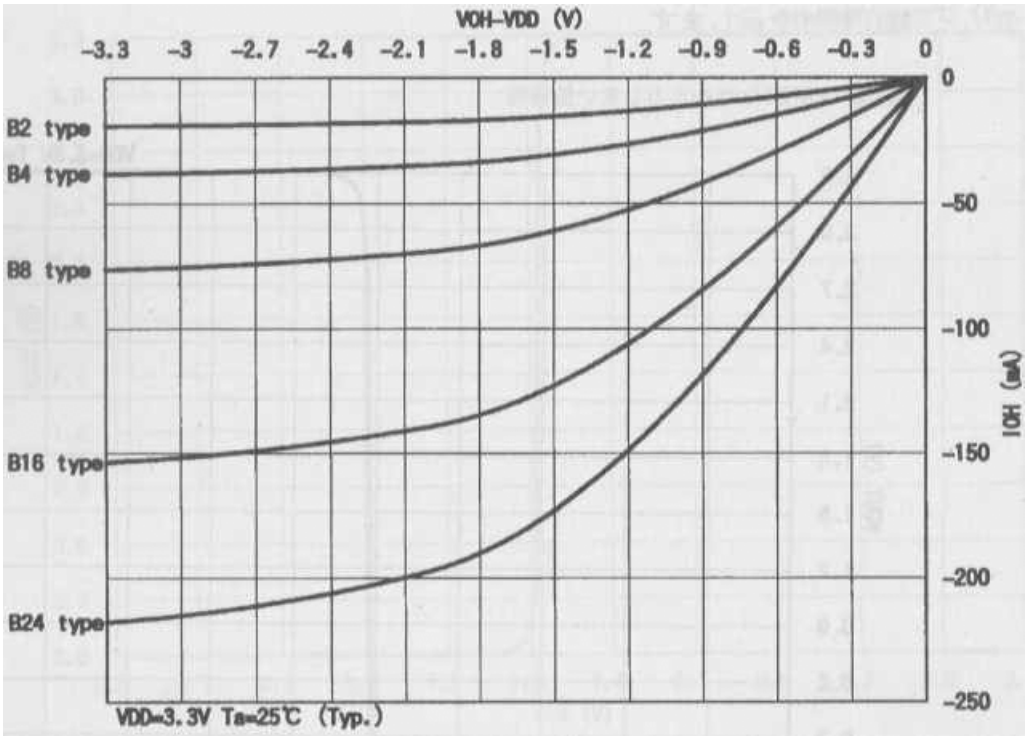


Fig. 2. Output Buffer VOH-IOH characteristics.

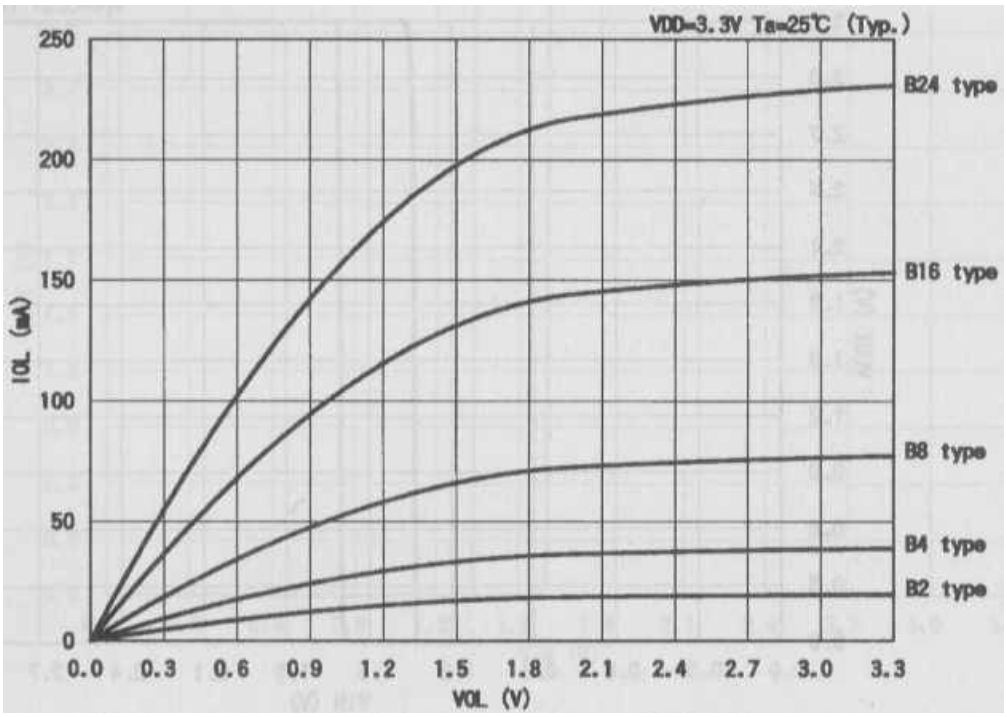


Fig. 3. Output Buffer VOL-IOL characteristics.

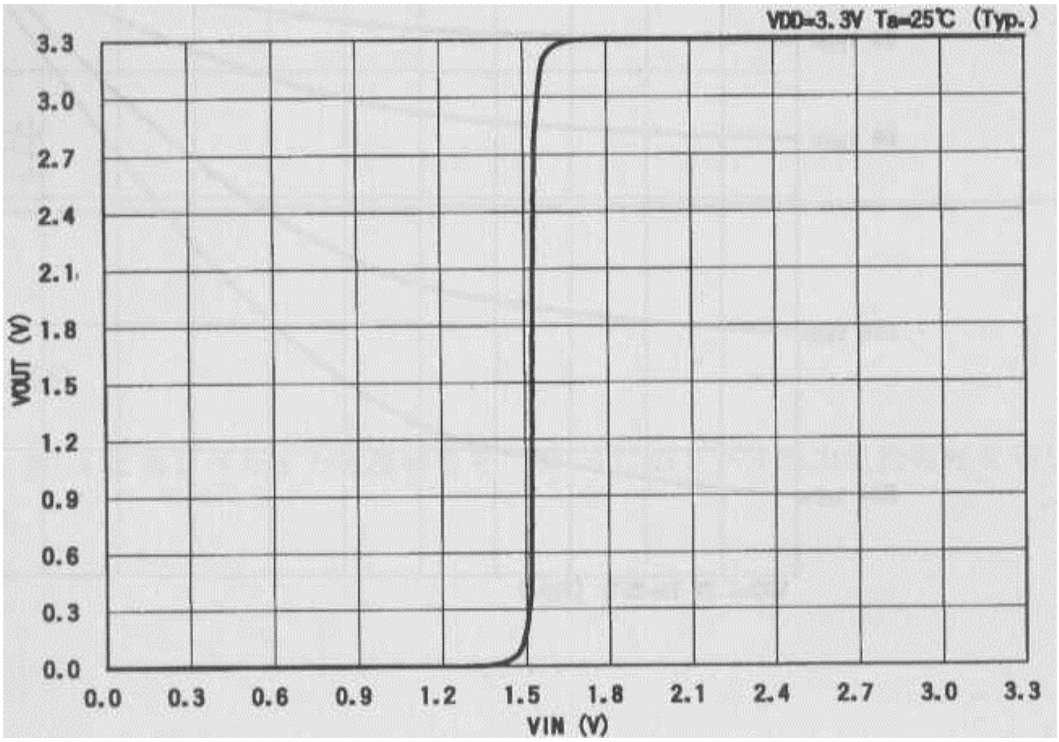


Fig. 4. CMOS Input Buffer characteristic.

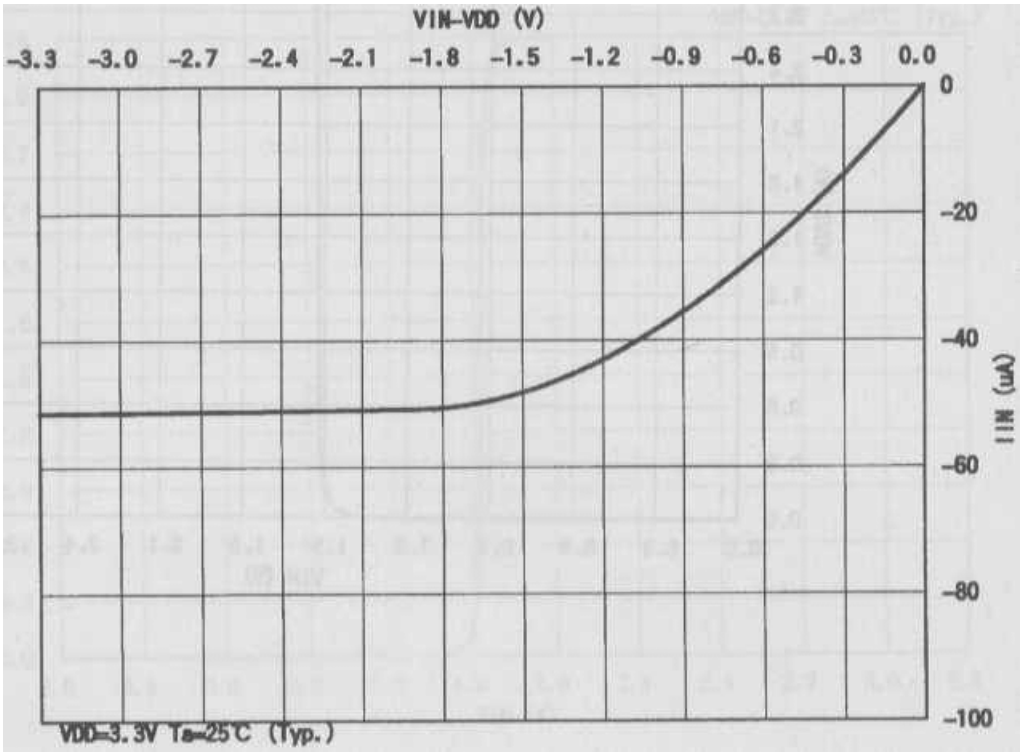


Fig. 5. Characteristic of Input buffer with Pull Up resistor.

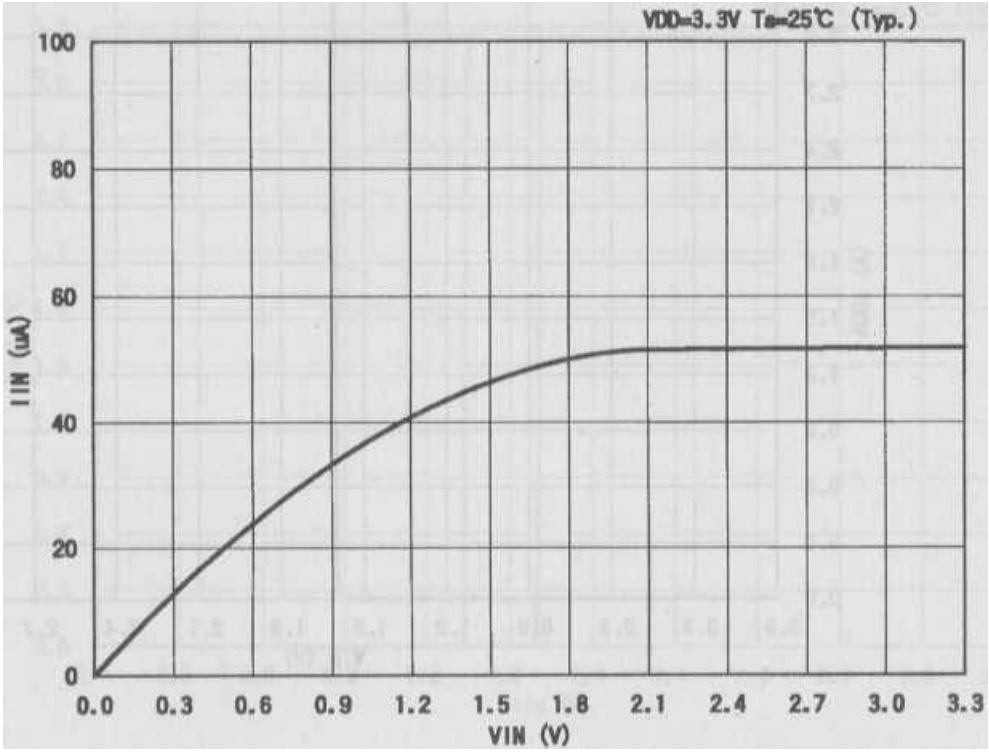


Fig. 6. Characteristic of Input Buffer with Pull Down resistor.

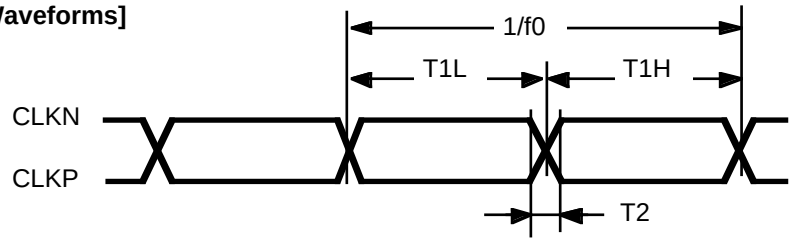
2.4.AC Characteristics

(VDD = 3.3 V, Ta = 25 ˚C, C_L = 30pF)

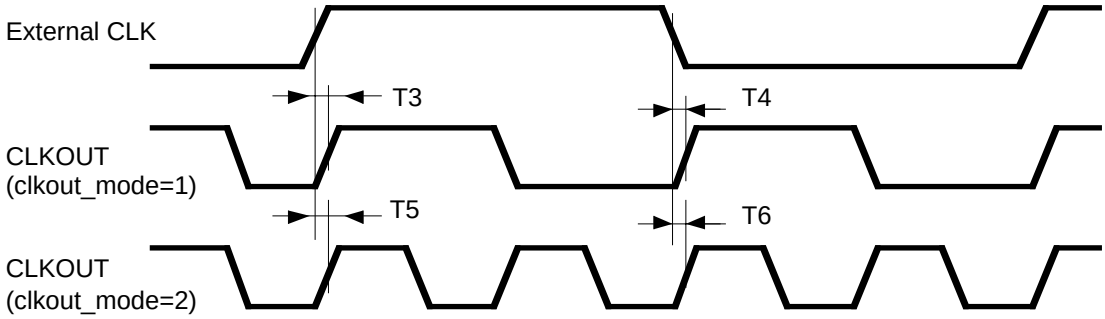
2.4.1.Clock Signal Characteristics (pll_multi=0)

Synbol	Characteristics	Condition	Min	Typ	Max	Unit
f0	CLK frequency			40	60	MHz
T1L/T1H	CLK duty factor		0.8	1	1.25	
T3	CLK transition time				2	ns
T4	External clock and CLKOUT phase offset	clkout_mode=1				ns
T5	External clock and CLKOUT phase offset	clkout_mode=1				ns
T6	External clock and CLKOUT phase offset	clkout_mode=2				ns
T7	External clock and CLKOUT phase offset	clkout_mode=2				ns

[Clock Waveforms]



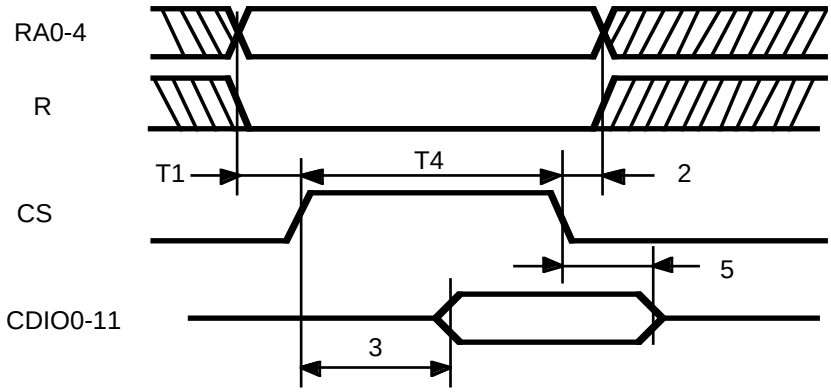
[Clock Offsets] (Pll_multi=0)



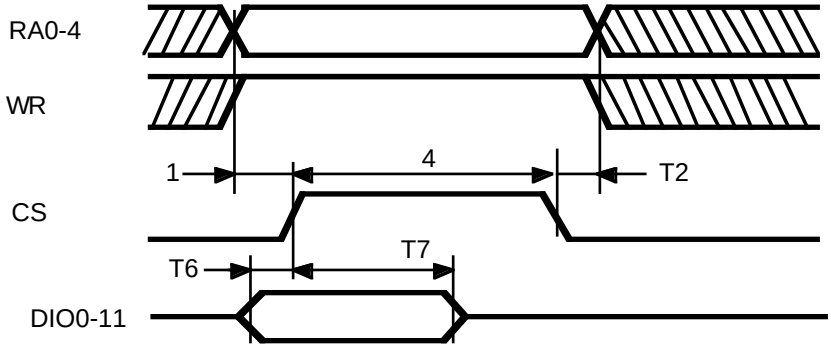
2.4.2.CSR Access Timing

Symbol	Characteristics	Min	Max	Unit
T1	RAx, WR setup time	1		ns
T2	CS negate to RAx, WR negate time	2		ns
T3	CS asserted to CDIOx asserted		17	ns
T4	CS pulse wiidth	8		ns
T5	CS negated to CDIOx negated		10	ns
T6	CDIO0-11 setup time	-1		ns
T7	CDIO0-11 hold time	9		ns

[CSR Read Cycle Timing Diagram]



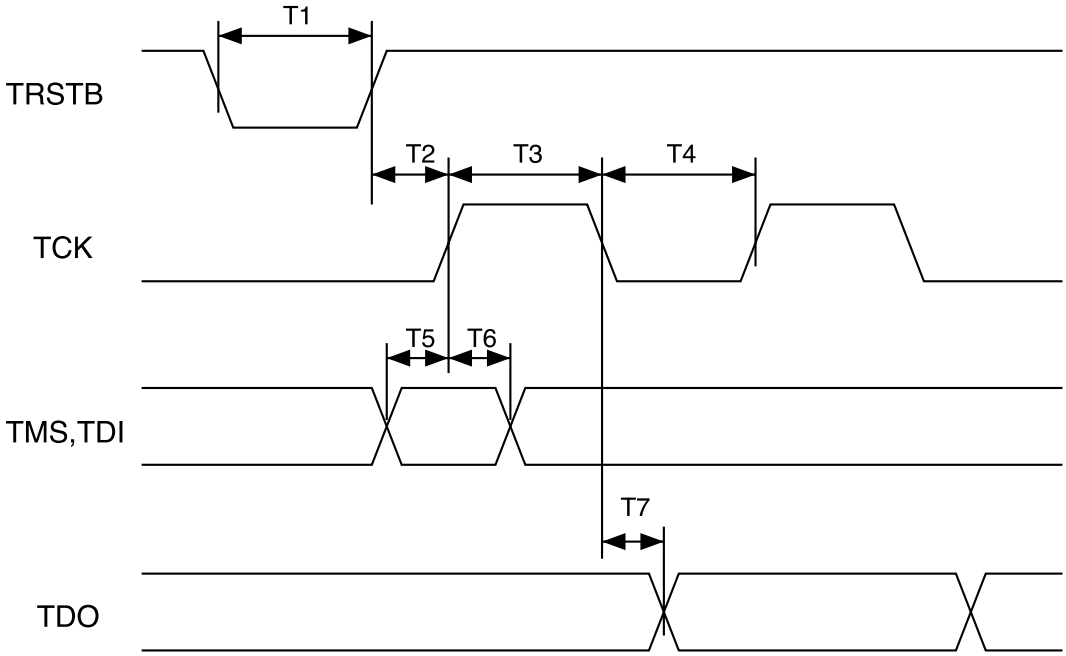
CSR Write Cycle Timing Diagram]



2.4.3.JTAG Timing

Symbol	Characteristics	Min	Max	Unit
T1	TRSTB width	4		ns
T2	TRSTB negate to TCK assert	3		ns
T3	TCK high width	6		ns
T4	TCK low width	6		ns
T5	TMS,TDI setup time	2		ns
T6	TMS,TDI hold time	2		ns
T7	TDO delay		8	ns

[JTAG Timing]



2.4.4.Serial Output Timing

Symbol	Characteristics	Condition	Min	Max	Unit
T1	SERIOUT-STROBE timing (leading strobe)	readout_speed=0(40Mbps)	-	-	ns
		readout_speed=1(20Mbps)	-	-	ns
		readout_speed=2(10Mbps)	-	-	ns
		readout_speed=3(80Mbps)	-0.5	1.5	ns
T2	SERIOUT-STROBE timing (DS strobe)	readout_speed=0(40Mbps)	-0.5	2	ns
		readout_speed=1(20Mbps)	-0.5	2	ns
		readout_speed=2(10Mbps)	-0.5	2	ns
		readout_speed=3(80Mbps)	-0.5	2	ns
T3	CLKOUT-STROBE timing (clkout_mode=2)	readout_speed=0(40Mbps)	3	5	ns
		readout_speed=1(20Mbps)	3	5	ns
		readout_speed=2(10Mbps)	3	5	ns
		readout_speed=3(80Mbps)	1.5	3.5	ns

[Serial Output Timing]