ATLAS

Production Readiness Review
ATLAS Muon TDC (AMT)

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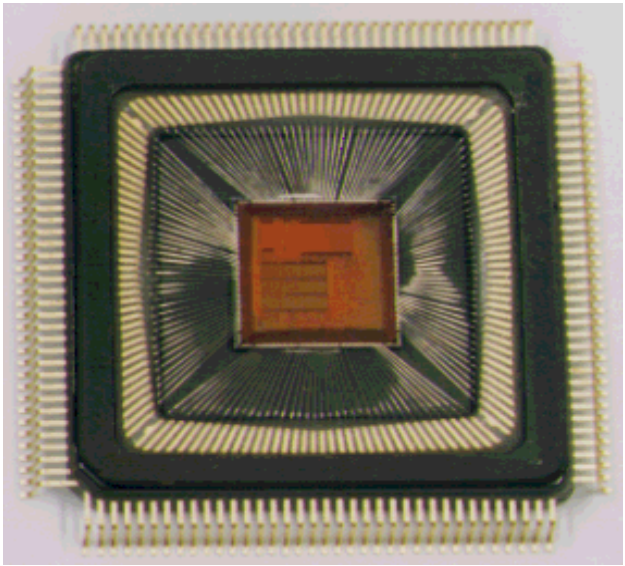
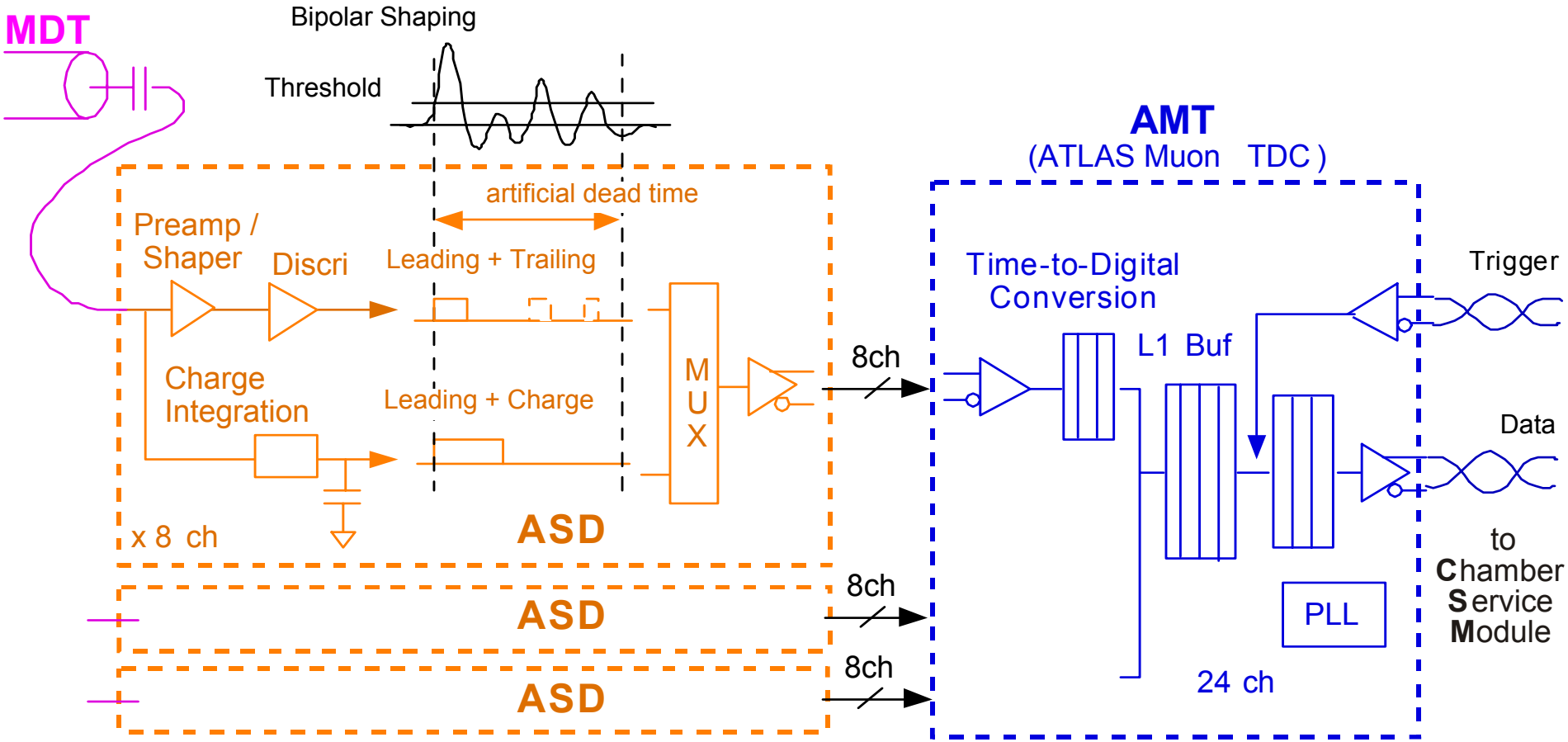
Specification of AMT

- Introduction
- MDT Front-end System
- Requirements
- Simulation Study



History

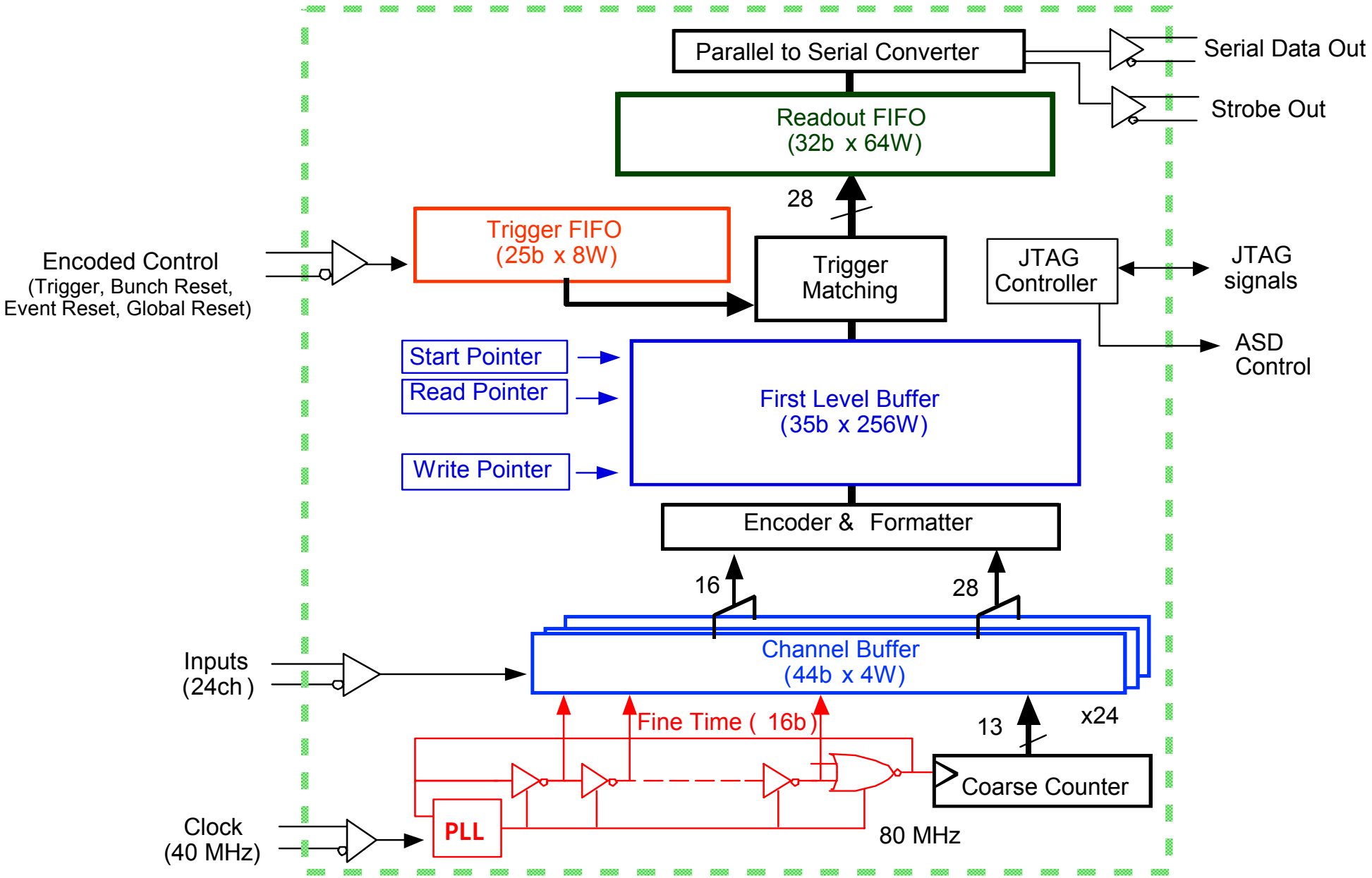
Year	Activities
1990	First TDC LSI was developed (CMOS 0.8 μm) at KEK.
1994	TDC for the SSC exp. was developed (CMOS 0.5 μm) at KEK
1996	Collaboration with CERN microelectronics group on the architecture study for the ATLAS TDC, and requirements document were written.
1998	A quick test chip (AMT-0, CMOS 0.7 μm) was developed at CERN.
1999	A test chip (AMT-TEG, CMOS 0.3 μm) was developed at KEK.
2000	A first prototype chip (AMT-1, CMOS 0.3 μm) was developed.
2001	Muon front end electronics Preliminary Design Review. Mezzanine boards with ASD-Lite and AMT-1 are developed and used in H8 beam test. Second prototype chip (AMT-2, CMOS 0.3 μm) was developed.
2002	Mezzanine board with ASD-8 and AMT-2 are developed and tested at Univ. of Michigan.



ATLAS MDT Front-end Electronics

Requirements to AMT

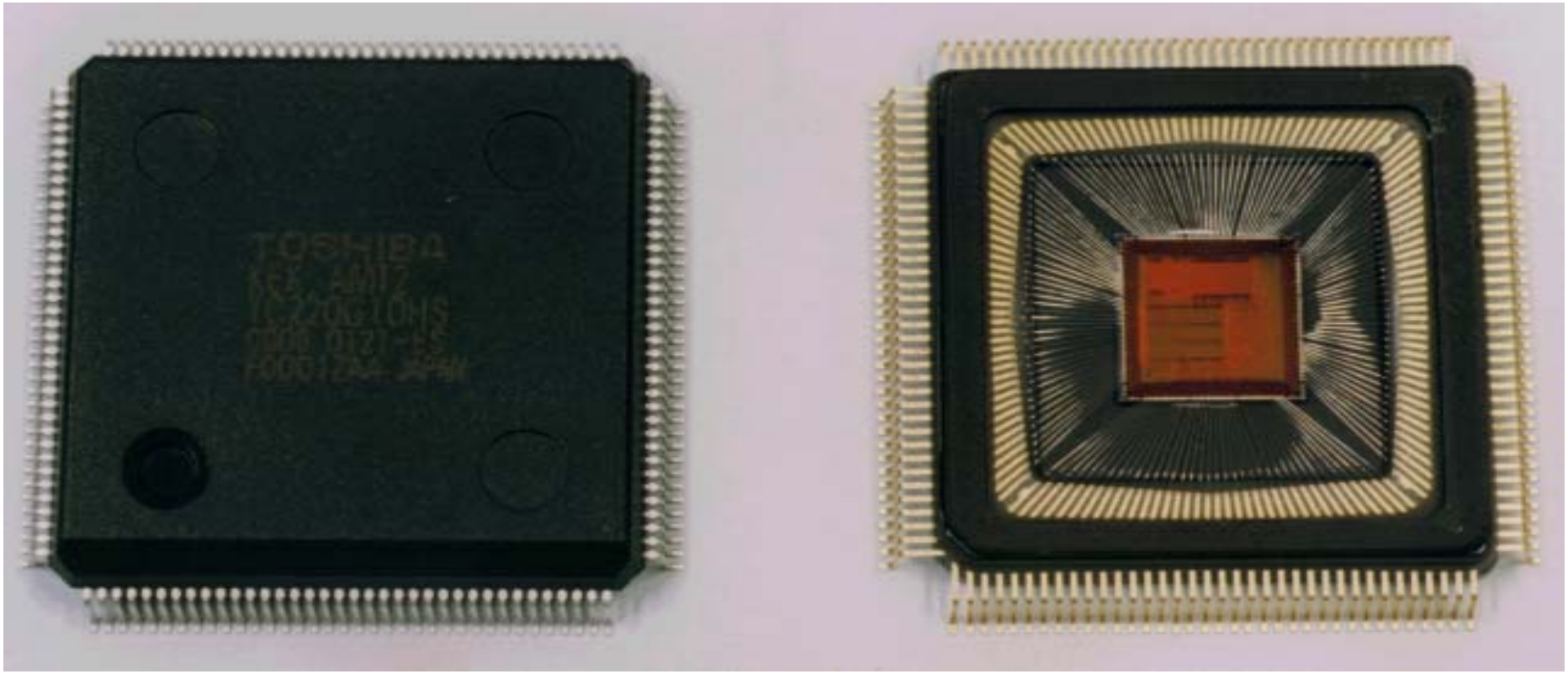
- ~370 k channels (16,000 chips)
- ~0.5 ns timing resolution
- 400 kHz max. input rate, 100 kHz trigger rate
- Leading and Width (Trailing edge) time measurement
- Mask Hit detection (optional)
- Shared Hit acquisition
- Trigger Latency > 2.5 μs
- Low-cost, Low-power (~10 mW/ch) & High-density (24 ch/chip)
- LVDS interface for active signals during measurement
- 40 Mbps Serial output
- Radiation Tolerant (~11 krad, 2×10^9 h/cm^2 @10year)
- JTAG I/F, BIST, Serial control



Block Diagram of the AMT

Specification of AMT

Least Time Count	0.78125 ns/bit
Time Resolution	RMS = 300 ps (leading and trailing edges)
Non Linearity	Max = +/-80 ps
No. of Channels	24 Channels
Serial Output	40 (10-80) Mbps with DS or edge strobe.
Double Hit	~5 ns
Max. Hit rate	400 kHz per channel
Max. trigger rate	100 kHz
Supply Voltage	3.3+-0.3V (~360 mW)
Process	0.3 μm CMOS Sea-of-Gate (Toshiba TC220G)
Number of Gate	110 k gates (36.2 % usage)
Package	0.5 mm lead pitch, 144 pin plastic QFP



Plastic Package

Ceramic Package

AMT-2 chip

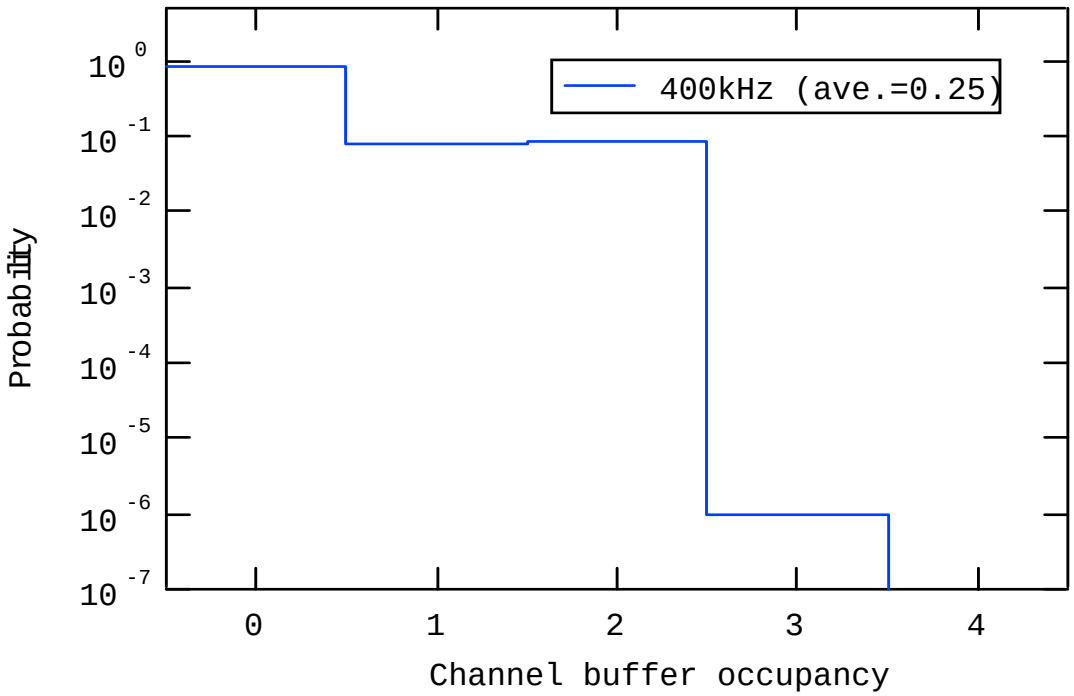
Simulation Condition

- 100 and 400 kHz hit rate (2/3 random hits and 1/3 correlated hits (4 hits))
- 100 kHz trigger rate (minimum separation is 125 ns)
- drift time = 0 ~ 800 ns
- pair (leading edge and width) mode measurement.
- pulse width = 10 ~ 200 ns
- dead time = 800 ns
- trigger latency = 2.5 μs
- mask & matching windows = 800 ns
- search window = 1000 ns
- reject offset = 3.5 μs
- both header and trailer words are read out
- a mask word is read out if exist
- Speed of the serial readout is 40Mbps.

Channel Buffer Occupancy

Since the data transfer rate of the channel buffer is faster than the input rate, there is no hit rejection in channel buffer.
(ASD dead time = 800 ns, time needed to transfer 24 hits = 650 ns)

Channel buffer occupancy for leading and trailing edge maeasurement in 800 k edges/sec.

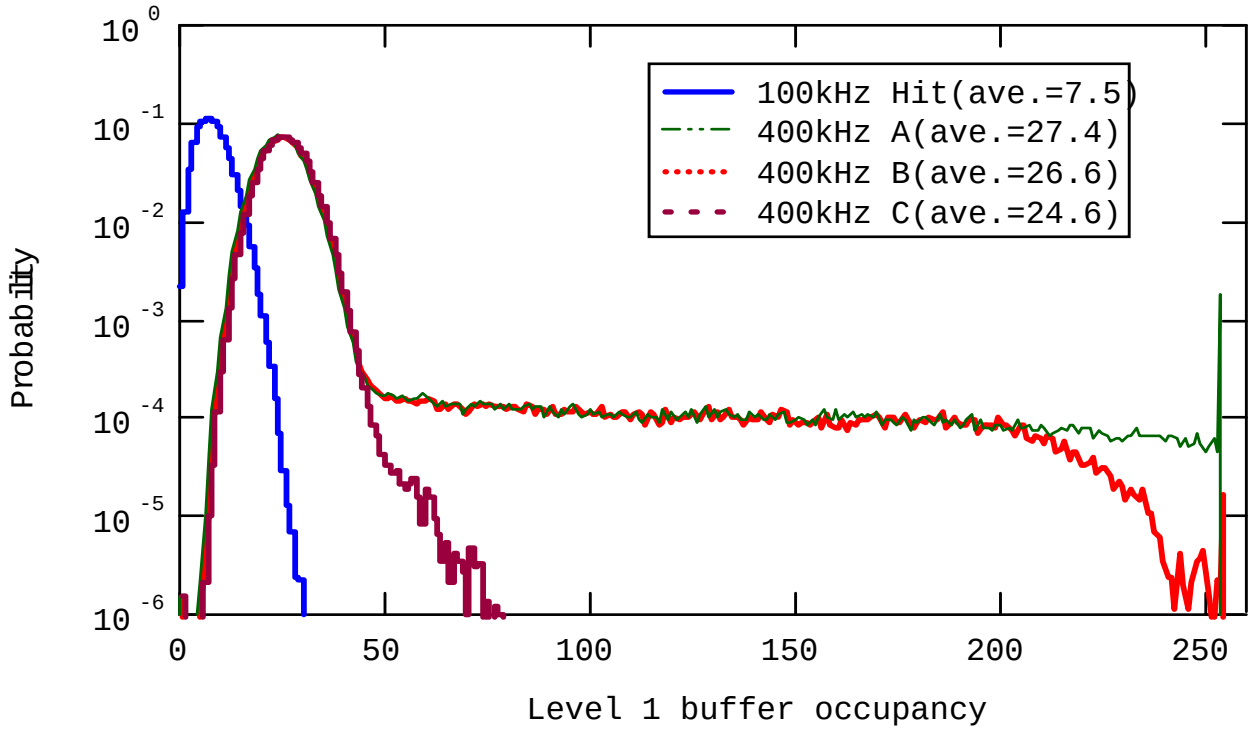


L1 Buffer Occupancy

Case A : No hit rejection from L1 buffer when the readout FIFO become full.

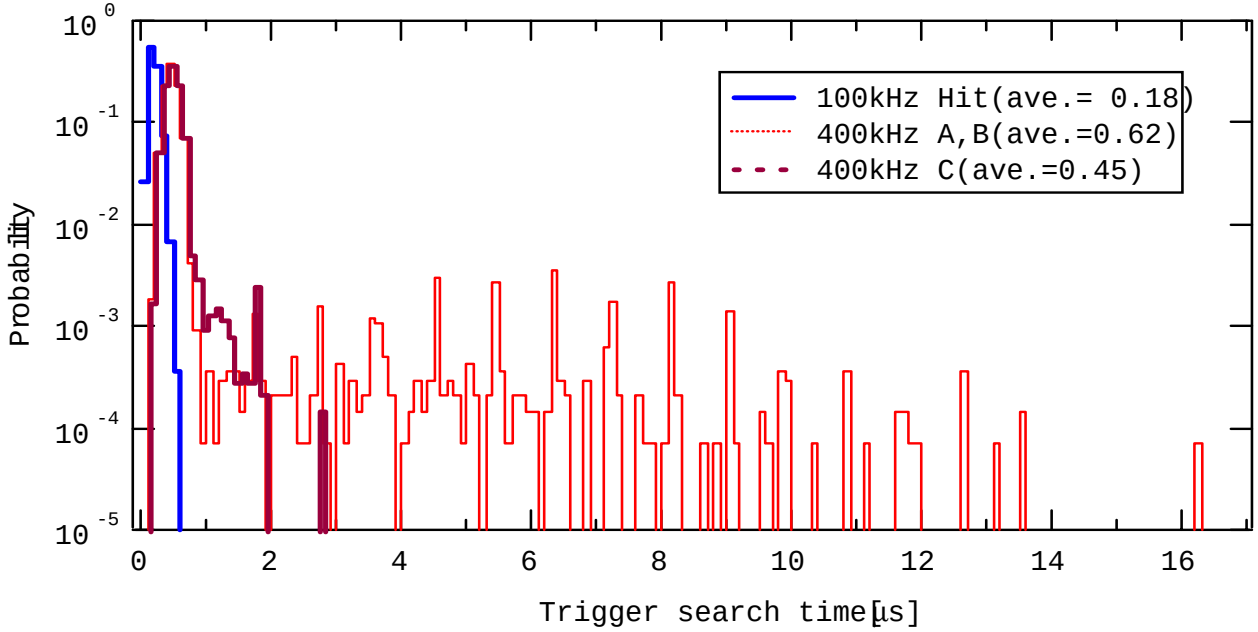
Case B : Hit rejection when the readout FIFO become full and L1 buffer occupancy become nearly full (192 word).

Case C : Hit rejection as soon as the readout FIFO become full .



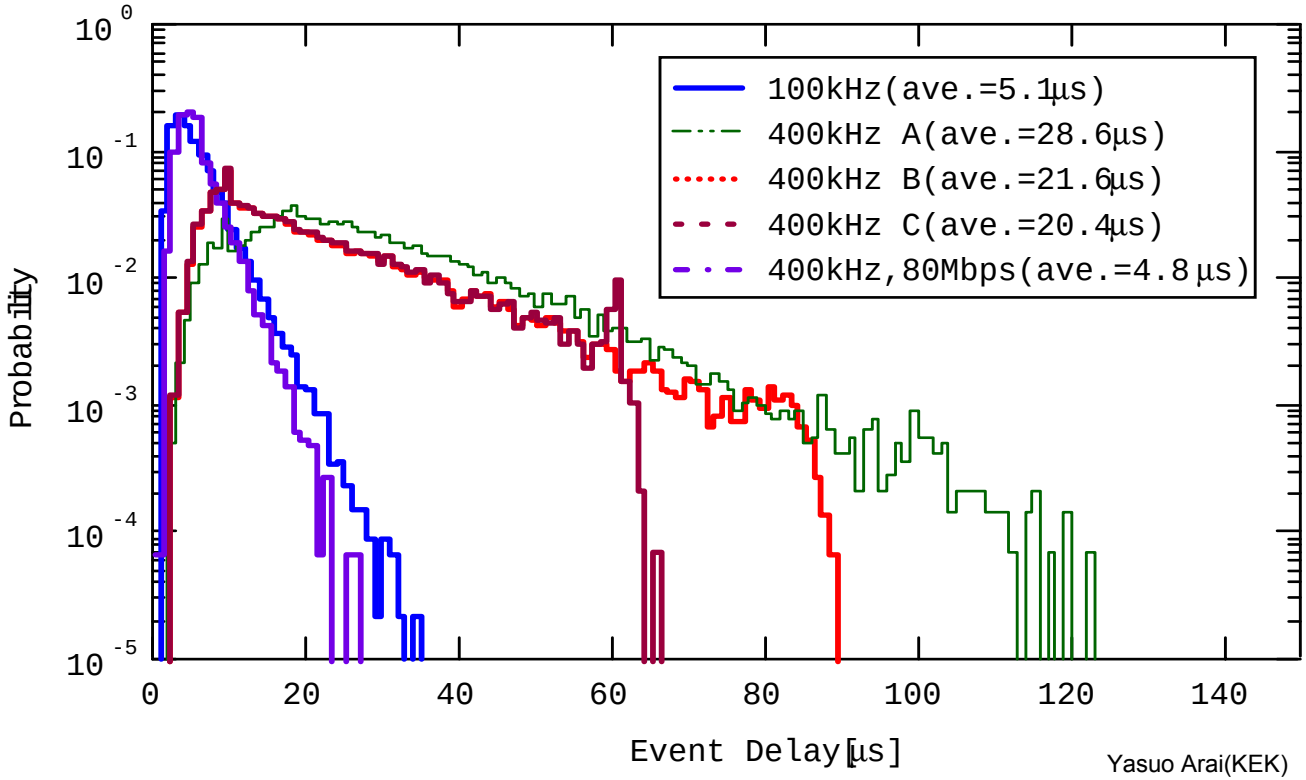
Trigger Search Time

Trigger Search Time must be less than AMT dynamic range (52 μsec).

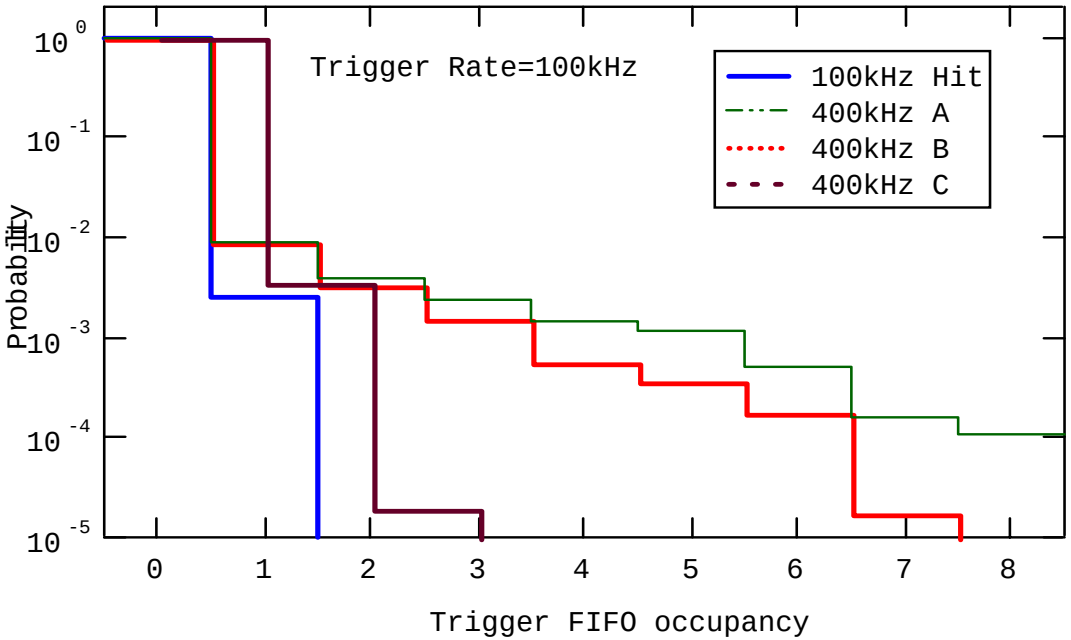


Event Delay

How long DAQ can wait an event?

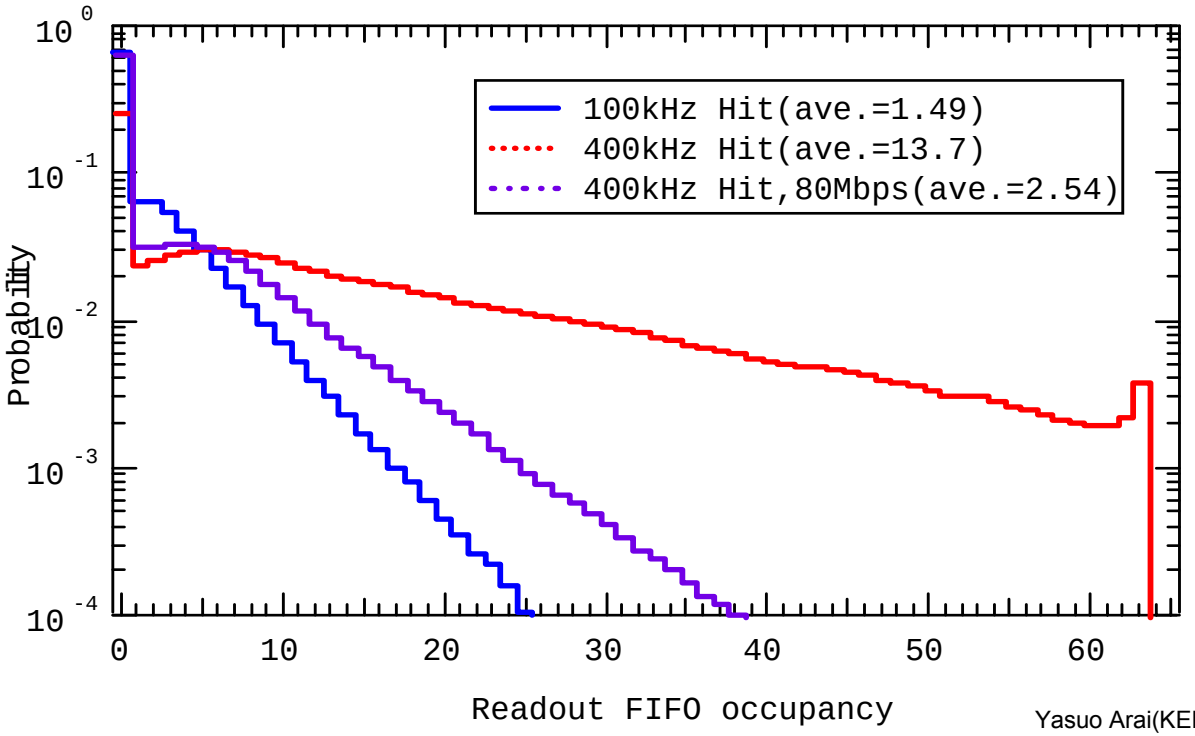


Trigger FIFO Occupancy



Readout FIFO Occupancy

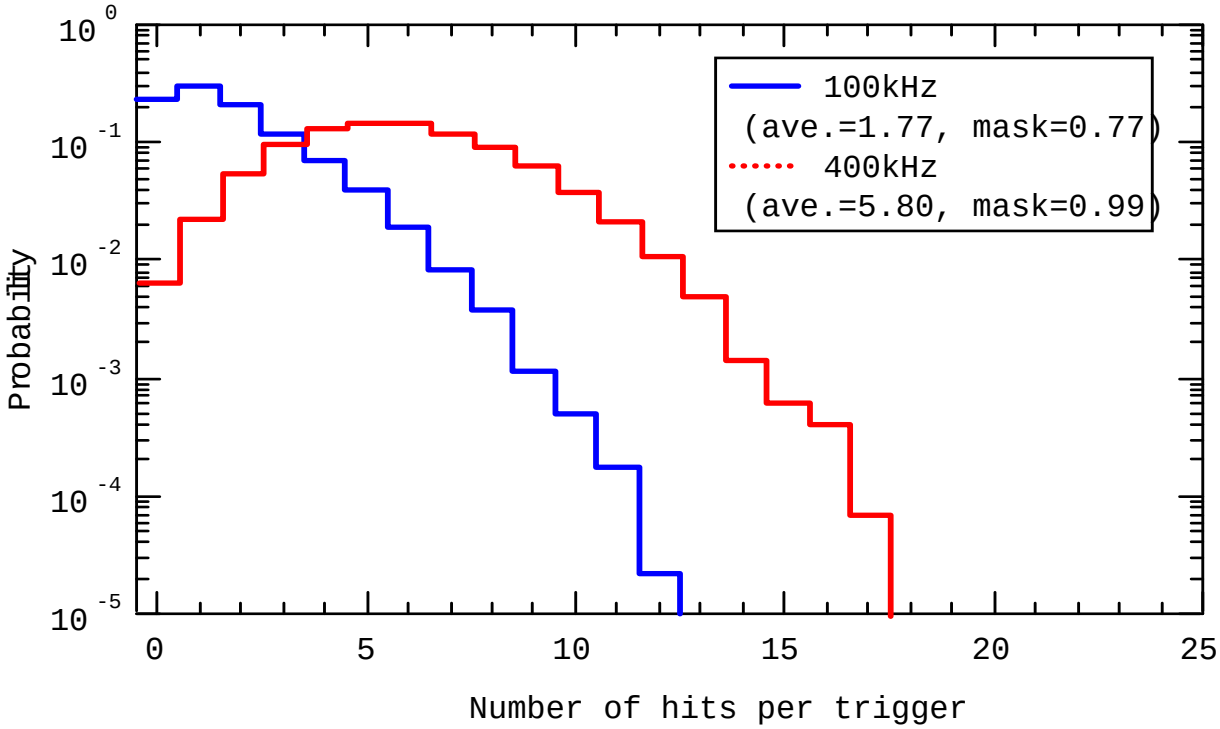
Independent of Hit Rejection method. Depend on readout Speed.



Number of Hits per Trigger

Event Delay : A > B > C

Rejected Hit : C > B > A



Hit Rate	Buffer Control Case	No. of Hits	No. of Mask	No. of words (incl. head, trailer and mask)	Rejected Hit ratio	Max. Event Delay
100 kHz		1.77	0.77	4.54	0%	40 µsec
400 kHz	A	5.80	0.99	8.79 (32 Mbps)	0.2%	130 µsec
	B				0.4%	90 µsec
	C				0.6%	70 µsec