Production Readiness Review
ATLAS Muon TDC (AMT)

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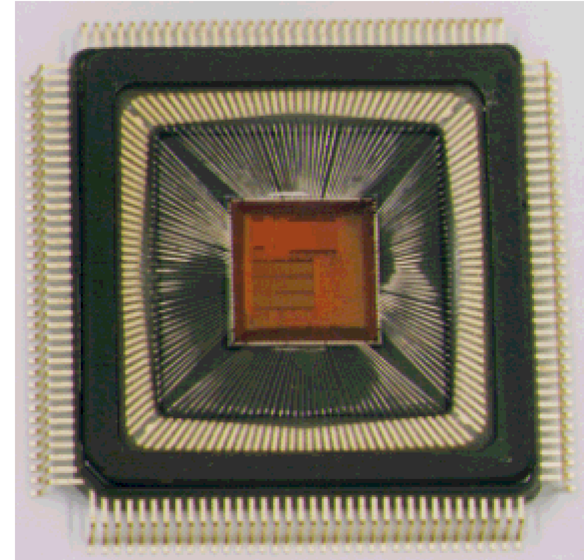
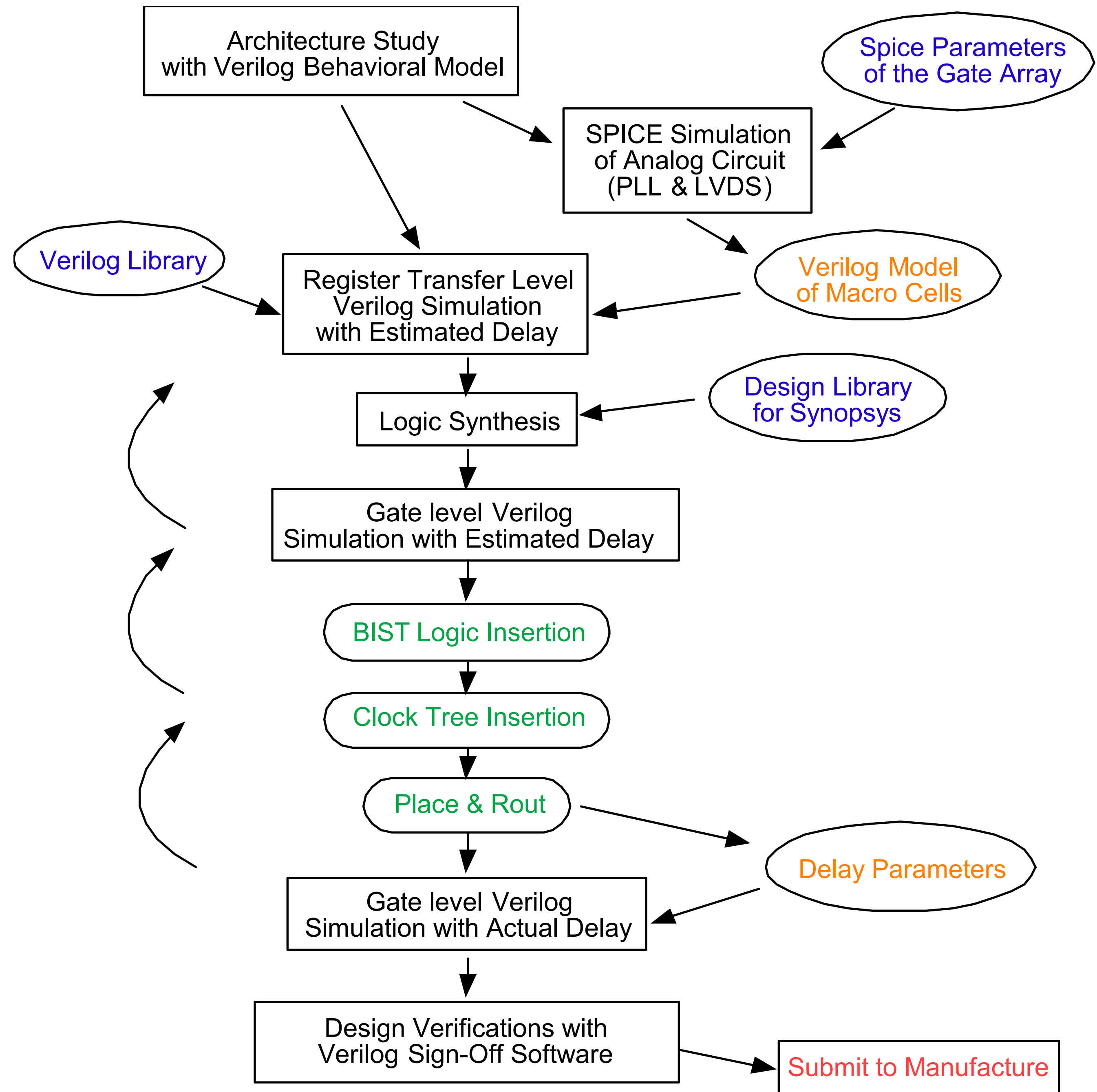
Yasuo Arai (KEK)
*yasuo.arai@kek.jp*
*http://atlas.kek.jp/tdc/PRR/*

# Design Verification & Test

- Design Flow
- Function Tests
- Time Resolution
- Power consumption
- Known Bugs



# Design Flow



# Design Summary

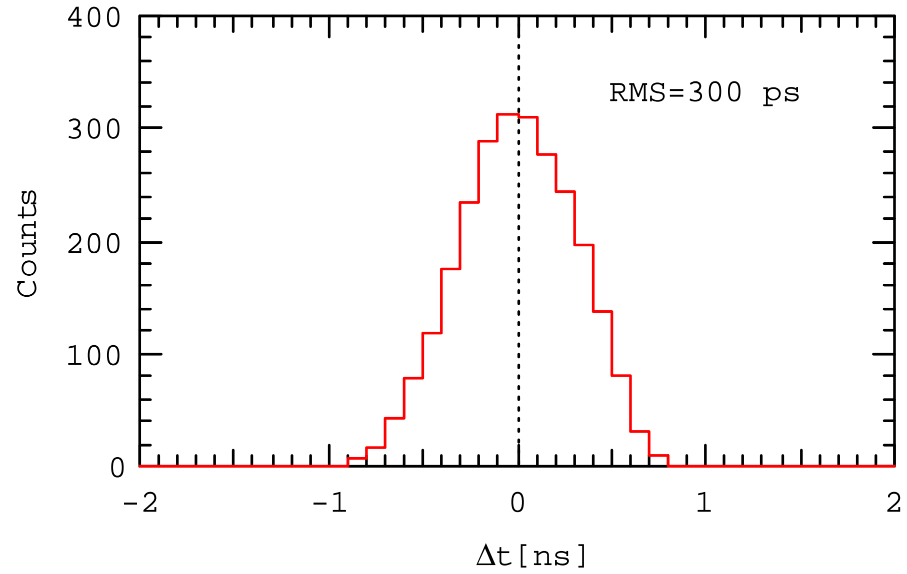
```
Number of input  pins    (excluding bidirectional pins) --------:       74
Number of output pins    (excluding bidirectional pins) --------:       26
Number of bidirectional pins -----------------------------------:       16
-----
Total number of I/O signal pins used ---------------------------:      116

Number of pad locations used for input  pins -------------------:       74
Number of pad locations used for output pins -------------------:       26
Number of pad locations used for bidirectional pins ------------:       16
-----
Total number of pad locations used for above -------------------:      116
Total number of pad locations available for above --------------:      160

Number of I/O slots used for input  buffers --------------------:      126
Number of I/O slots used for output buffers --------------------:       30
Number of I/O slots used for bidirectional buffers -------------:       16
Number of I/O slots used for internal buffers ------------------:       14
-----
Total number of I/O slots used for above -----------------------:      186
Total number of I/O slots available ----------------------------:      316

Number of redundant cells ( deleted ) --------------------------:       62

                                      Normal  Normal   IO     SMC
                                       cell   block  block  block   Total
------ ------ ------ ------  ------
Number of cell types used -----------:   117       5     15      0     137
Number of cell used -----------------: 11637       7     95      0   11739
Number of transistor pairs used -----: 69615  112990    216      0  182821
Number of gates used ----------------: 37854   69700    143      0  107697

Number of gates in master chip ---------------------------------:   297680
Array gate usage (%) -------------------------------------------:    36.18
Array gate usage excluding blocks (%) --------------------------:    16.61
```

## Test Patters for manufacturing

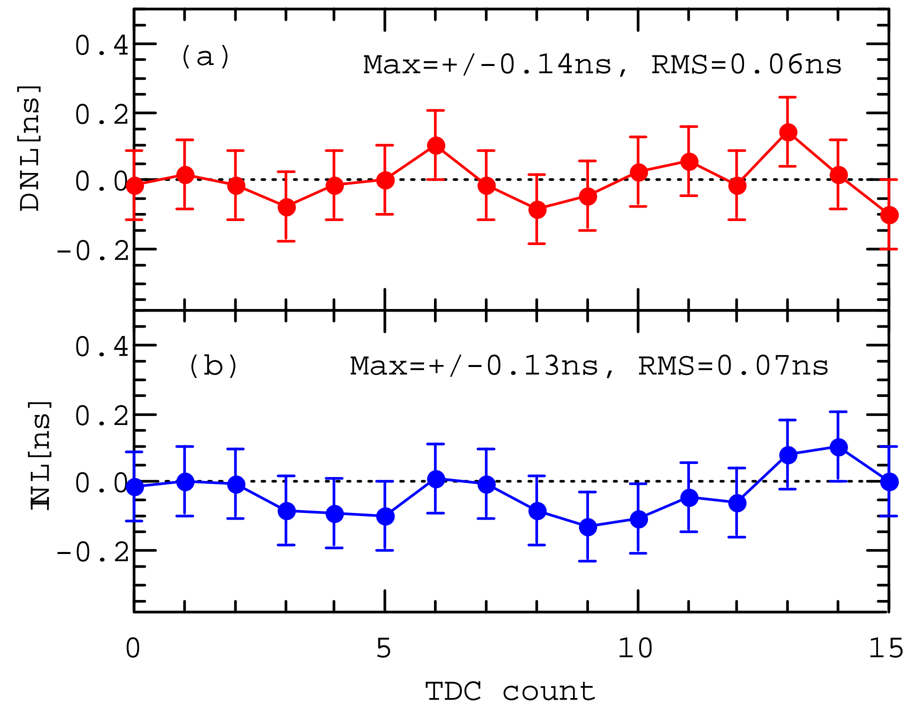
| | |
|---|---|
| fn1 | CSR read/write test and coarse counter test. |
| fn2 | Hit test 1 |
| fn3 | Hit test with serial readout |
| fn4 | Hit test with parallel readout |
| fn5 | JTAG test 1 |
| fn6 | Hit test with no trigger matching |
| fn7 | Encoded control input test |
| fn8 | Error Test。 |
| fn9 | Internal test with Core registers |
| fn10 | Channel buffer full test |
| fn11 | Level 1 buffer full test |
| fn12 | JTAG Test 2 and boundary scan test |
| fn13 | Hit Test 2 |
| pll | PLL oscillator stability test |
| idds | I/O buffer DC test and IDDS measurement |
| hiz | Output buffer Hi impedance test. |
| st | Toshiba standard test circuit test for input buff |
| bist | BIST test for memories. |

Toggle Check Coverage = 99.06%

## Time Resolution




## Differential & Integral Non-Linearity



# Test Summary

| | | |
|---|---|---|
| Time Resolution | Tested | OK |
| Double Pulse Resolution | Tested | OK |
| Leading/Trailing edge mode | Tested | OK |
| Pair mode measurement | Tested | OK |
| Channel buffer overflow | Tested | minor bug |
| L1 buffer overflow | Tested | OK |
| Trigger FIFO overflow | Tested | OK |
| Readout FIFO overflow | Tested | OK |
| Encoded Control Circuit | Tested | OK |
| Serial I/O | Tested | OK |
| JTAG I/F | Tested | OK |
| ASD Control | Tested | minor bug (extra TDO reg) |
| Trigger Matching | Tested | **major bug** |
| Mask Readout | Tested | OK |
| Error Reporting | Tested | minor bug |
| Power Consumption | Tested | OK |
| CSR Read/Write | Tested | OK |
| PLL | Tested | OK |

## Channel Buffer Overflow Error

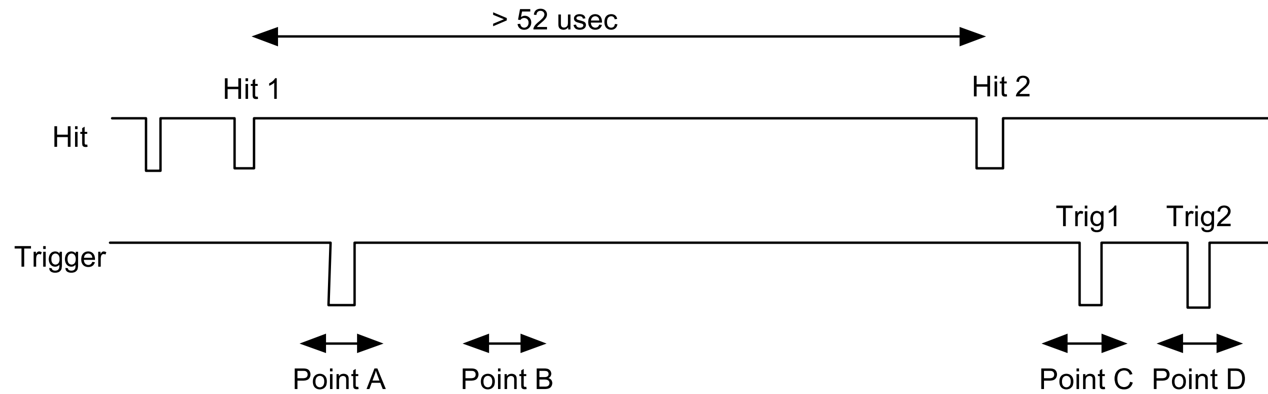
enable_rejected=1: report chan buf overflow as soon as the buf is available (O)

enable_reject=0: report chan buf oveflow with next valid hit. (X) (timing error)

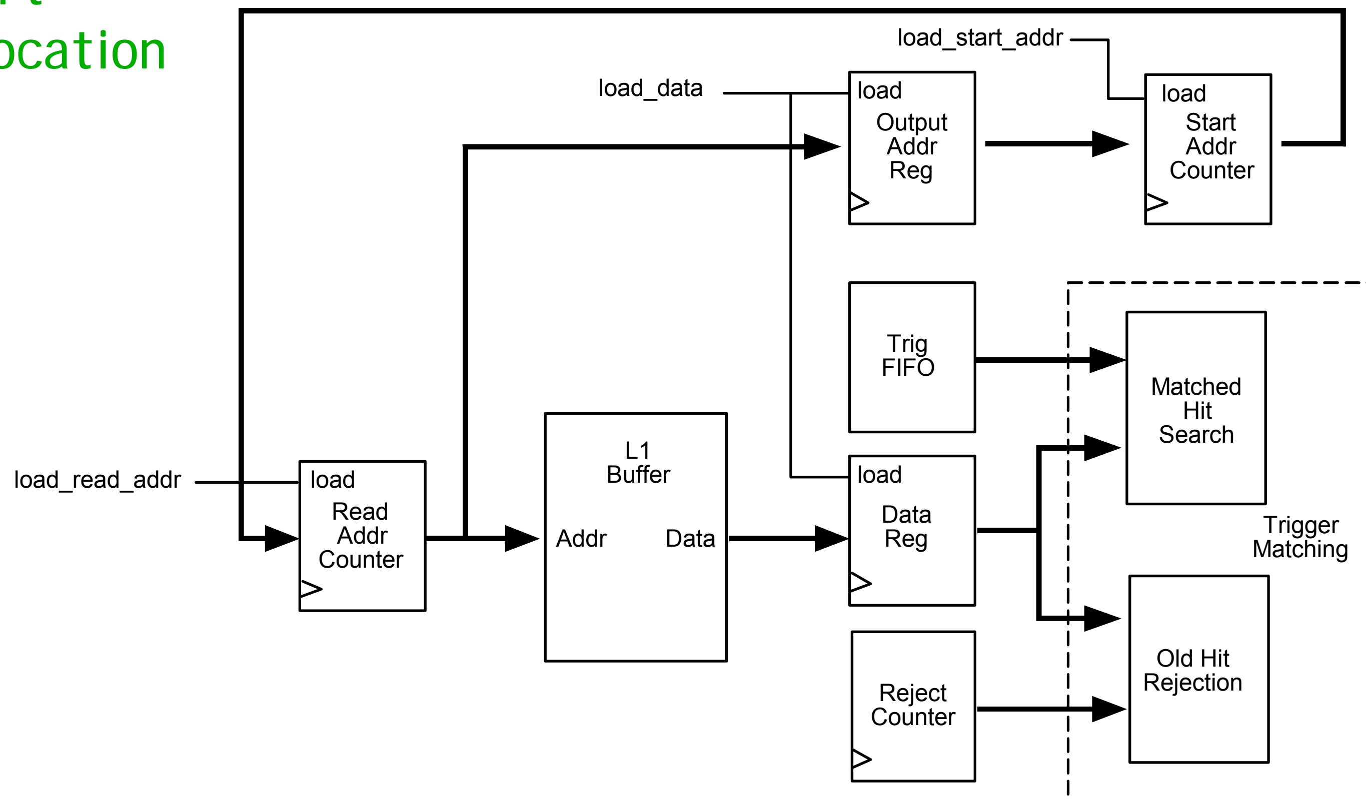
## Hardware Error Report Error

If enable this error reporting, an error word is inserted although no error occurs.
(can be checked by reading a CSR register through JTAG)

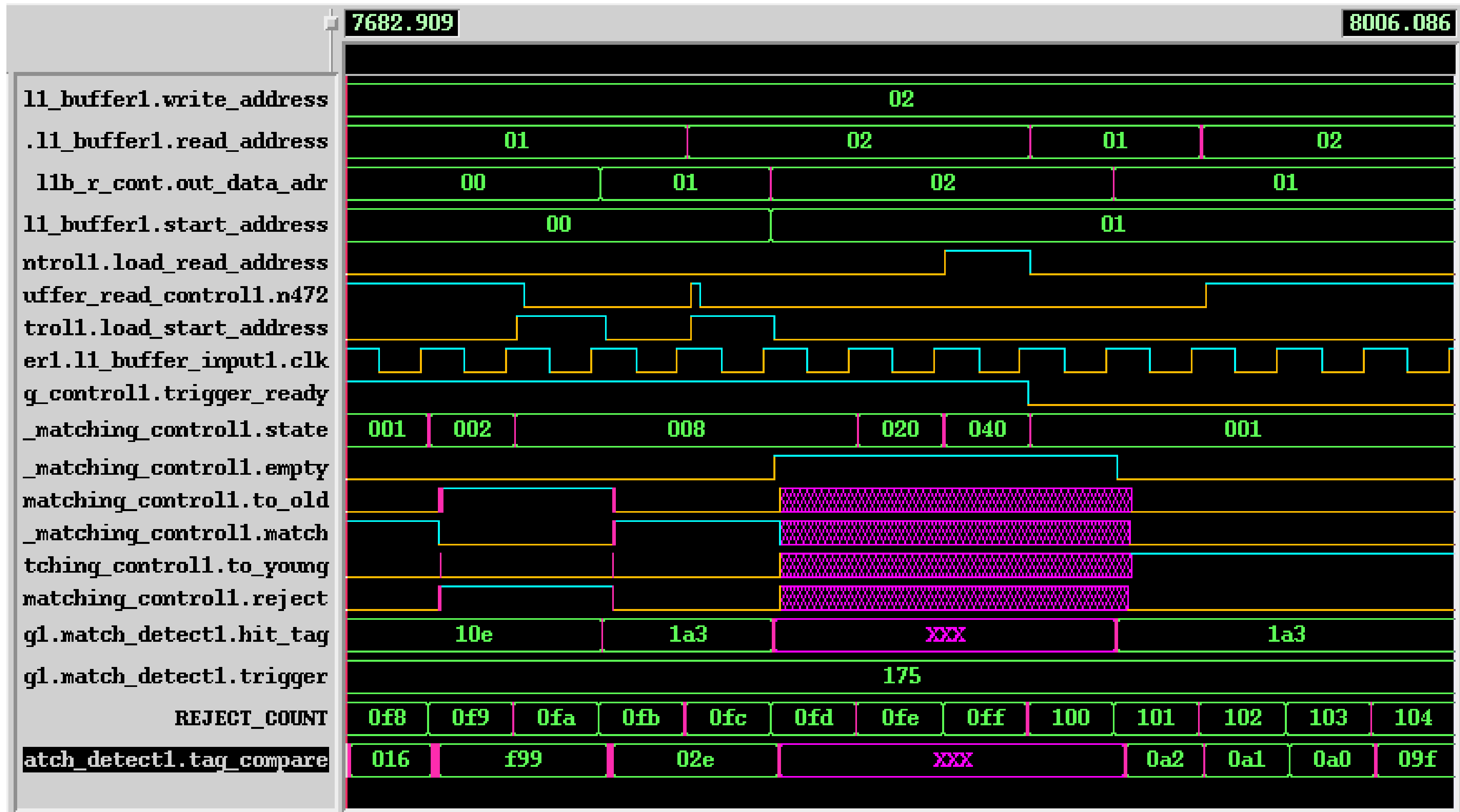
# Trigger Matching Error




Hit Miss and False Hit due to start pointer miss-location



# Point A (Normal Trigger matching)





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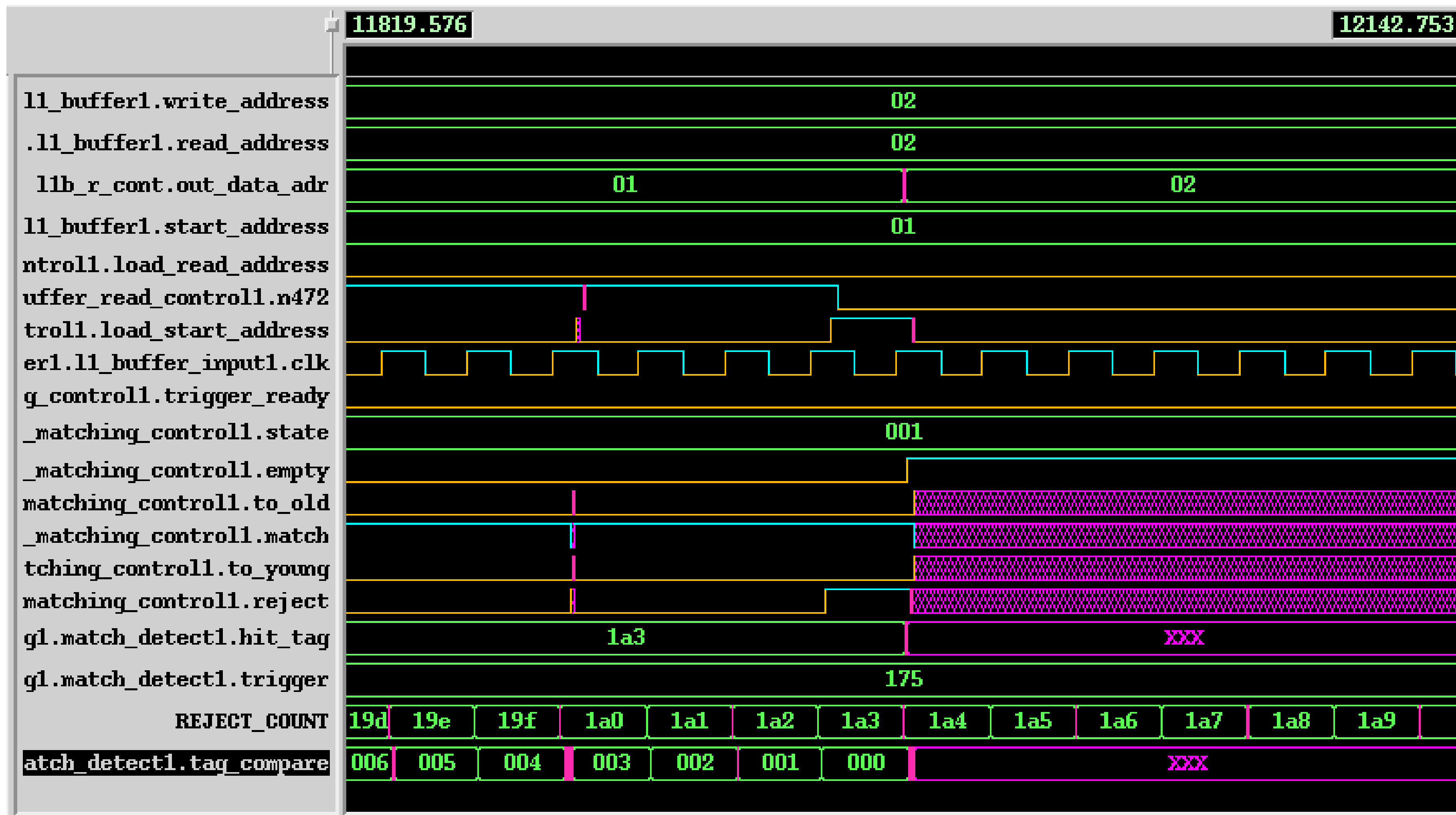
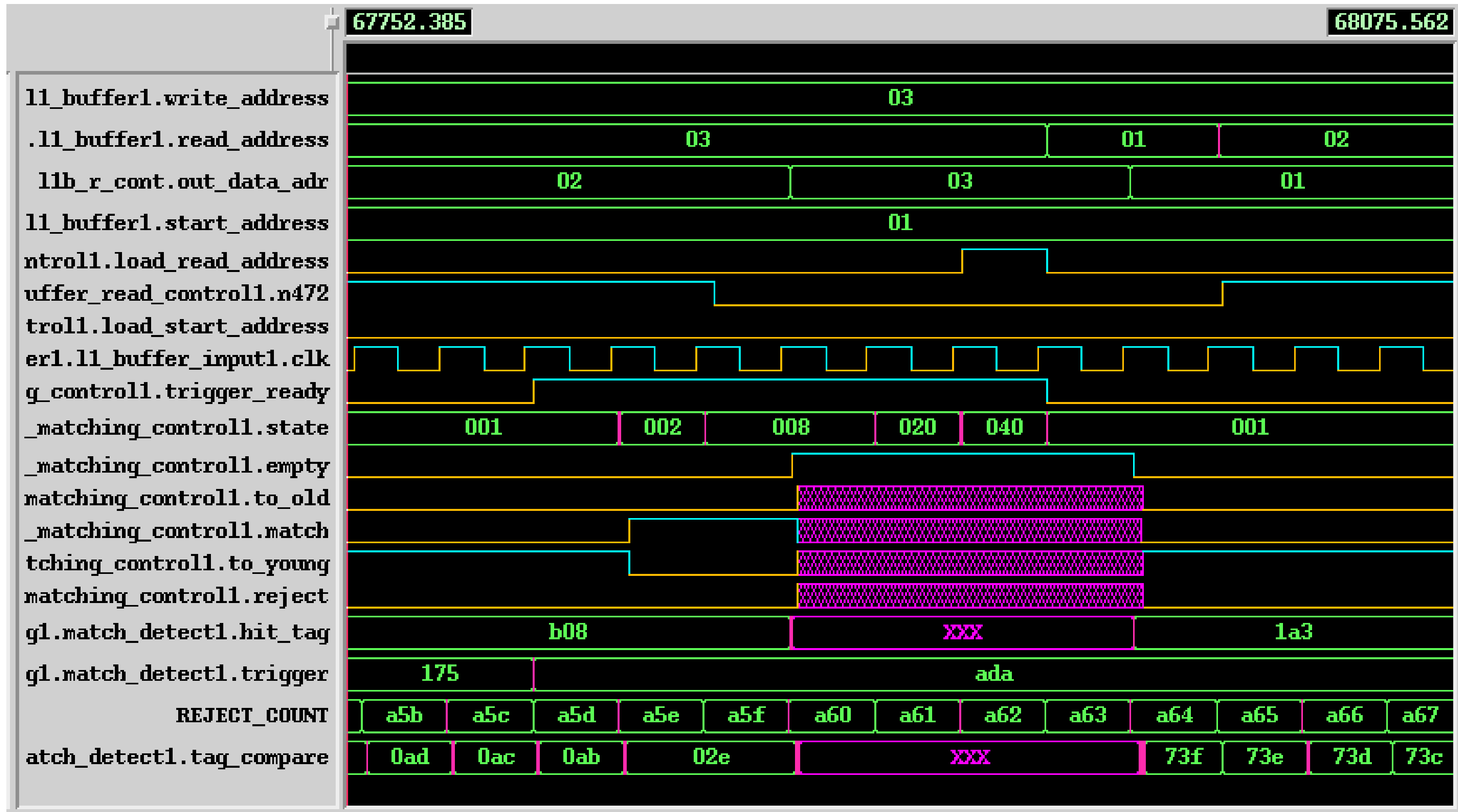
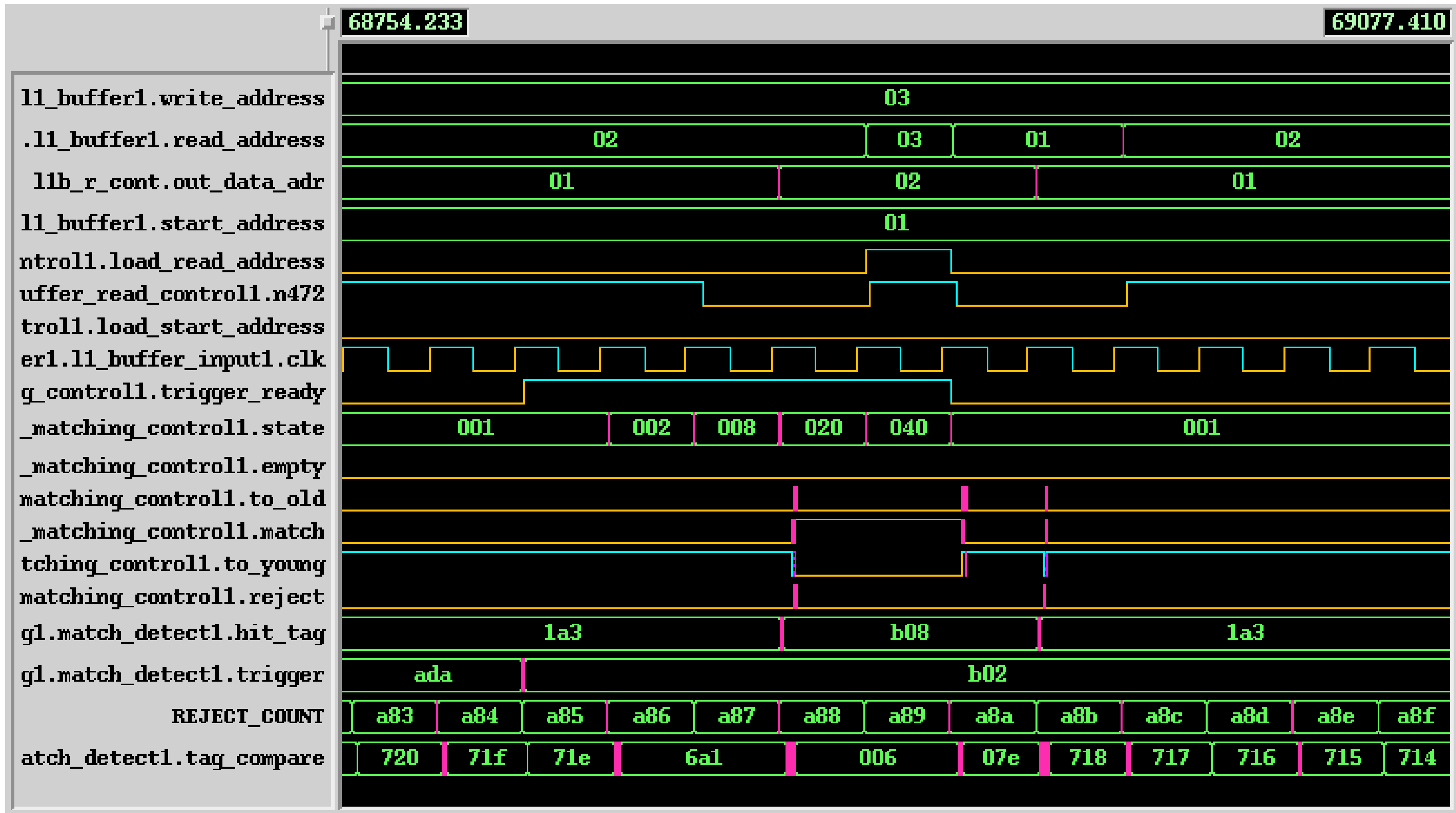
# Point B (Old Hit Rejection)



# Point C (1st Trigger)



# Point D (2nd Trigger)



## Condition of Error

12 bit Coarse Count : 0 ~ 102 μsec

Hit – Trigger : -51 μsec ~ +51 μsec

If a hit stay longer than 51 μsec, trigger matching goes bad order.