Please complete and submit this ATLAS Standard Form to ATLAS RHA Coordinator (<u>ARC</u>), at least 2 weeks after the date of the test.

<u>1. General information:</u>

| 1.1 | Date of the test: | Apr. 4 - 19, 2002 | |
|------|---|---------------------|--|
| 1.2 | Pre-selection, or Qualification ? (specify) | Pre-selection | |
| 1.3 | Name of the ATLAS (or other) System: | MDT | |
| 1.4 | Name of the board in the System: | MDT Mezzanine board | |
| 1.5 | Person responsible for the test: | Yasuo Arai | |
| 1.6 | Institute: | KEK | |
| 1.7 | Email: | yasuo.arai@kek.jp | |
| 1.8 | Person responsible for RHA of the Board: | Eric Hazen | |
| 1.9 | Institute: | Boston University | |
| 1.10 | Email: | Hazen@bu.edu | |

2. Component:

| 2.1 | Name: | AMT-2 | | |
|-------|--|--|--|--|
| 2.2 | Part Number: | TC220G10AF 0006 | | |
| 2.3 | Type (see section 12.1): | Front-end Electronics Device | | |
| 2.4 | Function (see section 12.1): | Drift Time Measurement | | |
| 2.5 | Main specification of the component: 24ch T | DC device. Time resolution is 0.78 ns/bit. | | |
| | | | | |
| 2.6 | Design (specify: COTS/ASIC): | ASIC | | |
| 2.7 | Design center (if known): | KEK | | |
| Man | ıfacturer: | | | |
| 2.8 | Name of the manufacturer: | Toshiba Co. | | |
| 2.9 | Address of the manufacturer (if known): | Kawasaki, Japan | | |
| 2.10 | Phone of the manufacturer (if known): | | | |
| 2.11 | Email of the manufacturer (if known): | | | |
| 2.12 | Web URL of the manufacturer (if known): | | | |
| Samp | Sampling: | | | |
| 2.13 | Number of tested components (irradiated): | 10 | | |
| 2.14 | Number of reference components (un-irradiated): | 1 | | |
| Batch | n origin: | | | |
| 2.15 | Batch origin (Homogeneous/Unknown): | Homogeneous | | |
| 2.16 | Manufacturing date code (for homogeneous batch): | 0210EAI | | |
| 2.17 | Manufacturing line code (for homogeneous batch): | F005 3ABA | | |
| | nology: | - | | |
| 2.18 | Name of the technology (if known): | TC220G | | |
| 2.19 | Technology (CMOS/BiCMOS/Bipolar/AsGa/Other): | CMOS | | |
| 2.20 | Minimum geometry (µm) : | 0.3 µm | | |
| Pack | age: | | | |
| 2.21 | Туре: | QFP | | |
| 2.22 | Part number: | QFP144-2020-0.50 | | |
| 2.23 | Number of pin: | 144 pins | | |
| 2.24 | Ceramic ? Plastic ? hybrid ? (specify) | Plastic | | |

3. Radiation:

| 3.1 | Name of the radiation facility: | RI facility of Tokyo Metropolitan Univ. |
|-----|---|---|
| 3.2 | Address of the radiation facility: | Hachioji, Tokyo, Japan |
| 3.3 | Radiation source (see 12.2) : | Co-60 |
| 3.4 | Radiation type (see 12.2) : | Photon gamma 1.173MeV and 1.332MeV |
| 3.5 | Radiation energy: | 1.173MeV and 1.332MeV |
| 3.6 | Dose rate (Gray/s) : | 0.6 Gray/s |
| 3.7 | Total dose after last step (Gray) : | 200 Gray |
| 3.8 | NIEL (if any) after last step (1 MeV eq. n/cm2) : | |
| 3.9 | Dosimetry / Calibration method: | Fricke Radiation Meter |

4. Radiation test method (see 12.3): (put an "X" to designate your answer. Specify in 4.10 if necessary)

| 4.1 | Extended TID test method for pre-selection of CMOS devices? | Х |
|------|--|---|
| 4.2 | Simplified TID test method for pre-selection of CMOS devices? | |
| 4.3 | Extended TID test method for pre-selection of bipolar devices? | |
| 4.4 | Simplified TID test method for pre-selection of bipolar devices? | |
| 4.5 | Extended TID test method for qualification of CMOS batches? | |
| 4.6 | Simplified TID test method for qualification of CMOS batches? | |
| 4.7 | Extended TID test method for qualification of bipolar or BiCMOS batches? | |
| 4.8 | Simplified TID test method for qualification of bipolar or BiCMOS batches? | |
| 4.9 | Other TID test method? | |
| 4.10 | Which other TID test method (specify) ? | |
| | | |
| | | |

<u>5. Total dose:</u> (if the irradiation is made in one single step, answer to question 5.1 and 5.2 only)

| 5.1 | Total number of irradiation steps: | |
|-----|---|----------|
| 5.2 | TID (Gray) after step 1: | 200 Gray |
| 5.3 | TID (Gray) after step 2 (if more than one step): | |
| 5.4 | TID (Gray) after step 3 (if more than two steps): | |
| 5.5 | TID (Gray) after step 4 (if more than three steps): | |
| 5.6 | TID (Gray) after step 5 (if more than four steps): | |
| 5.7 | TID (Gray) after step 6 (if more than five steps): | |

6. Simulation of Low Dose Rate Effects (see 12.4):

| Bipo | Bipolar devices only: | | | |
|------|--|---|--|--|
| 6.1 | Did you perform irradiation at elevated temperature to simulate low dose | | | |
| | rate effects (Y/N) ? | | | |
| 6.2 | If "yes" to Q.6.1, how much irradiation pre-tests did you perform to | | | |
| | determine the worst case temperature? | | | |
| 6.3 | If "yes" to Q.6.1, what is the worst temperature determined from pre-tests (°C)? | | | |
| 6.4 | If "no" to Q.6.1, which safety factor do you use to represent low dose rate effects? | | | |
| CMO | CMOS and BiCMOS only: | | | |
| 6.5 | Did you perform post-irradiation aging to simulate | Y | | |
| | low dose rate effects (Y/N)? | | | |
| 6.6 | If "no" to Q.6.5, which safety factor do you use to represent low dose rate effects? | | | |

7. Thermal and voltage stresses:

| During irradiation: | | | | |
|---------------------|--|----------------------------------|--|--|
| 7.1 | Temperature (°C) ? | 25 °C | | |
| 7.2 | Supply voltage (Y/N) ? | Y | | |
| 7.3 | If "yes" to 7.2, value of supply voltage: | 3.3 V | | |
| 7.4 | AC operation (Y/N) ? | Y | | |
| 7.5 | If "yes" to 7.4, which AC operation? Normal Opera | tion with clock and PLL running. | | |
| 7.6 | If "yes" to 7.4, which frequency? | 40 MHz | | |
| Duri | ng post irradiation annealing: | | | |
| 7.7 | Did you perform post-irradiation annealing (Y/N) ? | Υ | | |
| 7.8 | If "yes" to 7.7, annealing temperature (°C)? | 25 °C | | |
| 7.9 | If "yes" to 7.7, duration? | 168 hour | | |
| 7.10 | If "yes" to 7.7, supply voltage (Y/N) ? | Y | | |
| 7.11 | If "yes" to 7.7 and 7.10, which supply voltage? | Vdd (3.3V) | | |
| 7.12 | If "yes" to 7.7, AC operation (Y/N) ? | Ν | | |
| 7.13 | | | | |
| 7.14 | If "yes" to 7.7 and 7.12, which AC frequency? | | | |
| Duri | ng post irradiation accelerated aging: | | | |
| 7.15 | Did you perform post-irradiation ageing (Y/N) ? | Y | | |
| 7.16 | If "yes" to 7.15, aging temperature (°C)? | 100 °C | | |
| 7.17 | | | | |
| 7.18 | 8 If "yes" to 7.15, supply voltage (Y/N) ? Y | | | |
| 7.19 | | | | |
| 7.20 | | | | |
| 7.21 | If "yes" to 7.15 and 7.20, which AC operation? | | | |
| 7.22 | If "yes" to 7.15 and 7.20, which AC frequency? | | | |

8. Electrical measurement:

| During irradiation: | | | | | | |
|---------------------|---|-------|--|--|--|--|
| 8.1 | Did you perform on-line measurement (Y/N) ?Y | | | | | |
| 8.2 | If "yes" to 8.1, at which temperature (°C) ? | 25 °C | | | | |
| Voltag | 8.3 If "yes" to 8.1, describe on-beam operation and measurements: Voltage and Current measurement for both static (clock is stopped and PLL, LVDS drivers and receivers are disabled) and dynamic (40MHz clock is supplied, PLL is running at 80MHz, and LVDS driver and receivers are operated) state. | | | | | |
| After | r irradiation: | | | | | |
| 8.4 | Did you perform electrical measurements just after irradiation (Y/N) ? | Y | | | | |
| 8.5 | Duration between irradiation and electrical measurement? | 5 min | | | | |
| 8.6 | Temperature during electrical measurement (°C) ?25 °C | | | | | |
| After | r annealing: | | | | | |
| 8.7 | Did you perform electrical measurements after annealing (Y/N)? | Y | | | | |
| 8.8 | Duration between annealing and electrical measurement? 1 hours | | | | | |
| 8.9 | Temperature during electrical measurements?25 °C | | | | | |

8. Electrical measurement (cont.):

| After | After accelerated aging: | | | | | |
|-------|---|---------|--|--|--|--|
| 8.10 | Did you perform electrical measurements after aging (Y/N) ? Y | | | | | |
| 8.11 | Duration between aging and electrical measurement? | 3 hours | | | | |
| 8.12 | 2 Temperature during electrical measurement (°C) ? 25 °C | | | | | |
| Measu | Description of off-line measurements (after irradiation; after annealing or after aging): Measure Time resolution, CSR read/write verification, BIST(Built-In Self Test: Internal memory test), frequency of system clock generated by a PLL, maximum frequency of a ring oscillator. | | | | | |

9. Rejection criteria:

| | Measured parameter | Rejection Criteria | |
|-----|--|--------------------|--|
| 9.1 | Time Resolution | < 600 ps | |
| 9.2 | CSR and BIST | No Error | |
| 9.3 | Frequency of System Clock | 40 MHz +- 0.4 MHz | |
| 9.4 | Maximum Frequency of a ring oscillator | >70 MHz | |
| 9.5 | | | |

10. Results:

| | 10.1 | 10.2 | 10.3 | 10.4 | 10.5 | 10.6 |
|----|--------------------------|------|--------------------|-----------|---------|--|
| | Serial | Max. | Failure dose | Failure | Failure | |
| | number of | | (Gy) if any | during | during | Failure mechanism (if any): |
| | the device under test | | failure | annealing | ageing | for component "dead" or out of specification, give explanations and numbers |
| | under test | (Gy) | during irradiation | (Y/N)? | (Y/N)? | give explanations and numbers |
| 1 | А | 200 | intudiation | Ν | Ν | |
| 2 | D | 200 | | N | Ν | |
| 3 | Е | 200 | | Ν | Ν | |
| 4 | F | 200 | | Ν | Ν | |
| 5 | Н | 200 | | Ν | Ν | |
| 6 | J | 200 | | Ν | Ν | |
| 7 | K | 200 | | Ν | Ν | |
| 8 | L | 200 | | Ν | Ν | |
| 9 | М | 200 | | Ν | Ν | |
| 10 | Р | 200 | | N | Ν | |
| 11 | | | | | | |
| 12 | | | | | | |
| 13 | | | | | | |
| 14 | | | | | | |
| 15 | | | | | | |
| 16 | | | | | | |
| 17 | | | | | | |
| 18 | | | | | | |
| 19 | | | | | | |
| 20 | | | | | | |

11. Comments

Use the space below to comment test results, or to report them if the above-dedicated space is inappropriate for you.

12. Guidelines

12.1 Type and Function

| Туре | Function | | |
|------------------------------|---|--|--|
| Analogue device | ADC; Analogue memory; Analogue multiplexor; DAC; LVDS driver; | | |
| | LVDS receiver; Modulator/Demodulator; Voltage/Frequency converter | | |
| Data transmission Component | Receiver; Transceiver; Transmitter | | |
| Front-end electronic device | Drift Time Measurement; Multiple functions; Readout memory | | |
| Linear device | Amplifier; Comparator; Operational amplifier; Voltage reference; | | |
| Memory | SRAM | | |
| Microprocessor or peripheral | Microcontroller; Microprocessor | | |
| Optoelectronic component | Laser; Light emitting diode – LED; PIN diode; VCSEL | | |
| Power device | DC-DC converter; Power transistor; Voltage regulator | | |
| Programmable device | EEPROM; FPGA; Lookup table; Programmable delay | | |
| Passive component | Capacitor | | |
| Interfaces/Communication | LVDS; Switch | | |
| Mixed A/D device | Multiple functions | | |
| Logic gates | NOR, NAND, etc. | | |

12.2 Radiation source and type

| Source of radiation | Type of radiation |
|---------------------|---|
| Accelerator | Electron, proton, spallation neutron |
| Am-241 | Ions (fission products) |
| Cf-252 | Ions (fission products) |
| Co-60 | Photon gamma 1.173 MeV and 1.332 MeV |
| Cs-137 | Photon gamma 0.662 MeV |
| Cyclotron | Proton, ion (specify), spallation neutron |
| Reactor | Neutron |
| Tandem accelerator | Protons, ions |
| Van-de-Graaf | Electron |
| X-Ray generator | Photon X |

12.3 Radiation test methods:

see ATLAS Policy on Radiation Tolerant Electronics rev. 2, pp. 20-26 http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/ATLASPolicy/APRTE_rev2_250800.pdf

12.4 Low dose rate effects:

see ATLAS Policy on Radiation Tolerant Electronics rev. 2, pp. 11 http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/ATLASPolicy/APRTE_rev2_250800.pdf