AMT-2 TID Test Report

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1. Introduction

AMT chip is a front-end TDC chip used for the readout of drift time of the MDT. It must have adequate radiation tolerance to use in ATLAS environment. Actual Radiation Tolerance Criteria (RTC) is calculated from Simulated Radiation Level (SRL) with following equations.

RTC = SRL•SFsim•SFldr•SFlot

Here,

SFsim : Represents safety factor for SRL inaccuracies.
SFldr : Represents safety factor for low dose rate effects.
SFlot : Represents safety factor for the variation of radiation tolerance from lot to lot and within a lot.

SFlot for the pre-selection of COTS will be '2' if the final chips are produced in homogeneous batches. If the batches of the chip is unknown, we must use SFlot = ４. Although it is not impossible to request homogeneous batch to the fabrication company, the cost of chip will be increased. Since the radiation level is not so high in our case, we use SFlot = ４.

Gamma Irradiation test was done on April 4-5, 2002 at RI facility of the Tokyo Metropolitan University. We followed the test method shown in the reference [1]. Especially we used "Extended TID test method for the pre-selection of CMOS devices (section 2.1.1 Appendix 2), so we can use SFldr = '1' since accelerated aging tests at elevated temperature are done.

Simulated Radiation Levels for total ionizing doze (SRLtid) is 0.75 Gray/year for worst location MDT (Endcap 2) at 10^{34} luminosity [1], and SFsim is '3.5'. Thus maximum value of the RTCtid for 10 years operation is;

(RTCtid)max = 0.75 (Gray) x 3.5 x 1 x 4 x 10 (years) = 105 Gray = 10.5 krad

Although the (RTCtid)max is 10.5 krad、we irradiated the AMT chip up to 20 krad(Si) to get additional safety factor.

2. Method of Extended TID Test

Procedure of the extended TID test we followed is shown below;

a/ Selection of a calibrated ionizing dose facility.
We used 'Gamma Cell 220'(Fig. 1), which was installed with 12,000 Ci of ^{60}Co on May 1991.
b/ We selected a set of 11 good devices for test made on components from homogeneous lot.
c/ Serialization of all devices.
d/ Electrical measurements on each device at room temperature.
e/ Random selection of 1 component among the set of 11 devices. This component will not be irradiated; it will constitute the pre-radiation reference(s).
f/ Irradiation of the 10 other components at room temperature under bias in one-step up to the 20 krad.
g/ Electrical measurements at room temperature within 1 hour after the end of each dose step; rejection of the generic component if one of the 10 (or 20) components fails.
h/ After the last irradiation step, annealing under bias (168 hours at room temperature) plus electrical measurements (room temperature) at 24 hours and 168 hours; rejection of the generic component if one of the 10 components fails.
i/ Accelerated ageing under bias (168 hours at 100 ˚C).
j/ Electrical measurements at room temperature; rejection of the generic component if one of the 10 components fails.

Fig. 1 Photograph of Gamma Cell 220 at Tokyo Metropolitan University. Irradiation chamber is opened and irradiation board of the AMT-2 is located inside. The chamber will go down during irradiation.

3. Estimation of Dose Rate

Dose rate of the Gamma Cell was measured with Fricke Radiation Meter (0.8 N $FeSo_4$) on March 30, 1995 as 6.65 x 10^5 ± 0.5% [rads/hour] at the center of the sample chamber. Dose rate on April 4, 2002 is calculated from following equations.

At first decrease of source intensity is,

$I_1 / I_0 = (1/2)^{**}(T/T_{1/2})$ ($T_{1/2}$ = 1921 day, half-life of ^{60}Co)

$= 0.3968$ (@T=2562 day, April 4, 2002)

I_0 is the intensity at the calibration and I_1 is the intensity at the iradiation.

Absorbed dose of Silicon (D_{abs}^{Si}) is related to the absorbed dose (D_{abs}^{0}) of $FeSO_4$ as follows,

$$D_{abs}^{Si} / D_{abs}^{0} = (Z/Aw)_s / (Z/Aw)_0 = 0.498 / 0.553 = 0.901$$

Here Z is sum of atomic number constituting the molecular and Aw is the molecular weight.

Distribution of gamma intensity around chip location is almost flat within ±5%, and attenuation with

package, printed circuit board etc. are estimated as 10%. We neglected "Dose Enhancement" effect which will be less than 10%.

Thus we get dose rate of Si (R_{Si}) as、

$$R_{si} = (I_1 / I_0) \times (D_{abs}^{Si} / D_{abs}^{0}) \times 0.9 \times (6.65 \times 10^5) \text{ [rad/hour]}$$

$$= 2.14 \times 10^5 \text{ [rad/hour]}$$

$$= 59.4 \text{ [rad/sec]} \text{ (@ April 4, 2002)}$$

It takes 337 sec to irradiate the chip up to 20krad.

4. Irradiation and Measurement Setup

Fig. 2 shows setup during irradiation. Power, clock, reset, JTAG signals, and a control signal are connected to a irradiation board from a VME module. Power (Vdd=3.3V) was applied during the irradiation, and both static and dynamic current were measured at every 10 sec.

For static current measurement, clock was stopped and all LVDS receives and drivers were disabled and DC current path in the PLL was cut. After a short period of the static current measurement, the chip was operated in normal state and the dynamic current was measured, wherer 40 MHz clock was feed to the AMT-2 and PLL and all LVDS receives and drivers are enabled.

After the irradiation, the irradiated chip was moved from the irradiation board to an AMT-2 sub board (Fig. 3). Then following items were measured.

(i)Time resolution measurement

A simple time measurement was done by using two pulses generated from external clock. These pulses are injected into two channels and time difference was measured 100 times, and RMS value of the measurement was calculated.

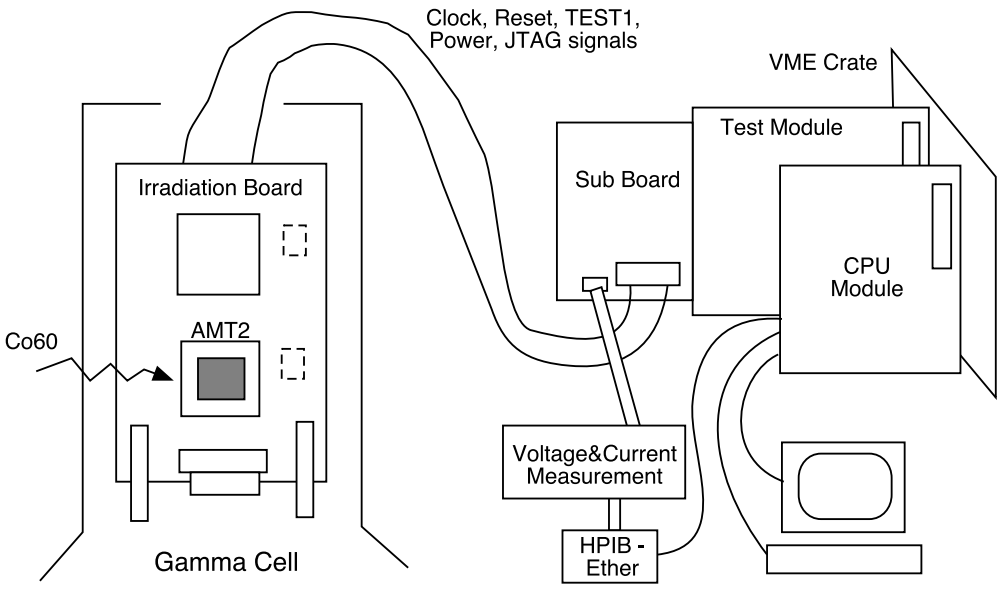

Fig. 2 Irradiation set up with on-line current measurement.

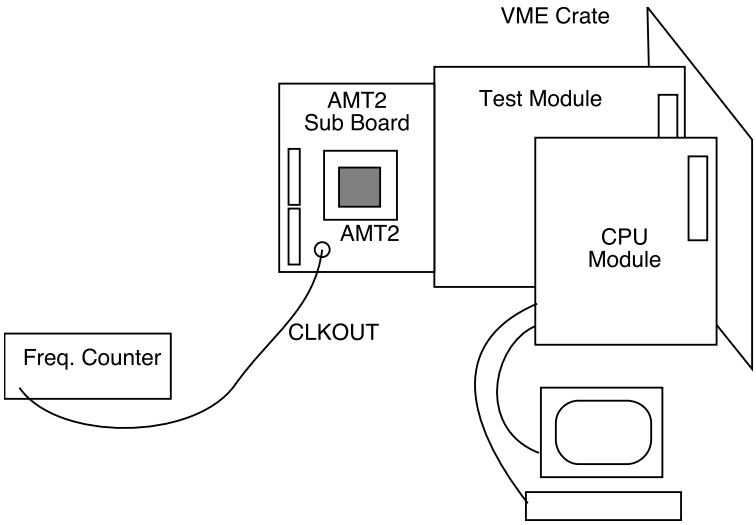

Fig. 3 Measurement setup after Irradiation.

(ii)Oscillating frequency of the ring oscillator.

Oscillating frequency of the ring oscillator after a 'divide by 2 counter' was measured at 2 points.

(a) Normal condition: The frequency should be around 40 MHz and this will be the measure of correct functionality of the PLL circuit.

(b) Maximum frequency: control voltage of the oscillator was forced to 3.3 V, so the oscillator will oscillate at maximum frequency. This will be a measure of internal gate delay.

(iii)CSRread/write verification

'0's and '1's are written to the CSR registers and read back through JTAG line.

(iv)BIST(Built In Self Test) memory test

BIST logic was activated through JTAG. All internal memories (L1 bufer, readout FIFO, and Trigger FIFO)were tested with 13N marching pattern.

5. Test results

5.1 Current Measurement

Static and dynamic currents were measured during irradiation and results are shown in Fig. 4. There was no variation observed during whole experiment.

For your reference, we show a result of a leakage current (static current) in Fig. 5 measured last summer. The AMT-2 chip was irradiated up to 230 krad. Since the leakage current start to increase above 40 krad, It is natural that we cannot see the leakage current increase in present experiment.

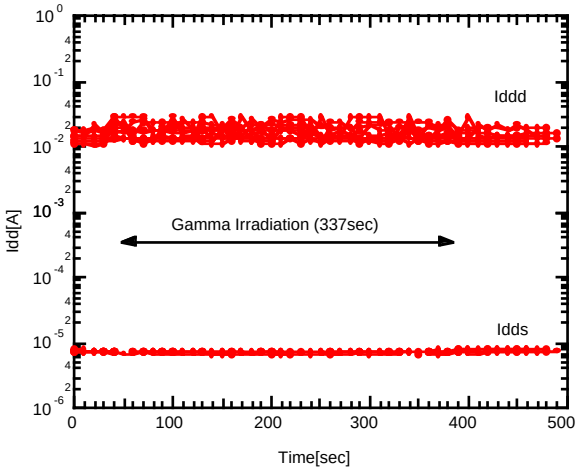

Fig. 4 Variation of static (Idds) and dynamic (Iddd) currents during irradiation. 10 irradiated chip and 1 non_irradiated chip are plotted

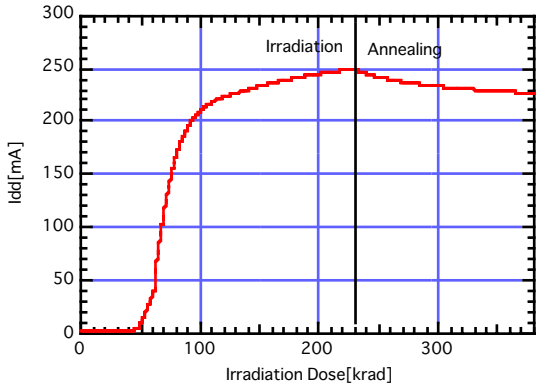

Fig. 5 Leak Current of AMT-2 (measured on Aug. 2001).

5.2 Time Resolution measurement

Result of the time measurement is shown in Fig. 6. We have not seen any degradation of the resolution during the experiment.

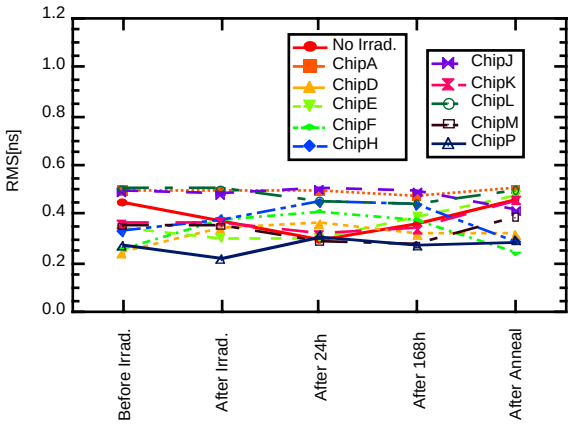

Fig. 6 Time difference measurement of two pulses for 'before irradiation', 'after irradiation', "after 24 hours at room temperature', 'after 168 hours at room temperature', and 'after 168 hours at 100 ˚C' annealing'.

5.3 PLL frequency

Fig. 7 shows variation of the 'PLL frequency / 2' and the 'Maximum frequncy / 2' for each measurement stages. There is no apparent change obeserved.

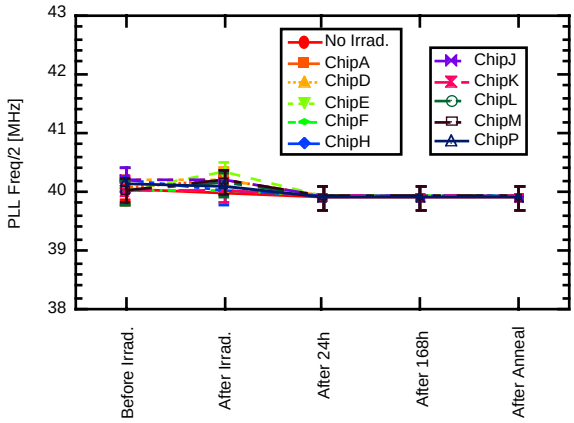

Fig. 7 Frequency variation of PLL clock generated from the PLL.

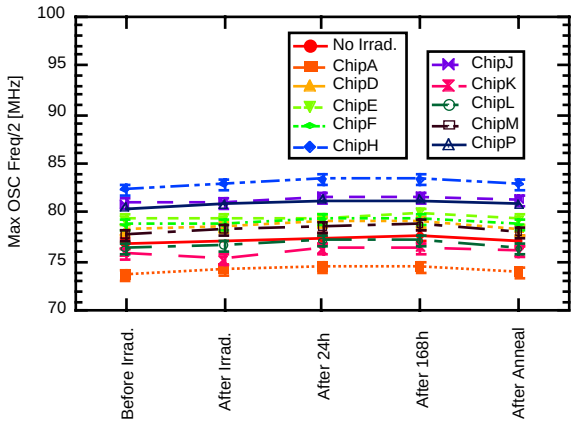

Fig. 8 Maximum frequency variation of the ring oscillator.

5.4 CSR and BIST Test

There was no error in the CSR and BIST test during the whole experiment.

6. Summary

We have done TID test to the AMT-2 according to the ATLAS standard test method. 10 AMT-2 chips were irradiated up to 20 krad. After annealing in room temperature for 168 hours, the chip was annealed at 100 ˚C for another 168 hours. Leakage current, time resolution, oscillating frequency and register and memory check were done, and we have not seen any damage in the AMT-2 chip. Therefore the AMT-2 has adequate TID tolerance for use in the MDT detector.

References

[1] "ATLAS Policy on Radiation Tolerant Electronics", ATC-TE-QA-0001, July 2001, and ATLAS Radiation Tolerance Criteria (Rev 2). Radiation tables were revised on Nov. 2001. http://www.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm