AMT-2 SEE Test Report

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1. Introduction

AMT chip is a front-end TDC chip used for the readout of drift time of the MDT. The chip contains both analog (PLL) and digital circuit, and must have adequate immunity to the Single Event Effect (SEE) caused by energetic hadrons.

To measure the SEE rates of the AMT-2 chip, proton irradiation experiment was done on May 16-18, 2002 at the Cyclotron and Radioisotope Center of Tohoku University. Maximum energy of the AVF cyclotron is 90 MeV for proton beam, and 70 MeV proton beam was used in this experiment.

We followed the test method shown in the reference [1] as much as possible. The 70 MeV proton beam is adequate to measure soft SEE rate, although proton beam energy of greater than 500 MeV is recommended to measure hard and destructive SEEs. Criteria for these SEEs are described below.

1.1 Soft SEE

Soft SEEs (also called soft SEUs) are phenomena of radiation induced bit flip (non-permanent). Soft SEUs rate can be calculated as follows;

$$\text{Soft SEUf} = (\text{Soft SEUm} / \text{ARL}) \times (\text{SRLsee} / 10^8\ \text{s}) \times \text{SFsim}$$

Where,

"Soft SEUf" is the foreseen rate of soft SEU in a given location.

"Soft SEUm" is the total number of soft SEU measured in proton beam tests.

"ARL" is the Applied Radiation Level.

"SRLsee" is the simulated Radiation Level in 10 years.

"SFsim" is the safety factor of the simulation, and is '5'.

Maximum value of the SRLsee is seen in Endcap 1 region and is 8.31 x 10^9 h/cm^2/y (for hadrons energy > 21 MeV) [1]. Average value of the SRLsee weight by number of channels in each position is 2 x 10^9 h/cm^2/y.

Soft SEEf rates must be lower than the corresponding radiation tolerance criterion (RTCsee.s).

$$\text{Soft SEUf} < \text{RTCsee.s}$$

(There is no defined value of RTCsee.s yet in MDT sub group)

1.2 Hard and Destructive SEE

Hard SEEs are phenomena of radiation induced permanent bit flip. Destructive SEEs produces permanent short circuits. One of the destructive effects in CMOS is the latch-up of the device.

Unfortunately, no study has been done to estimate the rates of hard or destructive SEEs in accelerator environment. The estimation of the rates of hard SEUs and destructive SEEs in a given ATLAS location can be done as follow [1].

$$\text{Hard or destructive SEEf} = (\text{hard or destructive SEUm/ARL}) \times (\text{SRLsee}/10^8\text{s}) \times \text{SFsim}$$

Where:

"Hard or destructive SEUf" is the foreseen rate of hard or destructive SEU in a given location.

"Hard or destructive SEUm" is the total number of hard or destructive SEU measured in proton beam tests.

The rates of the hard SEUs or the destructive SEEs foreseen for each ATLAS electronic component in a given location must be lower than the corresponding radiation tolerance criterion:

Hard SEUf < RTCsee.h

Destructive SEUf < RTCsee.d

(There is no defined value of RTCsee.h and RTCsee.d yet in MDT sub group)

2. Experimental Procedure

2.1 Beam-line setup

Proton beam was extracted through a Ti foil of 20 mmϕ and 100 μm thickness into air and irradiated to the AMT-2 chip. A photograph of the experiment setup is shown in Fig. 1 and Fig. 2, and block diagram of a measurement setup is shown in Fig. 3. Target board and ZnS fluoresce screen were mounted on a X-Y stage. Beam position was first monitored by the fluorescence screen and then target board was moved to the beam position. Actual beam profile and beam intensity were measured with dosimetry of a 100 μm thick Cu foil placed in front of the AMT-2 chip.

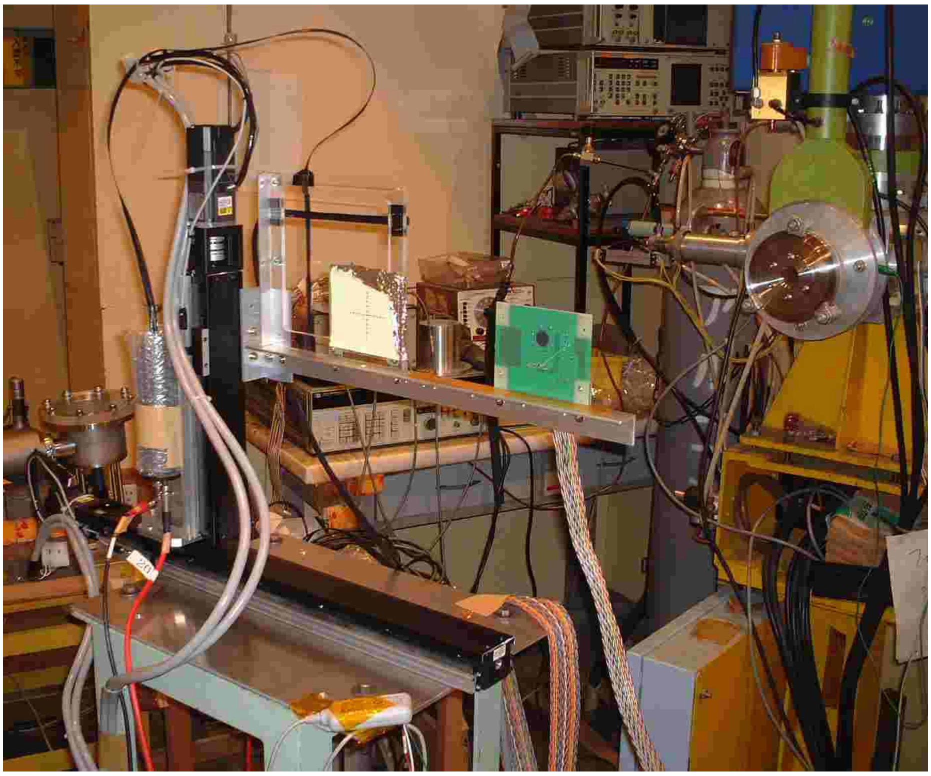


Fig. 1 Photograph of the experimental setup in the beam line. X-Y stage is seen in the center and the beam pipe end is seen at the right side.

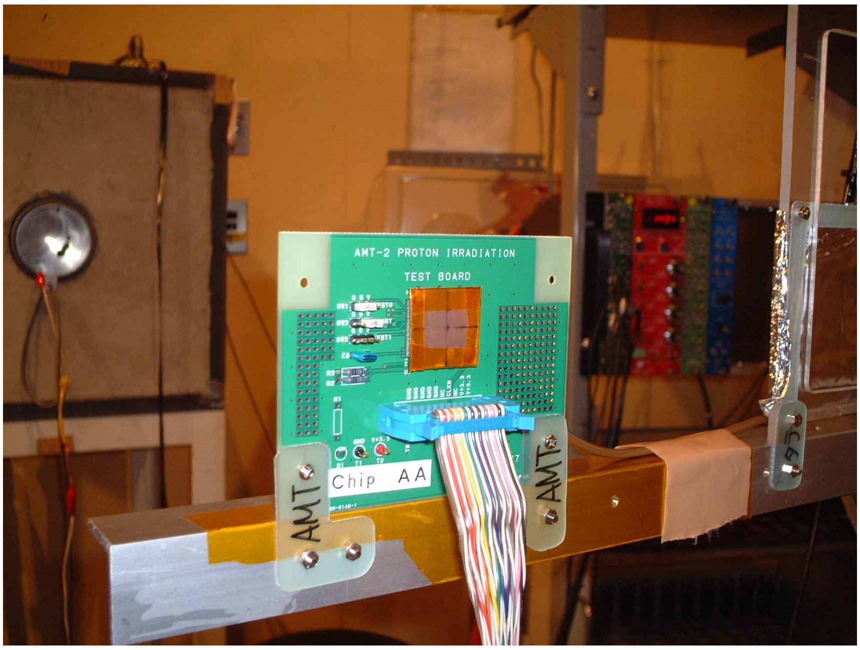


Fig. 2 Photograph of the front side of the target board. A Cu foil was attached in front of the AMT-2 chip.

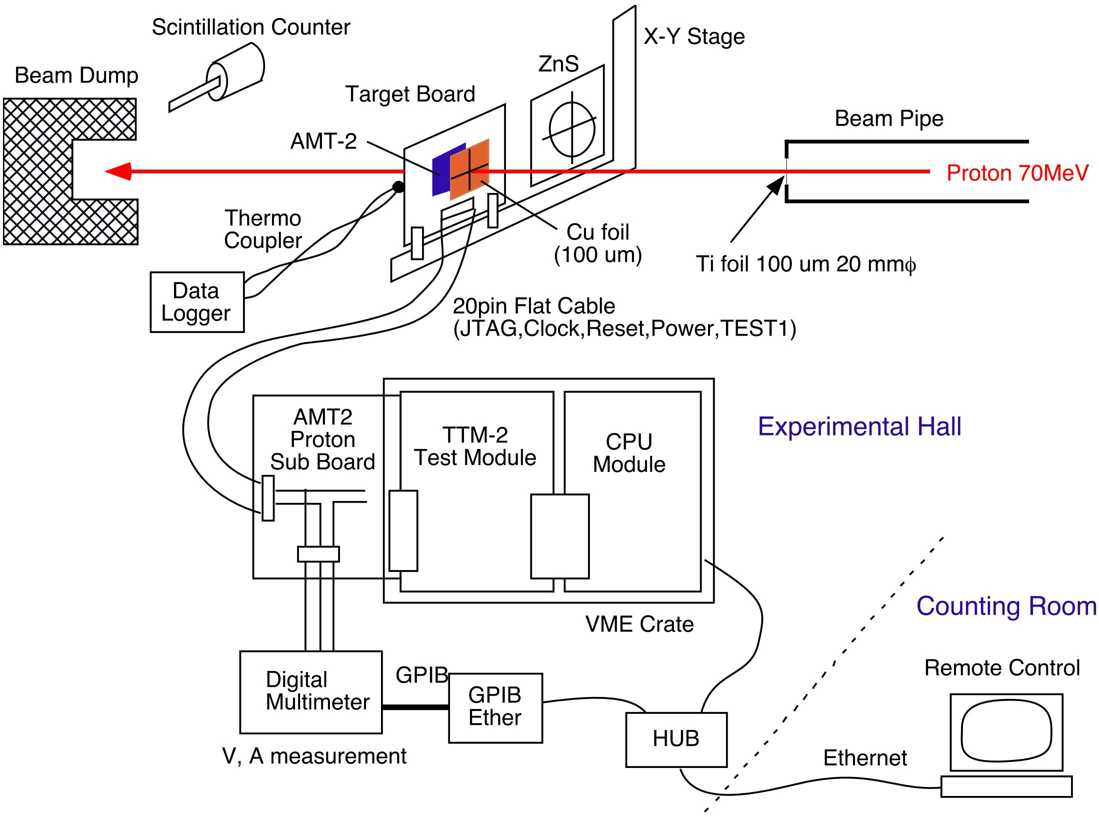


Fig. 3 Measurement setup of the SEE test.

The target board is connected with a 20 signals flat cable which includes power/ground, clock, reset, control and JTAG lines. This flat cable was connected to a VME module and controlled through a VME CPU module. Voltage and current to the target board were monitored with a digital voltage meter and recorded in the CPU module. Then the CPU module was remotely controlled from a counting room.

The beam intensity at a final beam stopper was around 2 nA. The beam was broadened and the size is defined with the 20 mmϕ Ti foil.

2.2 Memory Test

AMT-2 has 180 bits in the CSR registers, and a total of 11,360 bits in a L1, a trigger and a readout buffers (Fig. 4). The CSR register was composed of Flip-Flops, and the buffer memories are composed of 6 transistors static memory cells. Both circuits is complimentary for positive and negative logic signals, so we expect no difference between '0' to '1' and '1' to '0' transition rates of SEU.

Although we cannot directly read and write the contents of the buffers, we can use Built-in Self-Test (BIST) circuit to detect the SEU. The BIST circuit performs two kinds of 13N marching pattern test. The results are compressed in a 36-bit Linear Feedback Shift Register. If one or more error occurs in this test sequence, final result has different value.

Detailed sequence of the 13 N marching pattern test is shown in Fig. 5. We step forward the BIST sequence until state A or B in alternate cycle. At state A, contents of even addresses of memories are '0's and odd addresses are '1's. At state B, all memories have '1's. Then irradiate the chip to the beam for 11 sec. After the irradiation, we continue the BIST sequence and read out the final value. These measurements were repeated several times.

As for the CSR, the contents are directly written and read through JTAG lines. Before the irradiation, '0's and '1's were written to the CSRs, then after the irradiation the contents were checked for SEU.

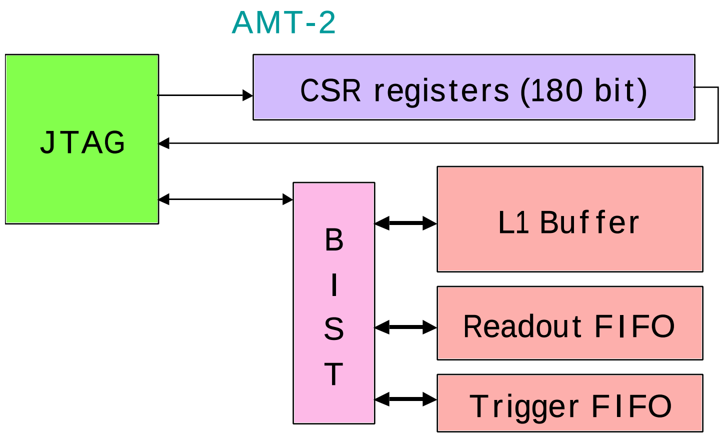
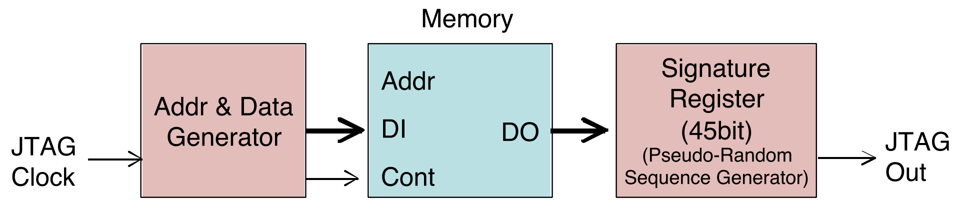


Fig. 4 CSR's and Buffers of the AMT-2.



13N Marching Pattern ('10' & '11' Backgrounds)

Addr.	Initialize	1st Step	2nd Step	3rd Step	4th Step
0	W(1)	R(1)W(0)R(0)	R(0)W(1)R(1)	R(1)W(0)R(0)	R(0)W(1)R(1)
1	W(0)	R(0)W(1)R(1)	R(1)W(0)R(0)	R(0)W(1)R(1)	R(1)W(0)R(0)
2	W(1)	R(1)W(0)R(0)	R(0)W(1)R(1)	R(1)W(0)R(0)	R(0)W(0)R(1)
:	\	\	\	/	/
N-1	W(0)	R(0)W(1)R(1)	R(1)W(0)R(0)	R(0)W(1)R(1)	R(1)W(0)R(0)

Pause A

Addr.	Initialize	1st Step	2nd Step	3rd Step	4th Step
0	W(1)	R(1)W(0)R(0)	R(0)W(1)R(1)	R(1)W(0)R(0)	R(0)W(1)R(1)
1	W(1)	R(1)W(0)R(0)	R(0)W(1)R(1)	R(1)W(0)R(0)	R(0)W(1)R(1)
2	W(1)	R(1)W(0)R(0)	R(0)W(1)R(1)	R(1)W(0)R(0)	R(0)W(1)R(1)
:	\	\	\	/	/
N-1	W(1)	R(1)W(0)R(0)	R(0)W(1)R(1)	R(1)W(0)R(0)	R(0)W(1)R(1)

Pause B

Fig. 5 BIST sequence (13N marching pattern).

2.3 Test Sequence

Whole test sequence is shown in Fig. 6. After measuring a static current (Idds), all CSR registers were set to \$aaa. Then front part of BIST sequence was done. After 11 sec of irradiation, rear part of the BIST sequence was done and contents of CSR registers were verified. Then dynamic state current was measured and go back to the first state. This sequence was continued about 40 min. The beam was always on during this sequence.

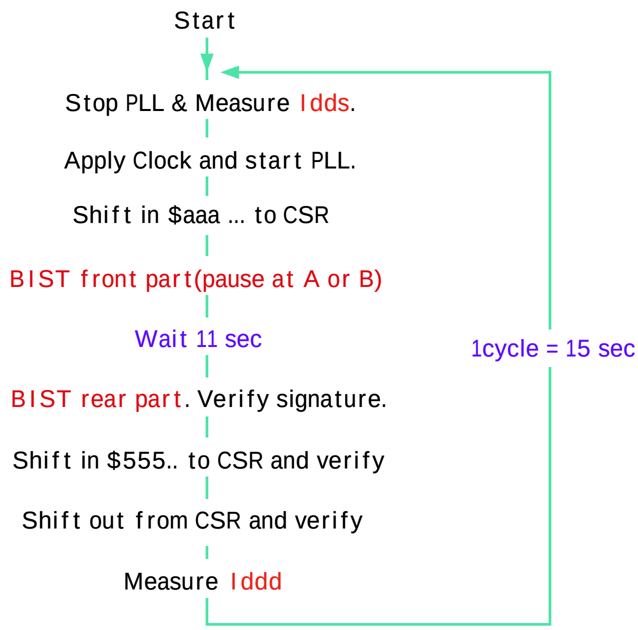
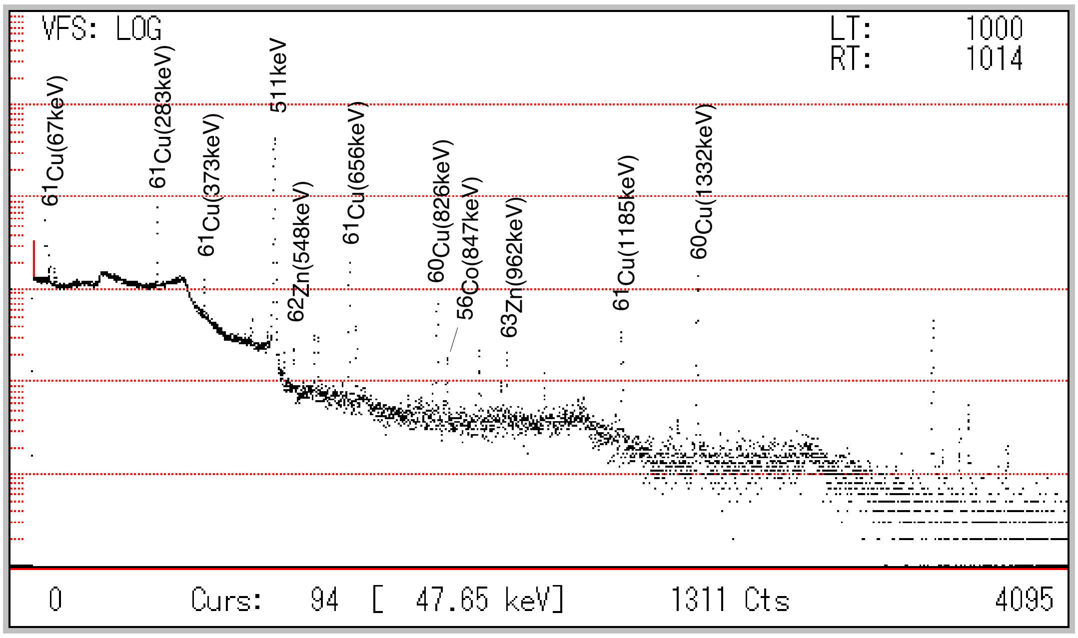


Fig. 6 Test sequence during irradiation.

2.4 Dosimetry

To measure the proton fluence, dosimetry of a Cu foil was done. Thickness of the Cu foil is 0.1 mm and its purity is 99.99+%. The size of the Cu foil is 25 mm by 25 mm and attached in front of the chip. After 1 hour from the end of irradiation, gamma-ray spectrum was measured for 1,000 sec with a Ge detector. An example of the spectrum is shown in Fig. 7.

Intensity distribution of each foil is measured with Imaging Plate and also surveyed with a GM detector through a 5 mmϕ Pb collimator. An example of the contour is shown in Fig. 8. The intensity is relatively flat in central 20 mmϕ area.



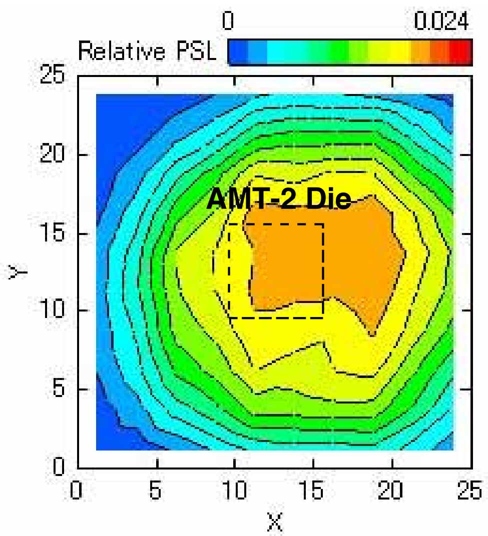


Fig. 8 Contour plot of the Cu foil measured with an imaging plate.

2.5 Temperature, Current and Beam Monitor

Temperature of the chip was measured from rear side with a thermo coupler. The output of scintillation counter was also monitored to see the beam status. These outputs are continuously measured with a data logger. An example of the measurements is shown in Fig. 9. The temperature of the chip increased from 24 ˚C to 34˚C during the irradiation.

We show the measurement of the static current (Idds) in Fig. 10. We can see the increase of temperature is related to the increase of the static current. For your reference, we show the result of Idds measurement with gamma-ray irradiation in Fig. 11. To have a 200 mA static current seen in the present experiment, about 100 krad absorbed dose is required.

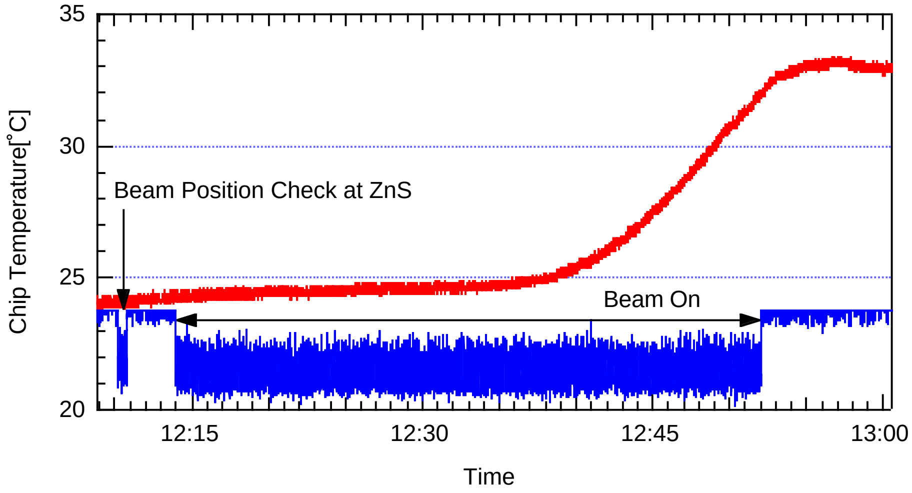


Fig. 9 An example of chip temperature variation (upper curve) and beam on/off monitor (lower curve).

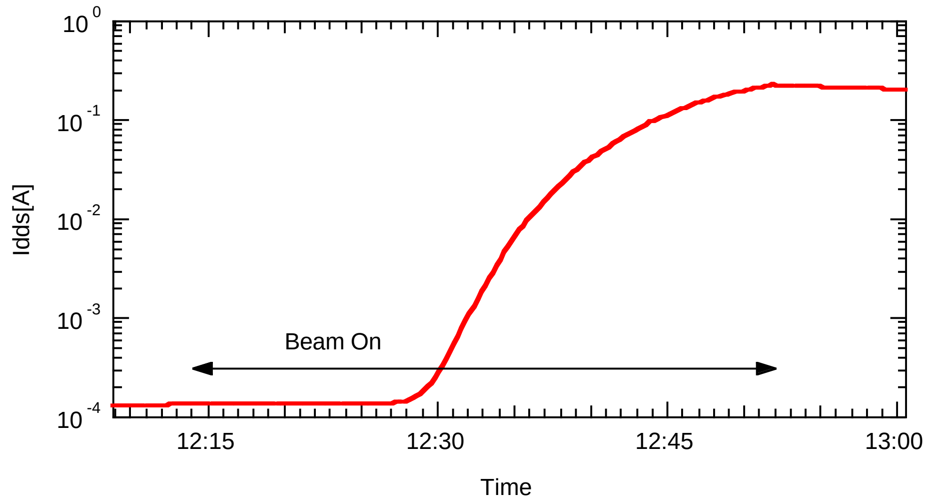


Fig. 10 AMT-2 Leak Current (Idds) variation during irradiation.

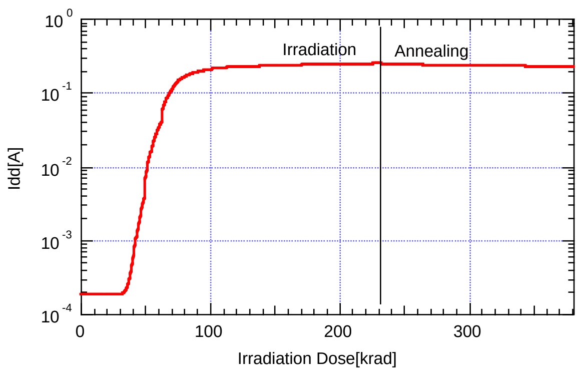


Fig. 11 Leakage current measurement at gamma-ray irradiation.

3. Test Results

3.1 Estimation of Proton Fluence

Proton fluence was measured with a dosimetry of a Cu foil. We would like to show you equations to get the fluence below. Production rate of a nuclear reaction can be shown as follows,

$$\frac{dN}{dt} = \phi \bullet \sigma_{eff} \bullet Nt - \lambda \bullet N$$

Here N is the number of production nuclei, ϕ is the incident beam flux, Nt is a number of target nuclei, σ_{eff} is an effective reaction cross section, and λ is a decay constant (= ln 2 / $T_{1/2}$). By integrating above equation, we get

$$N = \frac{\phi \bullet \sigma_{eff} \bullet Nt}{\lambda}(1 - \exp(-\lambda \bullet Tr))$$

Here Tr is an irradiation time. Defining t=0 as the end time of the irradiation, radiation intensity at t B(t) is,

$$B(t) = \lambda \bullet N(t) = \lambda \bullet N \bullet \exp(-\lambda \cdot t)$$

Thus the number of gamma-rays ($C\gamma$) measured in a detector from time Tm to Tm+Tc is,

$$C_\gamma = Br \bullet \varepsilon \int_{Tm}^{Tm+Tc} B(t)dt$$
$$= Br \bullet \varepsilon \bullet N \bullet (\exp(-\lambda \bullet Tm) - \exp(-\lambda \bullet (Tm + Tc)))$$

where Br is the branching ratio of the gamma-ray and ε is the detection efficiency. From above equations, we can get proton flux as,

$$\phi = \frac{C\gamma \bullet \lambda}{\varepsilon \bullet Br \bullet \sigma_{eff} \bullet Nt(1 - \exp(-\lambda \bullet Tr)) \bullet (\exp(-\lambda \bullet Tm) - \exp(-\lambda(Tm + Tc)))}$$

Actual flux was corrected by take into account the distribution of beam intensity. We get proton flux at center region of ~3.7 x 10^8 protons/sec/cm^2. Fluence (F) of each chip is summarized in Table. 1.

Absorbed dose (X) is calculated from the equation below

X = dE/dx x F

= 1.6E-5 (erg/(g/cm^2)) x F [erg/g]

= 1.6E-7 x F [rad]

The results are also shown in the Table. 1 and these values agree with the values estimated from the leakage current (section 2.5).

Since the period of waiting a bit flip is 11 sec in 15 sec cycle, effective fluence (Feff) of the SEU test is 73% of the proton fluence. We have observed only 1 error in BIST test (in state A of Fig. 5). There was no error in CSR test. By using an upper limit of 90% confidence level, upper limit of the SEU cross sections are calculated from following equations.

σ_{SEU}(Mem) < 2.44 / Feff / 11360 [cm^2/bit] (for 0 SEU)

σ_{SEU}(Mem) < 4.36 / Feff / 11360 [cm^2/bit] (for 1 SEU)

σ_{SEU}(CSR) < 2.44 / Feff / 180 [cm^2/bit]

Table. 1 Summary of SEU test.

Chip	Proton Fluence ($1/cm^2$)	Effective Fluence for SEU ($1/cm^2$)	Radiation Dose (krad)	Latch up	No. of SEU in Mem	σ_{SEU}(Mem) (cm^2/bit)	No. of SEU in CSR	σ_{SEU}(CSR) (cm^2/bit)
AA	$8.10x10^{11}$	$5.94x10^{11}$	130	None	0	$< 3.6x10^{-16}$	0	$< 2.3x10^{-14}$
CC	$8.02x10^{11}$	$5.88x10^{11}$	128	None	1	$< 6.5x10^{-16}$	0	$< 2.3x10^{-14}$
DD	$8.03x10^{11}$	$5.89x10^{11}$	128	None	0	$< 3.6x10^{-16}$	0	$< 2.3x10^{-14}$
FF	$8.06x10^{11}$	$5.91x10^{11}$	129	None	0	$< 3.6x10^{-16}$	0	$< 2.3x10^{-14}$
Total	$3.22x10^{12}$	$2.36x10^{12}$		None	1	$< 1.6x10^{-16}$	0	$< 5.6x10^{-15}$

According to the Soft SEUs rate equation shown in the section 1.1 ,

$$\text{Soft SEUf} = (\text{Soft SEUm} / \text{ARL}) \times (\text{SRLsee} / 10^8 \text{ s}) \times \text{SFsim}$$

$$= (1 / 2.36\text{x}10^{12}) \times (2 \times 10^{10} / 10^8) \times 5$$

$$= 4.24 \times 10^{-10} \text{ [upset/sec/chip]}$$

Multiplying the total number of AMT chips (16,000) used in the MDT, we get

$$\text{Soft SEUf} = 6.8 \times 10^{-6} \text{ [upset/sec/MDT]}$$

This is negligibly small number. Furthermore, AMT chip has parity bits for memories and CSRs and can detect whether a parity error occurred or not. Thus we think there is no problem in AMT-2 chip as for the soft SEUs.

3.2 Latch-Up

During the proton beam test, we see no latch-up phenomena in the chip.

4. Summary

We have done SEE test to the AMT-2 chip with a 70MeV proton beam. We see only 1 upset for the 2.36 x 10^{11} proton irradiation. Foreseen Soft SEU rate is 6.8 x 10^{-6} [upset/sec/MDT], and no latch-up was observed. Therefore we think there is no SEE problem in AMT-2 to use in MDT.

References

[1] "ATLAS Policy on Radiation Tolerant Electronics", ATC-TE-QA-0001, July 2001, and ATLAS Radiation Tolerance Criteria (Rev 2). Radiation tables were revised on Nov. 2001.
http://www.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm