TDC Architecture Study for the ATLAS Muon Tracker

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Abstract

The architecture of a new TDC LSI has been studied for the ATLAS precision muon tracker. Intensive simulations have been performed using a Verilog simulator for various conditions. The final chip will be fabricated in a 0.35 μm CMOS technology. A verilog RTL level model for a prototype chip has been implemented. Radiation hardness tests using a one generation older process (0.5 μm) have also been done.

1. Introduction

High-resolution, low-power and low-cost TDC LSI's are required in the ATLAS precision muon tracker (MDT: Monitored Drift Tubes). There are about 350 k channels and the TDC must have a sub-nano second timing resolution to match the high resolution of the MDT.

High-resolution TDC chips using CMOS technology have been developed in several groups [1,2,3,4,5]. Common for these chips is the use of a chain of CMOS gates as a fine time measurement within a clock cycle and a clock synchronous counter as a coarse time measurement. This scheme prevents the use of very high-speed clocks in the circuit and results in a low power device (~10 mW/ch). The gate delay of CMOS devices normally have very large variations as function of process, voltage, and temperature. By using voltage controlled delay elements as a part of a Delay Locked Loop (DLL) or a Phase Locked Loop (PLL) a self-calibrating TDC which has a timing resolution of ~250 ps can be built.

Intensive simulations have been done to optimize the TDC architecture by using a Verilog simulator. To match the MDT granularity, 24 channels will be implemented in a chip. From the simulation, the present TDC architecture shows ~100% efficiency for 100 kHz hit rates per channel and a trigger rate of 100 kHz. Based on the simulation results done at behavioral level, a RTL (register transfer level) model has also developed.

In this paper, we show our present baseline architecture of the TDC. A more detailed description of the TDC can be found in ref. 6. Final production chips will be fabricated in 0.35 μm CMOS sea-of-gate technology. An evaluation chip in a 0.7 μm CMOS process is being designed using full custom layout for time critical circuits. Radiation hardness tests of an existing chip in an one generation older process (0.5 μm) has also been done and preliminary results are shown in section 4.

2. TDC Design

MDT front-end electronics

The MDT front-end electronics consists of 8 channels Amplifier/Shaper/Discriminator (ASD) chips [7] and a 24 channels TDC chip as shown in Fig. 1. The following information can be extracted from the MDT signal [8]:

• The **leading edge** time, giving the position of the track. The required time bin size for the leading edge measurement is 0.78 ns.

• The **trailing edge** time, corresponding to electrons from the tube wall, which has a fixed time relative to the bunch-crossing time. The trailing edge resolution is about 25 ns.

• The **charge** of leading edge which can be used for slewing correction. The integrated charge is converted into a pulse width using a Wilkinson type voltage-to-time converter within the ASD. A resolution of 8 bits is considered sufficient.

• **Multi-hit** information for two-track separation. A second discriminator on the output of the shaper using a higher threshold is used to obtain double track separation.

Measurements will be selected from one of the following three modes depending on experimental conditions: (1) leading and trailing edge, (2) leading edge and charge, (3) leading edge, charge, and second hit.

The MDT signal continues until the last electron, comming from near the tube wall, reaches the anode wire and a second track might be masked by the signal from the preceding track. Since all leading edge information is stored in the TDC, the existence of a preceding hit can also be detected.

TDC architecture

A block diagram of the proposed baseline architecture is shown in Fig. 2, and the main specifications are summarized in Table 1.

The hit signal coming from the ASD chip is used to store the fine time and coarse time measurement in individual channel buffers. The fine time measurement is obtained as a fine interpolation of the basic clock cycle using a chain of delay elements. The timing of both leading and trailing edge of the hit signal can be stored as a pair to enable a pulse width measurement to be performed.

The time measurements from the channel buffers are stored during the first level trigger latency in a common first level buffer. First level triggers converted into trigger

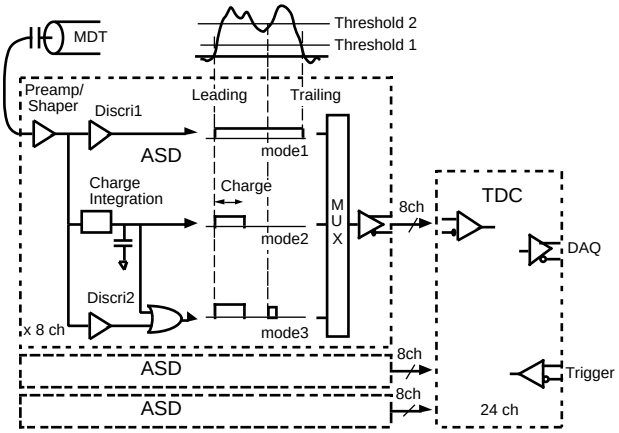

Fig. 1. MDT front-end electronics.

time tags and a corresponding event ID are stored temporarily in a trigger FIFO. Hits matching triggers are written into a readout FIFO waiting to be transferred to the DAQ system.

A fine time and a coarse time is only stored when a hit has been detected, thus the required memory size depends on the hit rate. One common buffer shared by many channels gives an effective use of memory, but it may introduce a significant dead time if not carefully designed. Our simulation shows the use of a small buffer (4 hits) per channel, before the L1 buffer, have removed this problem.

Time measurement part

To achieve a high resolution time measurement with sufficient stability, voltage-controlled delay elements, used as a part of a self calibrating feedback loop (PLL), will be used. The PLL produces a double frequency clock of 80 MHz from the LHC clock (40MHz). By dividing the 12.5 ns clock period into 16 intervals a time bin size of 0.78 ns is obtained.

The dynamic range of the fine time measurement is expanded by storing the state of a clock synchronous counter.

Table 1. ATLAS MDT TDC Specifications

Technology	0.35 μm CMOS sea-of-gate
Master gate size	~200 k gates
Number of channels	24 ch
Clock frequency	40 MHz
PLL frequency	80 MHz
Time bin size	0.78 ns
Time resolution	< 300 ps RMS
Dynamic range	17 bit
Double pulse resolution	<15 ns
Channel buffer	4 measurements
First level buffer	128 words x 31 bit
Readout FIFO	32 words x 28 bit
Trigger FIFO	8 words x 25 bit
Power supply	3.3 volt
Power consumption	~ 10 mW/channel
Signal input level	LVDS & CMOS level
Package	0.5 mm pitch, 144 pins QFP

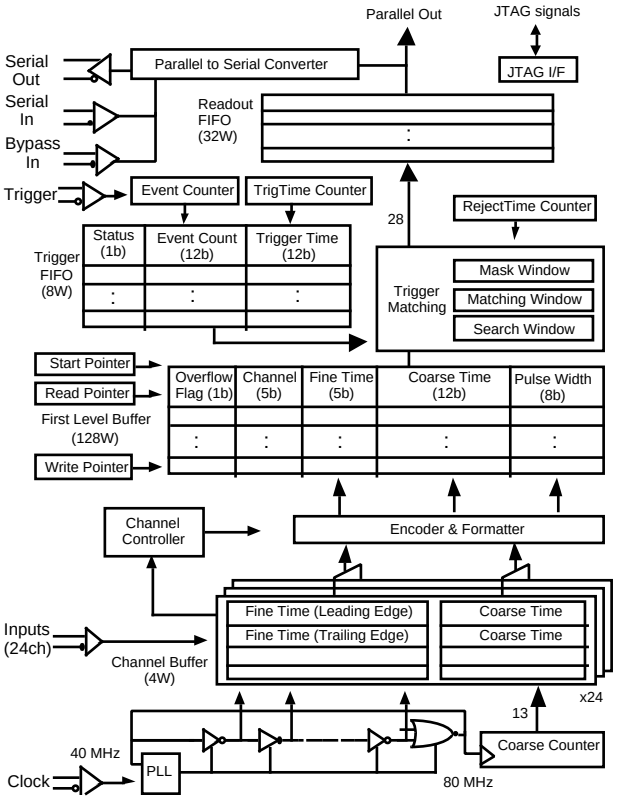

Fig. 2. Block diagram of the 24 ch TDC for the ATLAS MDT detector.

Channel buffer

Each channel has a 4 words deep buffer where measurements are stored until they can be written into the common first level buffer. The channel buffer is implemented as a FIFO.

The channel buffer must be controlled such that it is capable to measure the minimum pulse width of ~10 ns. To measure the pulse width of the hit signal, a time measurement pair consisting of a leading and a trailing edge is assembled.

First level buffer

The first level buffer is 128 hits deep and is written into like a circular buffer when a hit have been detected on a channel. Reading from the buffer is random access.

The layout of the first level buffer is optimized for having a complete leading edge measurement plus a reduced pulse width measurement per word. When performing a charge measurement the pulse width is stored as 8 bits with a resolution of 0.78 ns. In case of a trailing edge measurement the pulse with is stored with a 6.25 ns resolution to obtain the required dynamic range using a 8 bit representation.

When a hit has been detected on a channel the corresponding channel buffer is selected, the fine time measurement is encoded into binary form, and the complete time measurement is written into the first level buffer.

In case the first level buffer runs full, hit measurements from the channel buffers will be rejected. A special buffer

overflow detection scheme takes care of handling the buffer overflow condition and properly marking events which may have lost hits.

Trigger interface

A positive trigger is translated into a 12 bit trigger time tag and a 12 bit event ID. The trigger information is stored temporarily in a 8 words deep trigger FIFO to accommodate several triggers arriving within a short time interval.

In case the trigger FIFO runs full, triggers are rejected and complete events from the TDC are potentially lost. A full flag in the trigger FIFO together with the event number of the triggers are used to detect the loss of triggers.

Trigger matching

The trigger matching function selects the data related to the trigger from the first level buffer, and stores them into the read-out FIFO together with a header and a trailer.

A match between the trigger and a hit (leading edge) is detected within a programmable time window (matching window, Fig. 3) to accommodate the maximum drift time of the detector. All hits from this trigger time until the trigger time plus the matching window will be considered as matching the trigger.

A mask window before the trigger time is optionally checked to search for possible hits which may have masked a hit in the matching window. The masked hit information is written to the readout buffer as one single word with individual flags per channel.

The search for hits in the first level buffer, matching a trigger, can not be performed in a simple sequential manner. The hits are not guaranteed to be written into the first level buffer in strict temporal order. In addition a hit may belong to several closely spaced triggers. A fast and efficient search mechanism which takes these facts into consideration is implemented using a set of memory pointers and a set of programmable time windows;

To prevent the first level buffer to overflow, when no triggers have occurred for extended periods of time, hits are automatically rejected from the buffer when getting older than a programmable reject limit.

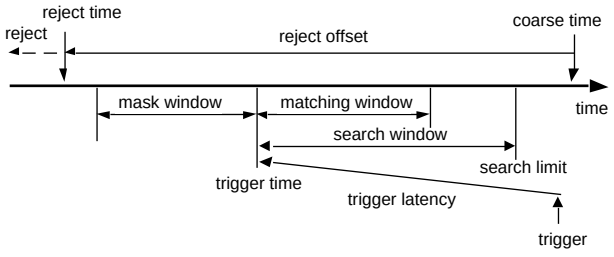

Fig. 3. Time relations of trigger matching and data rejection.

Signal connections

The TDC chip is mounted on a small board together with the ASD chips to avoid large number of cables between them. This front-end board will be located inside the detector directly at the ends of the MDT tubes.

It is important that noise from digital signals on the front-end board is kept to an absolute minimum so the small analog signal from the tubes are not corrupted. Low Voltage Differential Signaling (LVDS) [9] will be used for all connections to/from the TDC which are actively running while taking data.

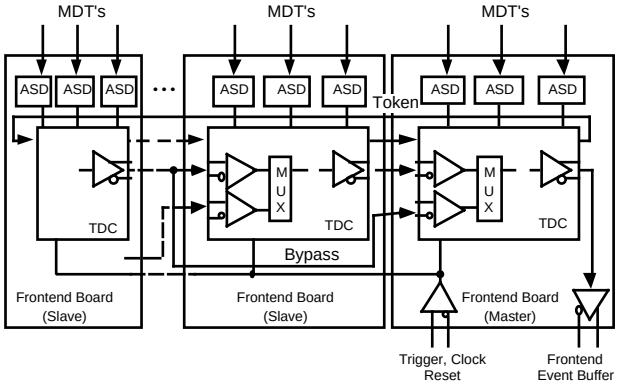

Fig. 4. TDC Readout in daisy chain connection with a bypass option.

Data Transfer

The connection from the TDC's to the data acquisition (DAQ) system is performed on serial links using thin cables with shielded twisted pairs. LVDS signals of 80 Mbits/s (or 160 Mbits/s) will be used for these links.

Several TDC's can share one serial link using a token based protocol (Fig. 4) to assemble data belonging to one event. The serial data from the TDC's in the daisy chain is sent from one TDC chip to the next together with a token finally arriving at the master TDC driving the serial link to the DAQ system. To avoid a complete loss of data, a scheme for bypassing the serial data around a failing TDC will be implemented.

The serial front-end link is likely to use a two wire data encoding scheme used by commercial transputer links (DS-Link). This encoding requires two wires but removes the need of any clock recovery circuitry in the front-end receiver.

Test and monitoring

The fact that the TDC is going to be embedded inside the detector requires special attention on monitoring and in system testing capabilities.

The standard IEEE 1149.1 JTAG protocol [10] is today an accepted standard for in system chip and module testing. The use of full boundary scan enables efficient testing of TDC module failures (shorts and opens between ICs) while located in the system. The TDC uses parity check on all its internal storage elements to detect single event upsets caused by radiation.

3. Simulation

Simulations of the baseline TDC architecture under different conditions have been done using the Verilog simulator [11].

The TDC has in its internal architecture a merging of hits from 24 channels into one common first level buffer.

The four hit buffer per channel acts here as a limited de-randomizing buffer. Other possible bottlenecks in the system is the read-out and merging of data from several TDC's. The baseline simulation conditions are the following:

- trigger rate & latency = 100 kHz & 2.5 μs,
- minimum interval between two triggers = 75 ns,
- no more than 16 triggers in any given 16 μs period,
- 100 kHz hit rate (2/3 random and 1/3 correlated),
- drift time = 0 ~ 600 ns,
- mask & matching windows = 800 ns,
- search window = 1200 ns,
- reject offset = 4 μs,
- readout link speed 80 Mbits/s.

The TDC architecture is also simulated under 300 kHz hit rate conditions. This condition shows how the TDC behaves under much higher hit rates than expected.

Hit and trigger generation

The average number of hits matched with triggers is 1.87 for the baseline conditions. At 300 kHz hit rates, the average value is 5.10.

In addition to the matched hits, there is a masked hit word if hits are found in the mask window. The fraction of events having one or more masking hits at baseline conditions have been found to 85% . For 300 kHz hit rates 99% will have a mask flag. The average total event size (without header/trailer) for the 24 ch TDC will be;

1.87data+0.85maskhit = 2.72words/event (@100kHz),
5.10data+0.99maskhit = 6.09words/event (@300kHz).

Channel buffer occupancy

The data transfer from the channel buffer to the first level buffer is an essential part of this TDC architecture. In present Verilog models it takes 4 clock cycles to transfer a single hit into the level one buffer. When several hits are waiting, the first takes 4 clock cycles to transfer and the following are handled with a rate of one hit per clock cycle. To make a conservative simulation an additional clock cycle has been added to the transfer time of the first hit.

The average occupancy is 2.1 x 10^{-4} and 8.3 x 10^{-4} for 100kHz and 300kHz hit rates respectively. No missing hits have been seen in a one million hits simulation.

First level buffer occupancy

In the baseline condition the average buffer depth is 8.9 and with a maximum of 34 (at the level of 10^{-6}). At 300 kHz hit rates the average value increases to 24.9 and the maximum reaches 60.

Double track separation.

In case double track separation is required, the critical part of the TDC for this mode of operation is the limited size of the channel buffers.

The hit rejection have been simulated and shown in the Table 2. The acceptance of hits have been divided into three different sub groups. Primary hit: single track hit, Secondary hit: hit from double track, Fake hit: noise hits from clustering of tube signal.

Table 2. The acceptance of hits in multi-hit mode in which the pulse width (charge) of primary hits is being measured.

Primary hit rate	prim. hit	second. hit	fake hit
50 kHz	100 %	94.1 %	94.2 %
100 kHz	99.99 %	93.1 %	93.0 %
400 kHz	99.86 %	90.4 %	90.1 %

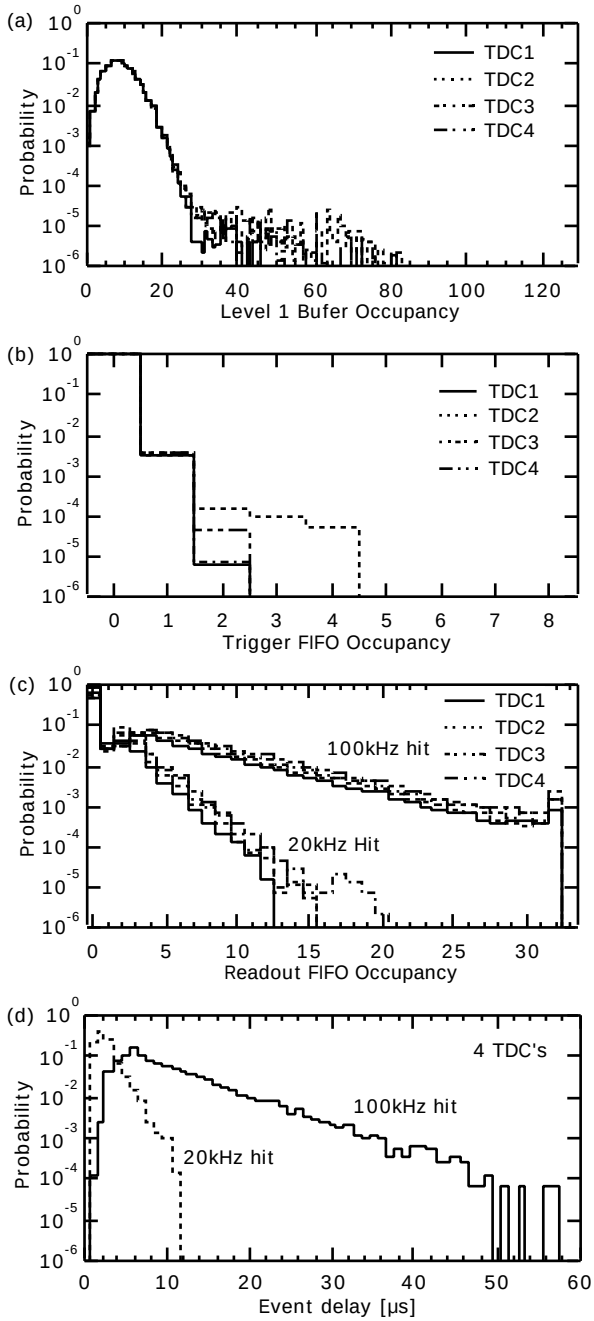

Fig. 5 Simulation for 4 TDC's per serial link. (a) first level buffer occupancies at 100kHz hit rate, (b) trigger FIFO occupancies at 100kHz hit rate, (c) readout FIFO occupancies, (d) event delay.

It can be seen that the acceptance of secondary hits are in all cases better than 90 %. Since there are around 1.5 hits per single track in this mode, the effective hit rate seen by the TDC is 400 kHz * 1.5 = 600 kHz at the highest rate. Simulations show that a first level buffer depth of 128 words is still sufficient.

Readout of four TDC's on a shared link

The performance of the readout architecture depends heavily on the number of TDC's sharing a serial link. At a 100 kHz hit rate, 2.72 words must be transferred from a TDC to DAQ system per trigger. With a trigger rate of 100 kHz this requires an average serial bandwidth of 8.7 Mbits/s per TDC (without header and trailer).

As an example of a rather severe condition, simulation results for the merging of data from 4 TDC's are shown in Fig. 5 (data is sent from TDC1 at first, then TDC2 .. follows). First level buffer occupancies and trigger FIFO occupancies are shown in Fig. 5 (a) and (b) respectively. The tails of the distribution come from the overload of the link as seen in Fig. 5 (c). The readout FIFO become full at the probability of 10^{-3} at 100 kHz hit rate. The maximum event delay in this case reaches about 60 μs (Fig. 5 (d)).

To prevent excessive long event delays it is desirable only to utilize half the maximum bandwidth available. Thus the maximum number of TDC's per serial links must be carefully choosed depend on the detector position.

4. Radiation Damage

The worst case neutron fluence and ionizing radiation doses in the MDT system in 10 years of high luminosity LHC operation are estimated to be 3 x 10^{12} neutrons/cm^2 and 1 krad respectively. Commercial CMOS processes are known to be relatively insensitive to neutron damage and normally support this level of ionizing radiation.

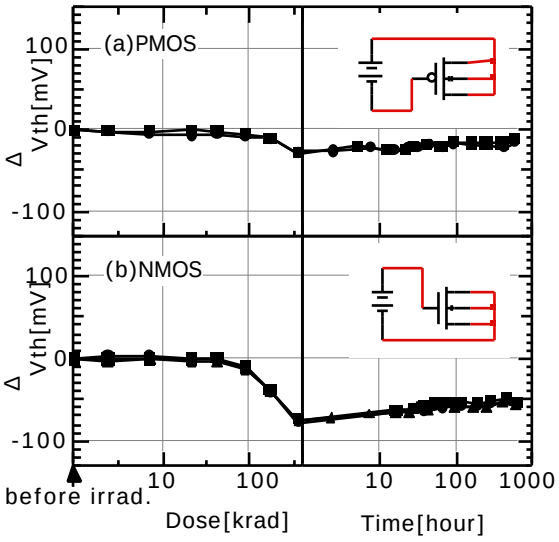

Fig. 6 Threshold variation of 0.5 μm CMOS transistors for irradiation dose and annealing time. Transistors are biased as ON state during the irradiation.

Radiation tests with an existing chip fabricated in a one generation older process (0.5 μm) from the same company (Toshiba) have been done and some results are shown here. We have used ^{60}Co γ-ray source, and irradiated up to 350 krad with a dose rate of 120 rad(Si)/sec rate.

Fig. 6 (a) and (b) shows the variation of threshold voltage for PMOS and NMOS respectively. Both transistors are biased to ON state during irradiation. OFF state transistor shows less variation than ON state one. We observed only 5 mV and 15 mV threshold shifts for PMOS and NMOS transistors at 100 krad. This is almost negligible compared with threshold variations from process (~100 mV). There is no apparent change in mutual conductance (Gm) and channel conductance (Gds).

An increase in drain leakage current at Vgs=0V and Vds=3V is observed for NMOS transistors above 10 krad. It becomes 10^{-6}A at 50 krad (normally $<10^{-12}$A). This leakage current causes an increase of the power consumption, but we still have a large margin for the use in the MDT.

5. Summary

The architecture study of a TDC for the MDT chamber have been presented. A TDC, using a PLL for a fine time measurement and having several internal buffers is shown to be adequate for the ATLAS MDT.

Several simulations of the baseline TDC under realistic conditions show that the present TDC architecture works satisfactory at hit rates per channel above 100 kHz and a trigger rate of 100 kHz. A study of the radiation hardness of a similar sub-micron CMOS process shows promising results.

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