Time Memory Cell VLSI and a High-Speed Serial Interface

Y. Arai and M. Ikeno,
KEK, National Laboratory for High Energy Physics

H. Shirasu and T. Emura
Tokyo University of Agriculture and Technology

A precision variable delay implemented in a LSI is one of the key elements in LHC experiments. Realizing such delay with a PLL technique, we have been developing low-power and high-density pipeline TDC chips for high-rate tracking detectors. The chip, named Time Memory Cell (TMC), has been adopted in several high-rate experiments and is proposed for the muon high-precision tracker of the ATLAS experiment. With this delay element, we also build a simple high-speed parallel-to-serial converter to solve a pin-count problem in trigger chip. The present status of the TMC and the first test results of the parallel-to-serial converter are presented.

I. INTRODUCTION

In LHC experiments, beam crossing interval will be 25 ns and many events will occur in each crossing. These very severe conditions require high precision delay elements in electronics for timing adjustment in trigger and readout system. Since our first idea to use an internal gate as a variable delay element [1], it is realized that high precision delay element of around 1 ns is easily available in conventional CMOS LSI.

At first, we developed a full-custom CMOS TDC chip [2,3] by using a Delay Locked Loop (DLL) circuit. The chip (TMC1004) attained 520 ps RMS timing resolution and has 4 channels of 1 μsec buffer. After our success of the chip, several groups are also developing TDC chips of the same kind [4,5,6]. Although the TMC1004 fulfills most of our basic requirements, we proceeded to a gate array technology to reduce development cost and turn-around time further. In addition, the gate-array structure is more adequate for a radiation-hardened process due to the uniform physical structure of transistors.

The direct conversion of the TMC circuit to a gate-array is not tribual due to the difference in the technologies; we thus developed a new time digitizing circuit with a phase locked loop (PLL) circuit. To obtain an even number of equally spaced timing signals, we invented an asymmetric ring oscillator. Besides the expected reduction of cost and the turn-around time, the time resolution and stability have also been improved in a new chip (TMC-TEG3) and attained time resolution of 250 ps RMS [7].

The TMC is adopted in D0 and PHENIX experiments for drift chamber readout and is proposed for the readout of ATLAS muon high-precision tracker.

Basic structure of the TMC can be considered as a serial-to-parallel converter so that it is straitght forward to make it a serial-to-parallel converter. Reversing the structure produces a parallel-to-serial converter as well.

Although a high-speed serial interface chip for network application is commercially available, it is not so easy to include such circuit in a custom LSI. Furthermore, in a recent LSI, usable number of gates is huge, but the number of input signal is limited by pin counts of the package. If a simple parallel/serial converter is implemented within a custom trigger chip, number of trigger signals handled in a single chip is greatly increased.

In this paper, we present status of the TMC chip development, and describe first test results of the parallel-to-serial converter.

II. TMC DEVELOPMENTS

A. TEG3 Chip

The TMC-TEG3 chip (Fig. 1) was developed in 1994 [4]. This chip already fulfills most requirements for the ATLAS muon detector; precise timing resolution of 250 ps, level-1 buffer of 3 μs, deadtime-less readout, dual-edge detection, low-cost and high-density. The chip was fabricated in a 0.5 μm CMOS gate-array technology.

A new asymmetric ring oscillator was developed for the TMC-TEG3 chip. A ring oscillator normally comprises an odd number of inverter stages; an odd number of timing signals can be obtained. However, an even number of timing signals (especially in 2's power) is desirable for the TMC. To obtain those signals we developed an asymmetric ring oscillator which generates an equally spaced even number of timing signals.

A simplified schematic of an asymmetric ring oscillator comprising 8 stages and their timing diagram are shown in

Figs. 2-(a) and 2-(b), respectively. The present TMC chip implements 32 stages. Timing signals are extracted from node A through H. With these timing signals, an input signal is latched at the timing equally spaced by T/8 (T/32).

Fig. 3 shows a timing resolution of the TMC-TEG3 chip. The RMS value of the data is 249 ± 6 ps. Since one LSB is 781 ps, the quantization error is 226 ps (= 781 ps / √12), indicating that the inherent error of the chip is about 100 ps. The characteristics of the TEG3 chip are summarized in Table. 1.

Table 1. Characteristics of the TMC-TEG3 chip.

Technology	0.5 μm CMOS Sea-of-Gates (TC180G).
System clock	50 ~ 10 MHz (12.5 ~ 2.5 MHz : x4 mode). single ended : CMOS level, or differential : ΔV > 50 mV (Vc = 2 ± 0.6 V).
Digitization Step	0.6 ~ 3.1 ns/bit (= clock period / 32).
Time Resolution	250 ps rms @40 MHz.
Differential/Integrated Non-linearity	< 0.1 LSB
Time Range	2.56 μs ~ 12.8 μs (clock period x 128).
Input Channels	4 ch (single ended or differential).
Master Gate Size	66k Master where 32k gates were used.
Phase Locked Loop	Response time : ~ 4 μsec.
Encoding Scheme	(hit tag + 5 bit) x 2 (rise and fall)
Double Pulse Reso.	≤ Clock Period
Power Consumption	< 200 mW (Vdd=3.3V) @40 MHz, 1 MHz input, 100 kHz readout.
Package	0.5 mm lead pitch, 144-pin plastic QFP.

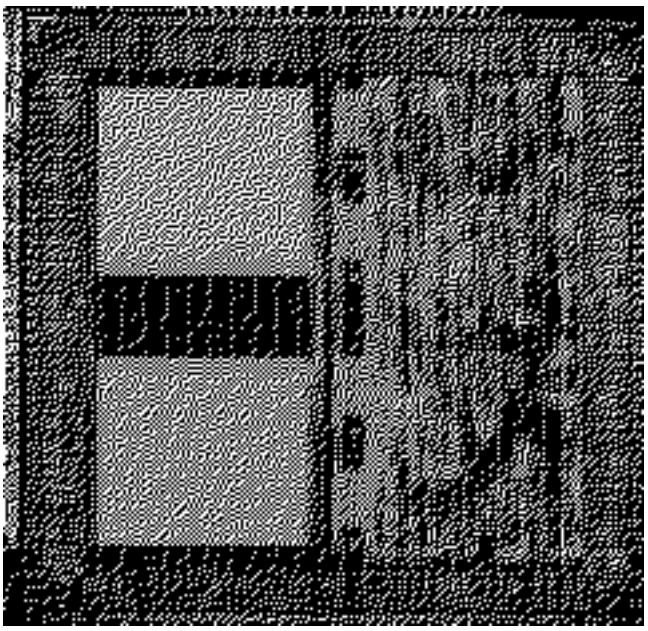

Fig. 1 Photograph of the TMC-TEG3 chip. The die size is 6.4 mm by 6.4 mm.

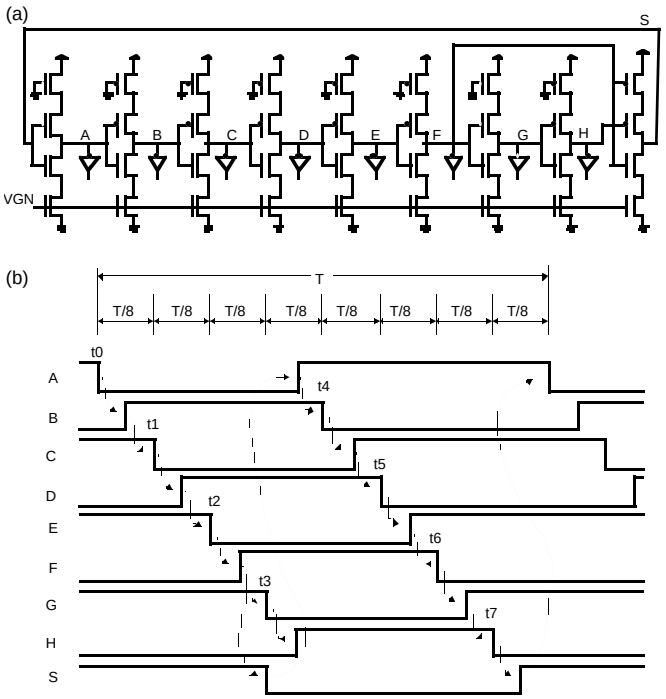

Fig. 2 An 8-bit example of the asymmetric ring oscillator. VGN is a delay control signal from a PLL circuit. (a) A circuit schematic, (b) timing diagram.

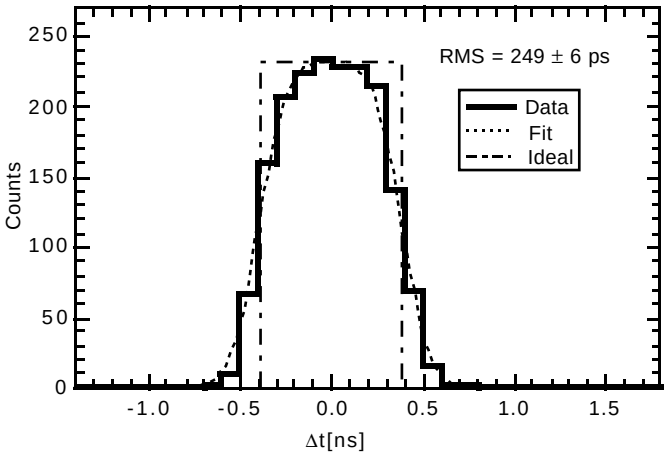

Fig. 3 Time-resolution measurement of the TMC-TEG3. Clock frequency for the chip was 40 MHz.

B. TMC-VME module

A 6U VME module (Fig. 4) has been developed [8] with the TMC-TEG3 chip. The module implements 8 TMC-TEG3 chips (32 channels) and a DSP. A block diagram of the module is shown in Fig. 5. The module works for both common start and common stop mode. The acquired data are stored in a dual port memory which can be accessed both from the DSP and from a VME bus. Most of the random logic is implemented in two complex PLD's.

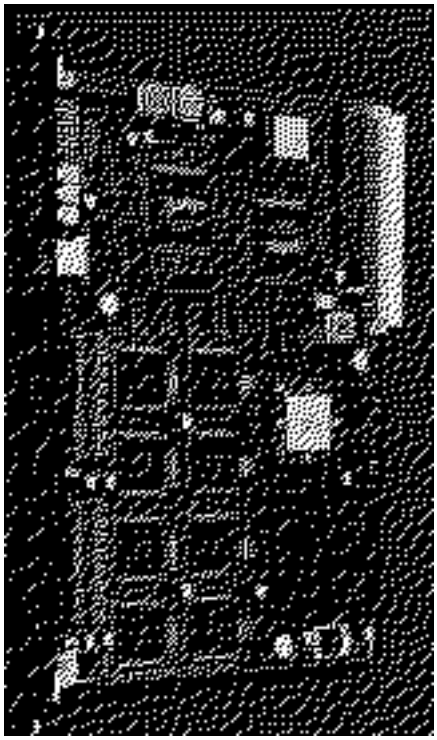

Fig. 4 Photograph of the 32 ch TMC-VME board.

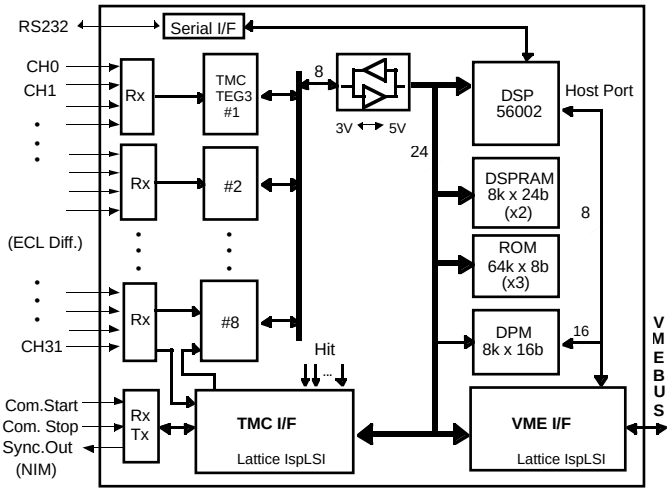

Fig. 5. Block diagram of the 32 ch TMC-VME module.

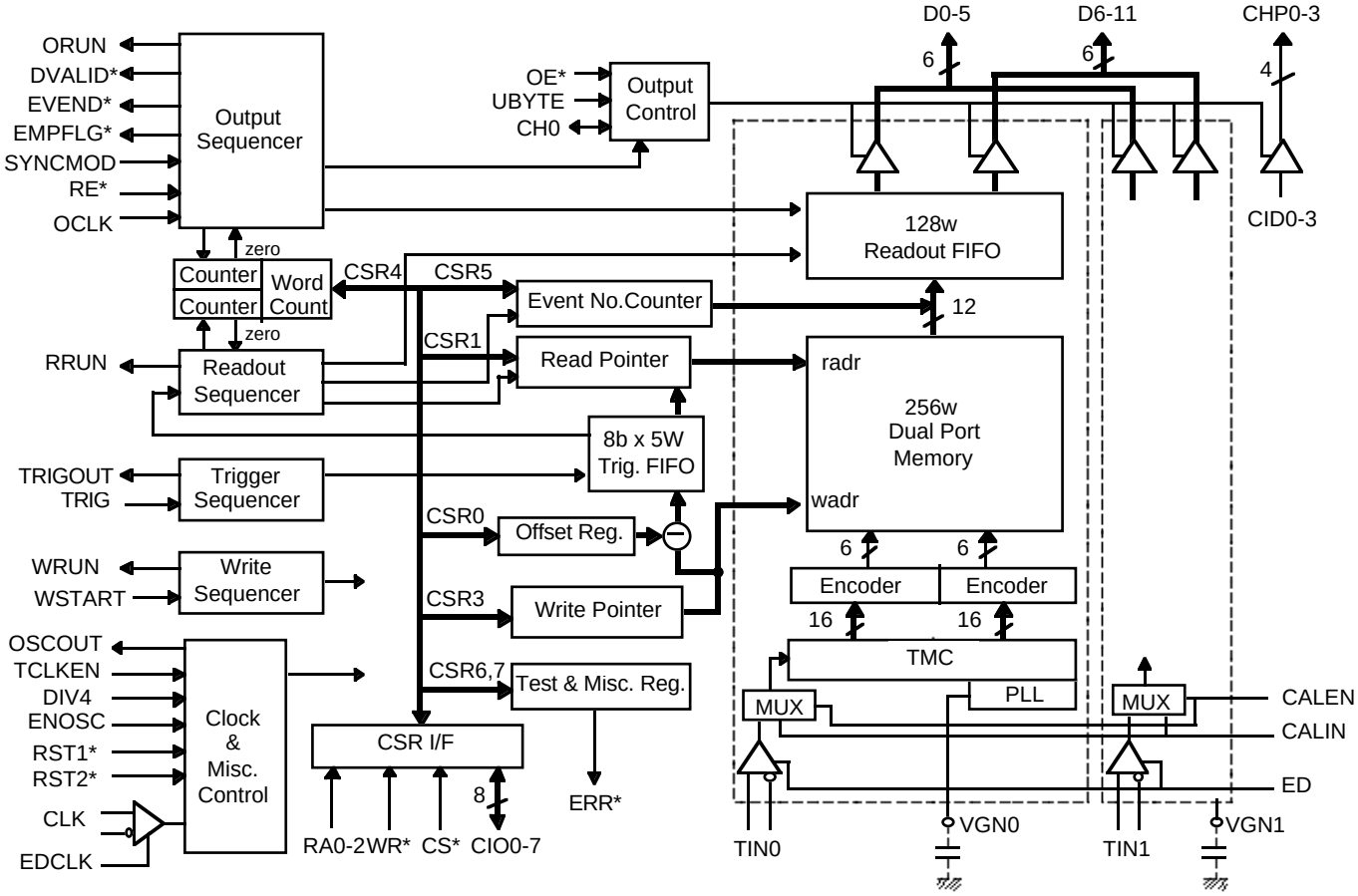

Fig. 6 Block diagram of the TMC-TEG5 chip.

C. TEG5 Chip

In the latest version of the TMC chip (TMC-TEG5), more functions which are required in high-rate experiments were added. The block diagram of the chip is shown in Fig. 6. The TEG5 chip is a prototype chip for the PHENIX experiment and contains 2 channels of circuit (production chip will have 4 channels).

This chip includes a trigger FIFO, readout FIFO's and related sequencers besides the TMC circuit. The depth of the dual port memory is increased from 128 of the TEG3 to 256. There are two encoders and each encoder covers 16 bit. Thus the double pulse resolution is reduced to less than 14 ns. The chip can accept up to 5 consecutive trigger signals which is the requirement of the PHENIX experiment, and the trigger FIFO stores the corresponding event position from where the data are read out and transferred to the readout FIFO.

III. SERIAL INTERFACE

In an ATLAS muon trigger, a large number of coincidence logic is required to generate a trigger signal. Each coincidence logic is relatively simple but the number of signals handled in a chip is limited by available pin counts of the package. Thus the detector part covered by a trigger chip is limited and many interconnections between trigger chips are necessary.

Number of cables can be reduced by using commercial serial interface chips, but this does not solve the pin counts problem. If we can implement a serial interface and the coincidence logic in the same chip, number of channels processed in a chip can be greatly increased. Thus the problem of the interconnection and boundary overlap are reduced.

Since the TMC circuit can be regarded as a kind of serial-to-parallel converter (S-to-P), we have built a test circuit of a parallel-to-serial converter (P-to-S) by using the same delay elements used in the TMC circuit.

The schematic and the output wave form of the parallel-to-serial converter are shown in Fig. 7-(a) and 7-(b) respectively. A parallel data is latched in flip-flop's sequentially at a fixed time interval, and outputs of the flip-flop are connected to exclusive OR's. The serial output will change at the data of "1" and not change at the data of "0" (NRZI: non return to zero change on one). Along with the data, a start bit and two stop (parity) bits are included, thus in total 11 bits are sent out in a cycle. For synchronization between P-to-S and S-to-P, we provided a separate synchronizing signal in this test.

Since there is no 50Ω driver in the gate-array library which we were using, we used most powerful output driver (24 mA, high-speed type) available.

Fig. 8 shows a wave form measured after a 10 m-long RG-174/U cable. Clock frequency of 20 MHz was used in this measurement. Since 11 bits were sent out in a cycle, this corresponds to 220 Mbps. The rise and fall time of the signal was still less than 2 ns after the 10 m long cable, and we can see eye patterns clearly. High level output voltage reached 2.7V while the power supply voltage was 3.3 V. Since the circuit layout was done automatically and not optimized, some variation of delay time between bits was observed.

There are still many items to be optimized; use of a differential signal, clock synchronization method, error collection and so on.

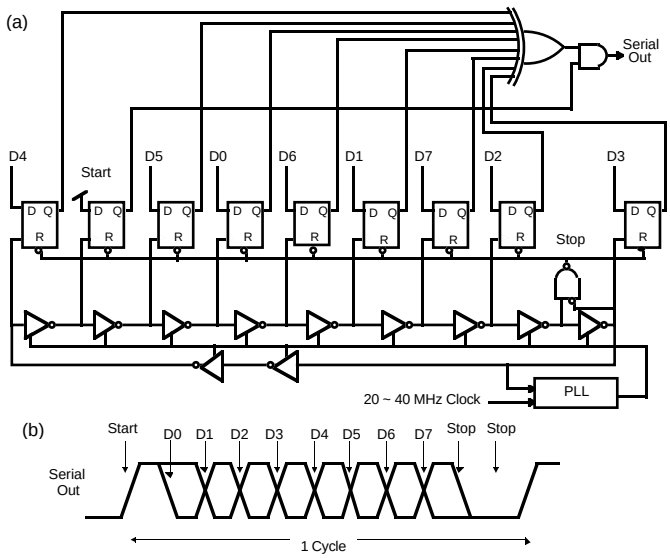

Fig. 7. (a) Simplified schematic of the parallel-to-serial converter. (b) Serial output wave form.

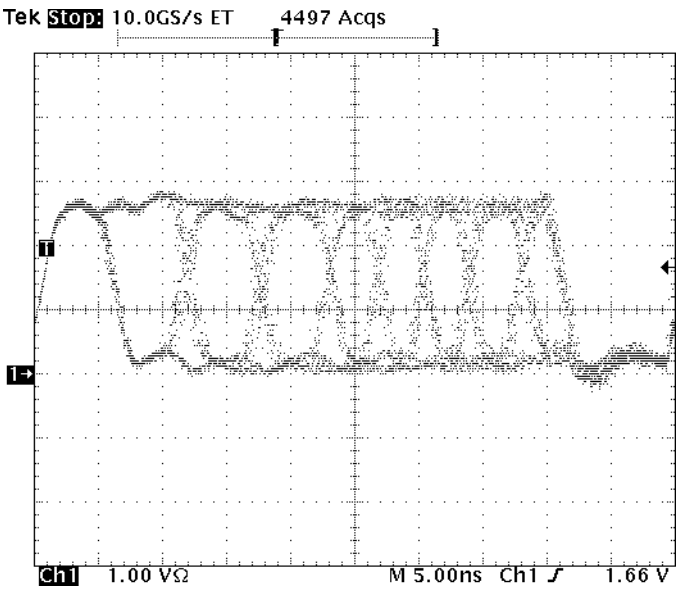

Fig. 8. Serial output wave form measured at 10 m point of the RG-174/U cable. Clock frequency was 20 MHz.

IV. SUMMARY

We have been developing a high-precision Time-to-Digital converter chip (TMC) and its module. The TMC is used in high-rate experiments and proposed for the ATLAS muon high-precision tracker. In addition to the TDC functions, the recent chip includes data handling functions for the second level bufferring.

We also tested a new parallel-to-serial converter, and succeeded to measure up to 220 Mbps serial transmission of the signal after 10 m-long cable. This result is very promising for developing a serial interface for a trigger chip which will run at LHC clock frequency of 40 MHz.

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REFERENCES

[1] Y. Arai and T. Ohsugi, "An Idea of Deadtimeless Readout System by Using Time Memory Cell", Proceedings of the Summer Study on the Physics of the Superconducting Supercollider, Snowmass, (1986)455.

[2] Y. Arai and T. Baba, "A CMOS Time to Digital Converter VLSI for High-Energy Physics", in Symposium on VLSI Circuits Digest of Technical Papers, pp. 121-122, June 1988.

[3] Y. Arai and T. Matsumura and K. Endo, "A CMOS 4 ch x 1 k Time Memory LSI with 1 ns Resolution", IEEE J. of Solid-State Circuits, vol. 27, pp. 359-364, March 1992.

[4] M. Campbell, J. Chapman and J. Mann, "A Deadtime-Less Multihit TDC ASIC with Buffers", Proceedings of the International Conference on Electronics for Future Colliders, LeCroy Co., May, 1993, pp. 91- 98.

[5] M. J. Loinaz and B. A. Wooley, "A BiCMOS Time Interval Digitizer for High-Energy Physics Instrumentation", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 28.6.1 - 28.6.4.

[6] C. Ljuslin et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Trans. on Nucl. Sci. vol. 41, pp.1104-1108, 1994.

[7] Y. Arai and M. Ikeno, "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution", to be published in IEEE J. of Solid-State Circuits, Jan. 1, 1996.

[8] Y. Arai, M. Ikeno, T. Murata, H. Shirasu and T. Emura, "A VME 32 ch pipeline TDC module with TMC LSI", to be published in IEEE Trans. on Nucl. Sci.