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Abstract

Architecture of the front-end electronics for the ATLAS muon precision chamber (MDT) is presented. Especially, test results of a prototype TDC chip are described in detail. The chip was fabricated in a 0.3 μm CMOS Gate-Array technology. Measurements of critical elements of the chip such as the PLL, and data buffering circuits demonstrated adequate performance. The effect of gamma-ray irradiation, using a Co^{60} source, and neutron irradiation, were also examined. The test results revealed radiation tolerance adequate for the operation of the circuits in the environment of the ATLAS MDT. Mounting of the front-end electronics to the MDT is scheduled to start in year 2001.

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Keywords: ASD; TDC; PLL; Radiation damage

1. INTRODUCTION

The ATLAS muon spectrometer is designed for stand-alone measurement capability and aiming for a P_T resolution of 10% for 1TeV muons. This requires a single wire resolution of <80 μm and a systematic timing error for an individual tube of about 500ps. Maximum hit rate is estimated as 400 kHz per tube (including a safety factor of five). The ATLAS MDT (Monitored Drift Tube) system consists of about 1,200 chambers, and each chamber has two super layers (3 or 4 layers of individual tubes). There are about 370 k drift tubes of 3cm diameter, with lengths from 1.5 to 6m.

To avoid aging problems, Ar/CO_2 93/7 (3 bars absolute), which has a maximum drift time of 800ns and is very nonlinear, is finally selected for MDT gas. The long drift time and the non-linearity cause multiple threshold crossings even for a single hit. A scheme of a bipolar shaping and a fixed dead time equal to the maximum drift time is adopted to avoid multiple hits from multiple threshold crossings for a single track. Although this cause dead time increase of a few

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percent, it was shown that this does not cause a degradation of the pattern recognition efficiency [1].

The task of MDT front-end electronics is to process the information contained in the ionization electrons arriving at the anode wire. An amplifier-shaper-discriminator (ASD) chip [2] converts the induced current signal into a voltage pulse which is sent to a discriminator. A time to digital converter (TDC) measures the time of the leading (and trailing edge) of the discriminator output and stores it in a buffer.

All the front-end electronics located near detector must have adequate radiation tolerance. Total dose expected for worst location of the MDT electronics is 11 krad for 10 years LHC operation (including a safety factor of 4). The expected neutron flux at MDT front-end electronics for 10 years of LHC operation is less than 1.2×10^{13} n/cm^2 (including safety factor of 4). Radiation tolerance test for the TDC chip is described in section 3.

2. FRONT-END ARCHITECTURE

Block diagram of the MDT front-end electronics is shown in Fig. 1. Three ASD chips and one AMT (ATLAS Muon TDC) chip are mounted on a small multi-layer printed circuit board (readout board), which plugs into an MDT end plug PCB. A Chamber Service Module (CSM) [3] is located just outside of the MDT chamber. The CSM merges up to 18 TDC links to a fast optical link signal and send data to a Muon Readout Driver Module (MROD).

Each superlayer is entirely enclosed in a faraday cage shield at both ends. All DC signals are filtered at the shield entry point. All AC signals entering or leaving the shield are low-level differential signals (LVDS). Each complete MDT chamber is electrically isolated from the support structure, and all services (gas, electrical, etc) are also electrically isolated or floating at the source. The JTAG interface [4] is used to load various settings for the ASD and the TDC chips, and it will also be used for board level testing during production as well as system testing.

Two modes of operation will be provided in MDT measurement (Fig. 2). In one mode the ASD output gives the time over threshold information, i.e. signal leading and trailing edge timing. The other mode measures leading edge time and charge and is considered the default operating mode. The Wilkinson ADC serves as a time slew correction and also provides diagnostics for monitoring chamber gas gain. It operates by creating a gate of ~20ns width at the leading edge of the signal, integrating charge onto a holding capacitor during the gate, and then running down the hold capacitor at constant current (the maximum rundown time is of order 100ns). The discriminator also generates artificial dead time to avoid multiple hit.

The ASD is contained within a custom 8-channel CMOS IC which is processed in HP 0.5μm n-well CMOS. The outputs of three ASD chips drive a 24-channel AMT.

3. AMT DEVELOPMENT

The AMT must be a high-resolution (sub-nano second), low-power (20 mW) and low-cost LSI. To study the chip architecture, intensive Verilog simulations were done [5]. In addition, a quick test chip was fabricated in a 0.7 μm CMOS process [6] for a medium scale system test (10 k channels) of muon front-end electronics.

Since the mass production of the chip is scheduled in year 2001, we have selected a relatively advanced process, 0.3 um CMOS Gate-Array technology (Toshiba TC220G), for the AMT chip. This new process provides a lower per channel cost and higher performance. In addition, we can expect a longer lifetime for the process, and, in turn, easier maintenance. To measure the basic performance of the design and confirm the radiation tolerance of the process, we have developed a test element group chip (AMT-TEG) using the 0.3 μm process. The chip contains bare NMOS and PMOS transistors, a ring oscillator for radiation tests. Gamma-ray irradiation was performed with a Co^{60} source at Tokyo Metropolitan University. Neutron irradiation was performed at the PROSPERO reactor in France.

Photograph of the chip is shown in Fig. 3, and a block diagram of the AMT-TEG chip is shown in Fig. 4. The AMT-TEG chip also contains most of circuits used in the final AMT chip. Only the trigger interface and trigger matching circuit are excluded. In addition some circuits were simplified and error checking was minimized. To reduce number of input pins, only 16 hit input pins are implemented and selectively connected to the internal circuitry. Since the detailed operation of the chip is described in other documents [5, 7], only brief explanation is presented here.

The hit signal is used to store the fine time and coarse time measurement in individual channel buffers. The fine time measurement is obtained from taps along an asymmetric ring oscillator. The time of both leading and trailing edge of the hit signal (or leading edge time and pulse width) can be stored. Each channel has a 4 word buffer where measurements are stored until they can be written into the common first level buffer. To achieve a high-resolution time measurement with sufficient stability, Phase Locked Loop (PLL) is used to stabilize the asymmetric ring oscillator. The PLL circuit produces a double frequency clock of 80 MHz from the LHC clock (40MHz). By dividing the 12.5 ns clock period into 16 intervals a time bin size of 0.78 ns is obtained.

3.1 PLL and Ring Oscillator

Although the chip is designed in a gate-array technology, layout of the time critical parts such as PLL and the asymmetric ring oscillator were designed manually to achieve high resolution. We determined the jitter of the PLL circuit by measuring the oscillation period of each cycle. RMS values of the measurements versus frequency and power supply voltage are plotted in Fig.

5 (a) and (b) respectively. The jitter of the PLL is small (< 140 ps) and stable for the 40-120 MHz frequency range and for supply voltages between 2.8 - 3.8 V (normal operating condition is 80 MHz and 3.3V respectively).

The jitter shows a small structure around 90 MHz and the value is a little worse than that of the previous chip [8] which was fabricated in a 0.5 μm process. However the jitter is still small enough for the MDT detector which requires 500 ps resolution. Additional attention will be directed to the layout around the PLL in next chip to achieve better stability.

3.2 Channel Buffer

Recording speed of the channel buffer is important to have a good double pulse resolution or edge separation. Minimum edge separation was determined by reducing pulse width and pulse separation until the hit information is lost. Leading and trailing edge of double pulses, of which width is 5 ns and separation is 10 ns, are successfully recorded in the 4 word channel buffer.

The data transfer speed from the channel buffer to the first level buffer is an essential part of this TDC architecture. If the channel buffer become full, further hit information will be lost. In a Verilog simulation, the probability of hit loss is very low ($< 10^{-6}$) for 300 kHz input rate in all channels. The transfer speed is measured by changing the number of simultaneous hit channels and determining the minimum hit interval where all hits are accepted.

In Fig. 6 minimum hit interval for N channel simultaneous inputs are plotted. Above the data point all hit information is recorded, but if the hit interval is reduced less than the data point, a part of the hit information become lost due to the lack of the transfer capability. The line in the figure shows expected speed from the circuit. We see the overhead for arbitration is only 2 cycle and successive data transfer occurs at each cycle.

3.3 Time Resolution and Non-Linearity

Time resolution was measured by supplying a clock synchronous hit signal to the input and varying the delay time of the signal. The result is shown in Fig. 7. The RMS value of 305 ps is obtained. This value is worse than that of previous TDC chip [8] which achieved 250 ps resolution, but still has adequate resolution for our purpose.

Non-linearity of the time measurement was measured by applying a hit signal for which the delay time is uniformly distributed, and counting the number of hits recorded in each bin. The Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are shown in Fig. 8 (a) and (b) respectively. Both are small enough (RMS < 70 ps) for our purpose.

4. TDC IRRADIATION TEST

4.1 Gamma-ray Irradiation

Gamma-ray irradiation test was done at Tokyo Metropolitan University with a Co^{60} source. The irradiation rate was about 90 rad(Si)/sec[9], and total dose irradiated was 100 krad(Si). During the irradiation so called worst bias conditions for MOS transistors (3.3 V is applied to NMOS gate, and no voltage is applied to PMOS gate), were used. To study post-radiation effects, parametric measurements were also done after annealing (1 week at 100 degree C) following the MIL-STD-883 method [10].

Total dose expected for worst location of the MDT electronics is 11 krad for 10 years LHC operation [11]. In a sub-micron process, most severe damage from the ionization process is an increase of leakage current. An increase of NMOS drain leak current above 25 krad(Si) was seen while no increase is seen in PMOS. Recovery of the pre-radiation condition is seen after the annealing in NMOS.

Threshold voltage shifts of transistors are not seen in PMOS transistors. NMOS transistor while small shifts (~100 mV) are seen in two NMOS transistors. Since these transistors do not have any protection circuit, the transistors are susceptible to damage. More samples are needed to confirm whether the shift is due to the irradiation or not.

Fig. 9 shows variation of oscillating frequency of a ring oscillator and supply current. The ring oscillator is composed of 33 NAND gates. The oscillating frequency becomes lower above 50 krad(Si). The total chip current was also increased above 50 krad(Si). Considering low dose rate in the LHC environment, the chip has enough margin to be used in the MDT environment.

4.2 Neutron Irradiation

Neutron irradiation was done at the PROSPERO reactor facility in France. Eight chips were exposed to neutron flux of 1.0×10^{13} and 4 chips were exposed to 1.6×10^{13} n/cm^2 (1 MeV neutron equivalent). During the neutron exposure, chips are placed in a conductive plastic case. The expected neutron flux at MDT front-end electronics for 10 years of LHC operation is less than 1.2×10^{13} n/cm^2 [11].

After cooling of the radioactivity (~ 2 months), we measured transistor parameters and ring oscillator frequency. We have not observed any apparent change in all sample chips.

5. SUMMARY

Front-end electronics architecture of the ATLAS Muon precision chamber is presented. Most of the front-end components are under development in US, and the TDC is being developed in Japan. Mounting of the final electronics to the MDT chamber is scheduled in mid 2001.

A TDC test-element group chip (AMT-TEG) was developed for circuit performance test. Radiation tolerance was also measured for gamma-ray irradiation and neutron exposure. The AMT-TEG chip demonstrated adequate circuit performance for the MDT TDC. In addition, the 0.3 μm process showed adequate radiation tolerance for both gamma ray and neutrons at the radiation level of MDT front-end electronics.

Acknowledgements

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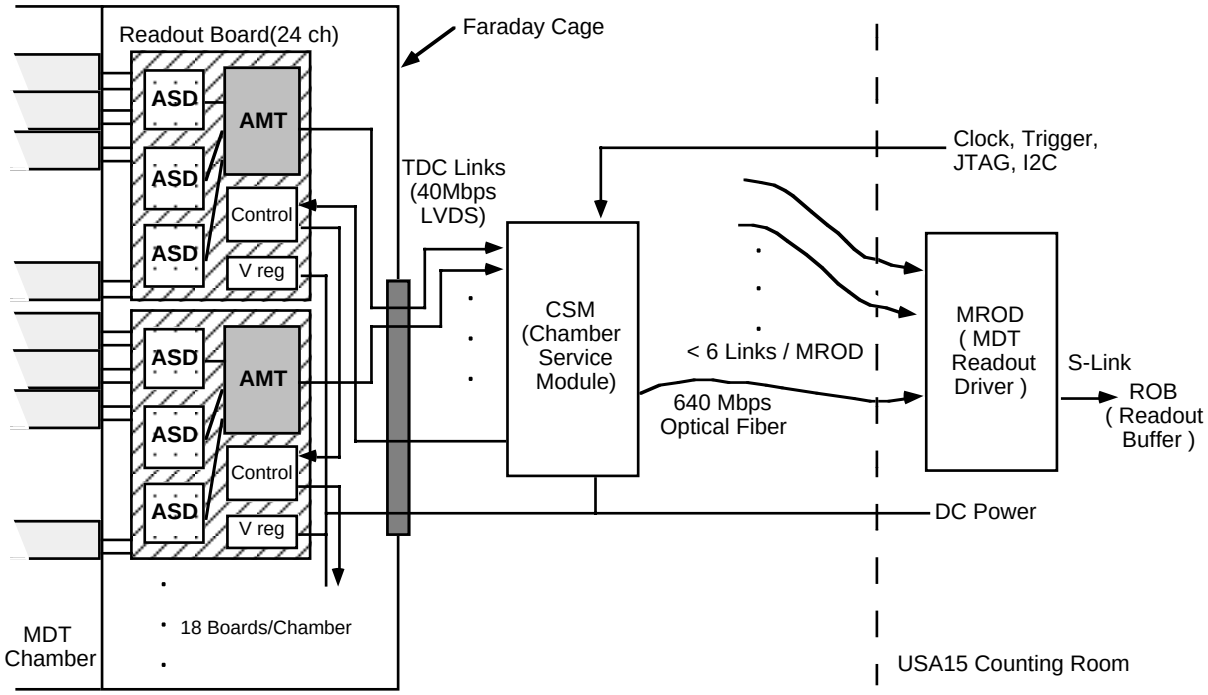

Fig. 1. Block Diagram of the MDT front-end electronics.

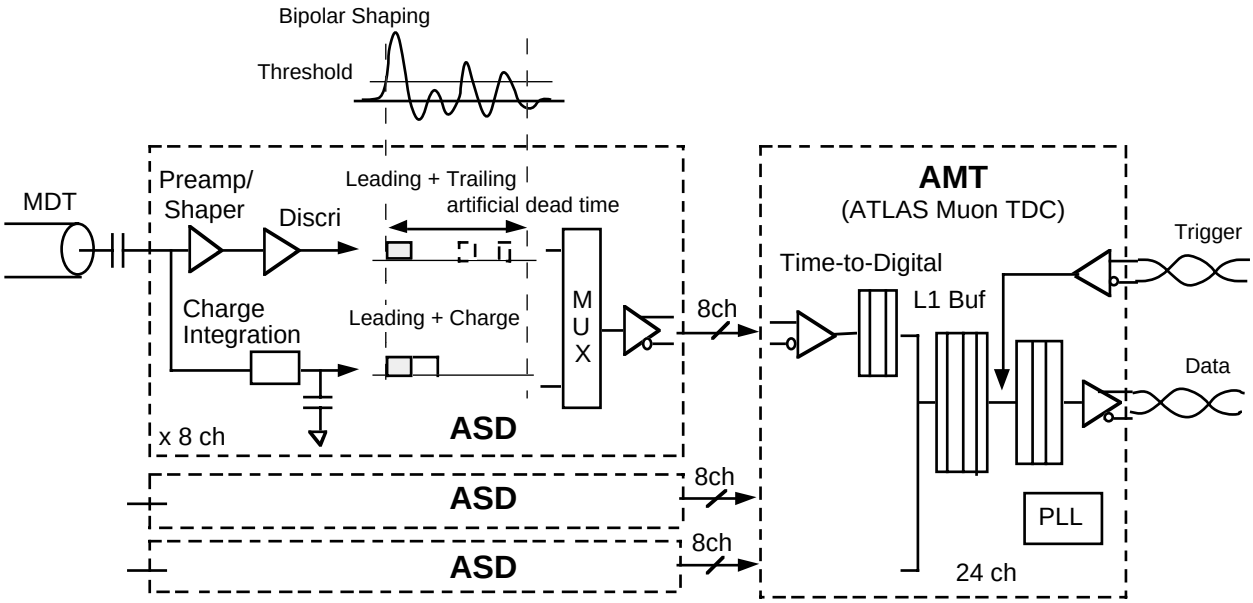

Fig. 2 Signal processing in the ASD and the AMT.

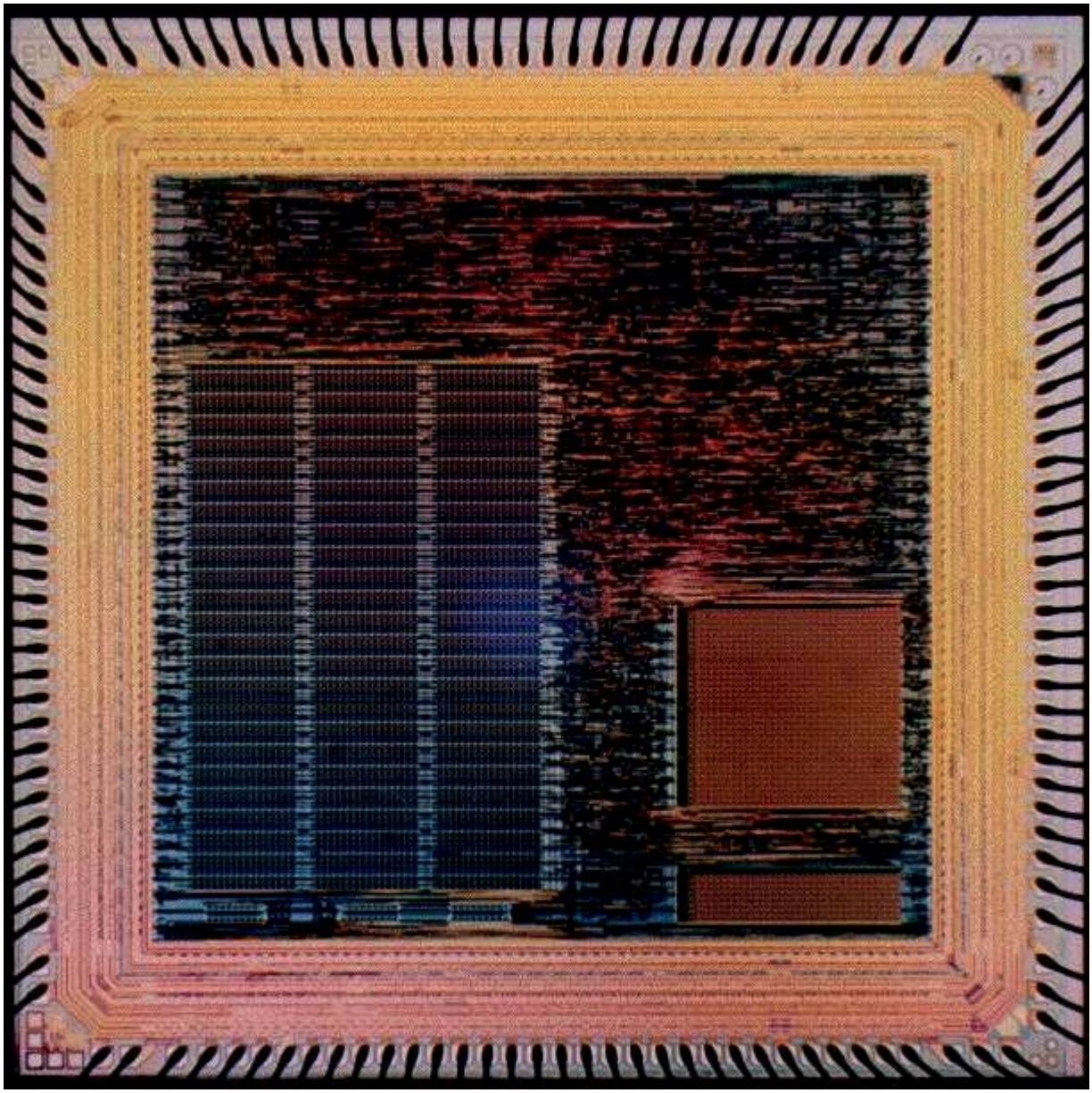

Fig. 3. Photograph of the AMT-TEG chip. The size of the chip is 5.2 mm by 5.2 mm. Total number of gates used is about 70 k gates. The large block in the left side is the 24-ch channel buffer.

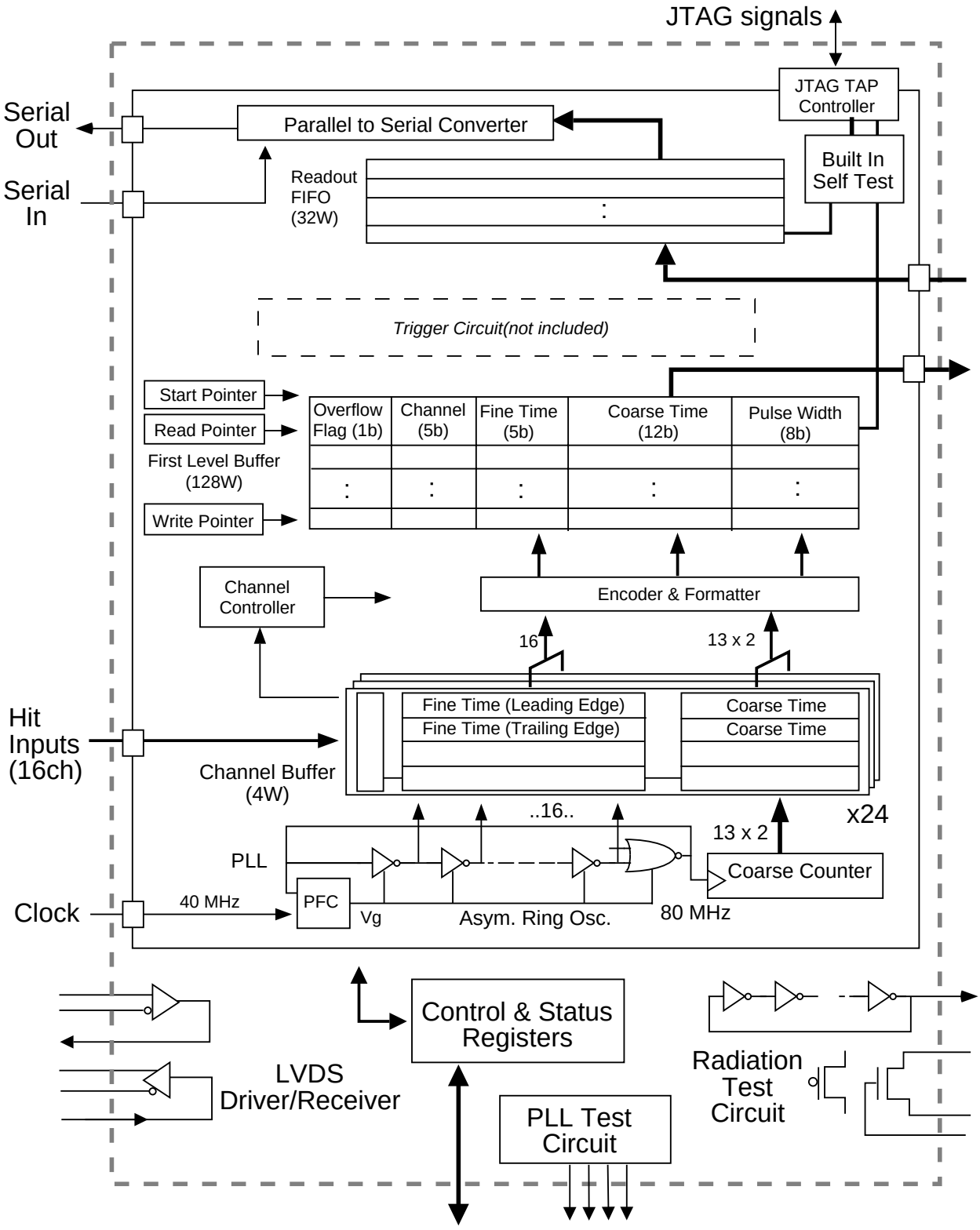

Fig. 4. Block diagram of the AMT-TEG chip.

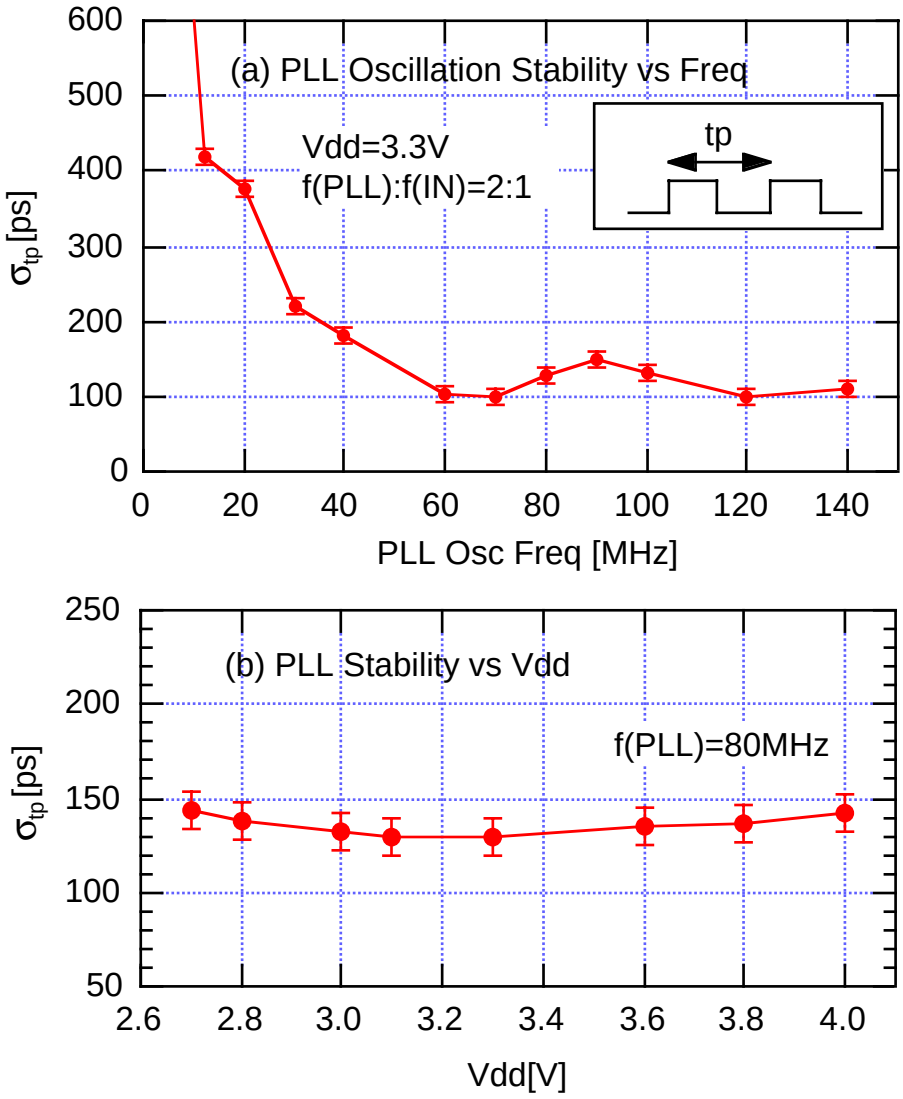

Fig. 5. (a) Stability of the PLL vs. oscillation frequency. (b) Stability of the PLL vs. supply voltage.

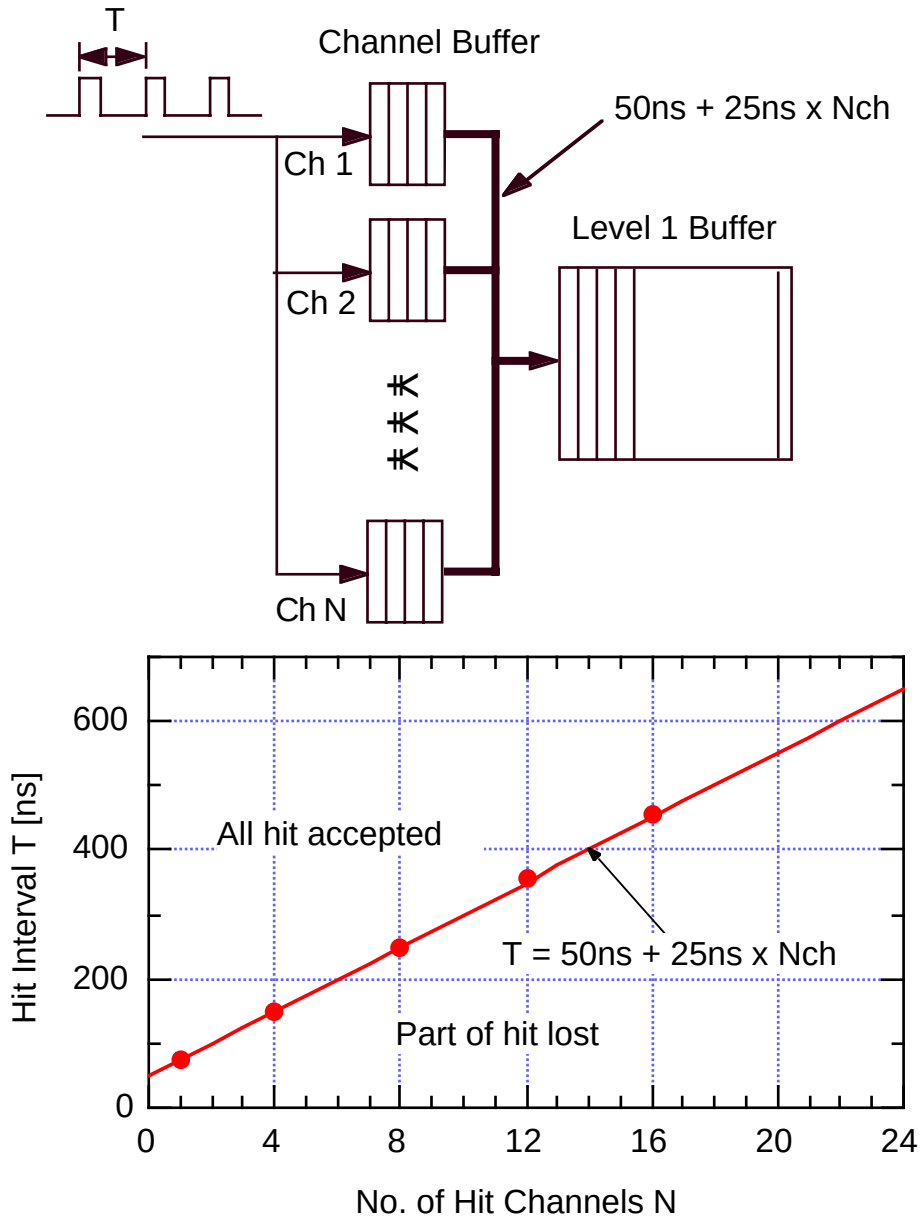

Fig. 6. Minimum hit interval for simultaneous hit inputs. System clock cycle is 25 ns. The data points show minimum hit intervals and the straight line indicates the expected performance from the 2 cycles plus N cycles required by the design.

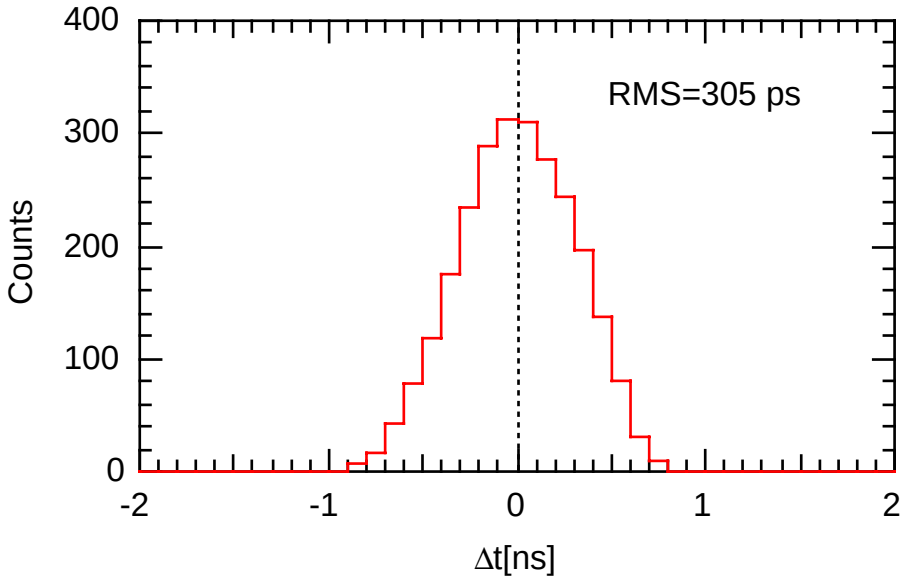

Fig. 7. Time resolution measurement. Input clock frequency is 40 MHz and time bin is 781.25 ps/bit. The data contains digitization error of 225 ps.

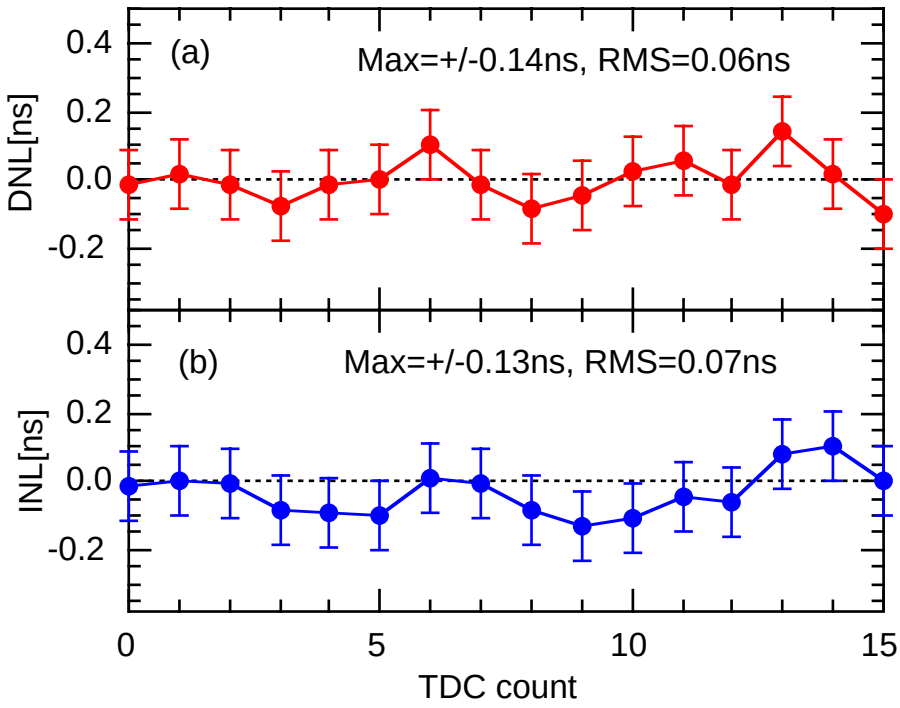

Fig. 8. (a) Differential non-linearity, and (b) Integral non-linearity measurement.

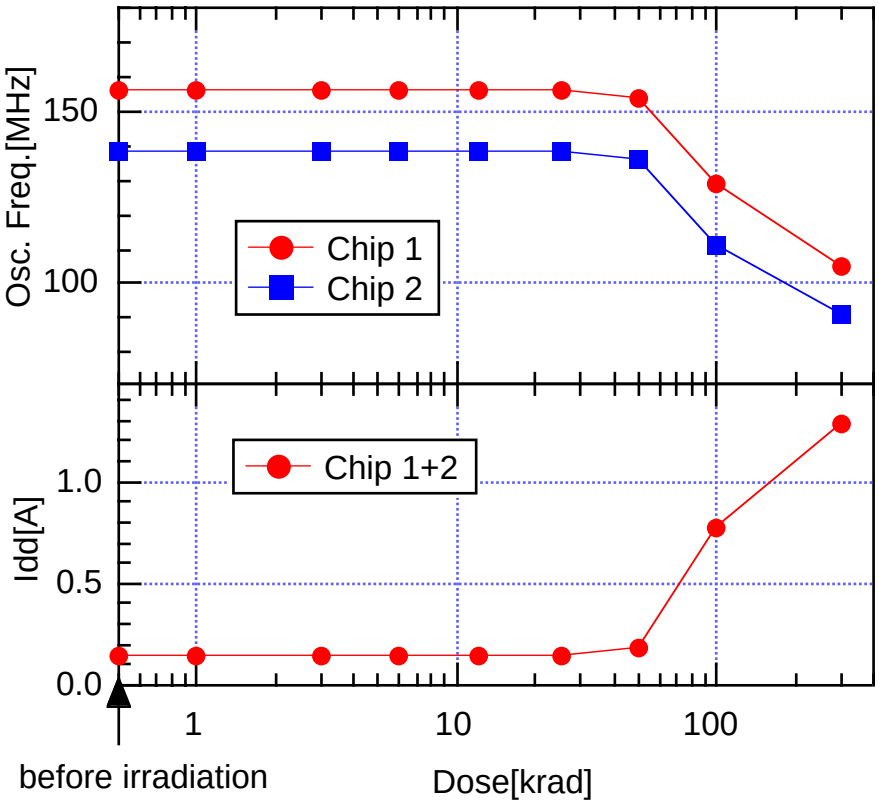

Fig. 9. (a) Oscillation frequency of a ring oscillator, (b) Total current of two chips. Left-most points show the value before irradiation.