Submitted to the 1999 IEEE Nuclear Science Symposium, Seattle, Oct. 24-30, 1999.

A Pipeline TDC Module with TMC-PHX1 LSI

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Abstract

A new 32-channel pipeline TDC module, which implements custom-developed Time Memory Cell LSIs, has been developed for high-rate wire-chamber applications. Time resolution of the module is 300 ps r.m.s., and the time range is 6.4 μsec. For handling data transfer and controlling the module, a 40MHz digital signal processor is implemented in the module. Most of the control logic is implemented in two complex PLDs to achieve a density of 32 channels in a single-width, double-height VME module.

I. Introduction

A high-precision and deadtime less Time-to-Digital Converter (TDC) modules are common instruments in recent high-energy and nuclear physics experiments. We have been developing several kinds of VME TDC modules [1, 2] which use our custom-developed Time Memory Cell (TMC) chips [3].

A new TMC chip, TMC-PHX1 [4], was recently developed for the drift chamber readout of the PHENIX experiment at the RHIC accelerator. To utilize the advanced performance of the chip in a small test experiments, we have developed a new VME TDC module by using the TMC-PHX1 chip.

The TMC-PHX1 chip has a r.m.s. timing resolution of 300 ps, records both rising and falling edge timings, and keeps past 6.4 μsec signal transitions. The chip has 4 channel inputs, and implements two levels of data buffers (level 1 buffer and readout FIFO) and a trigger buffer. After receiving a trigger signal, corresponding data are moved from the level 1 buffer to the readout FIFO. Up to 8 triggers can be buffered in the trigger FIFO. The chip was fabricated in a 0.5 μm CMOS gate-array technology, and packaged in a 100-pin plastic QFP.

One of the old TDC module (TDC-304) [2], which use the TMC-304 chips, has been widely used in many test beam experiments and K2K experiment [5]. However, the TMC-304 chip has no zero-suppression logic and no readout FIFO, so the trigger rate is limited to less than 100 Hz.

Since the TMC-PHX1 chip implements zero-suppression logic and two levels of data buffer, a TDC module which has higher rate capability can be developed by simply replacing the chip from the TMC-304 to the TMC-PHX1. Furthermore, we replaced on-board DSP chip and CPLDs to latest one to get higher cost performance and better availability.

The photograph of the new TDC module, named TDC-PHX1, is shown in Figure 1, and the block diagram of the module is shown in Figure 2. For handling data transfer and controlling the module, a DSP (TI TMS320LC542) is implemented on the module. A formatted data are stored in a dual-port memory that is accessible both from DSP and VME bus. Interface to the VME bus and TMC chips are realized in two complex PLDs (ALTERA EPM7256A). The VME interface can also handle block transfer mode.

In addition to volatile memories, there is a Flash memory for storing programs and constants. The module also has a serial interface and a JTAG test ports for debugging/programming the DSP and CPLDs.

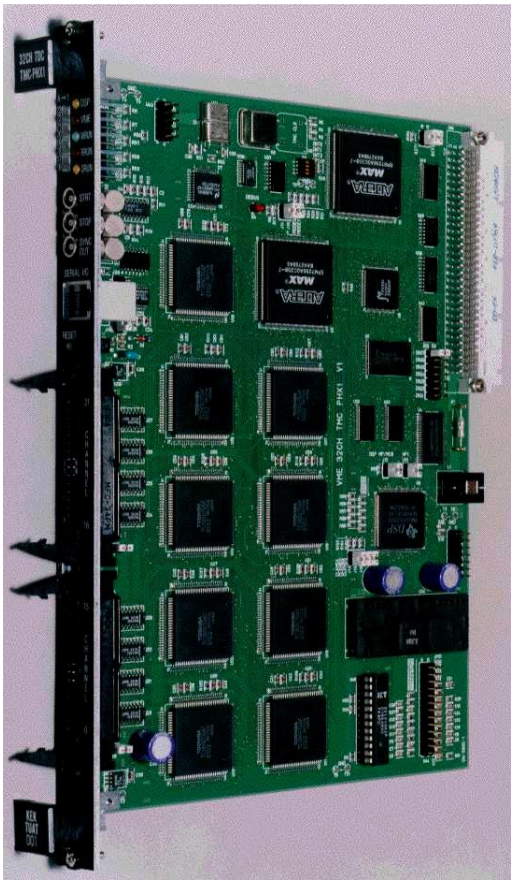

Figure 1. Photograph of the TDC-PHX1 module.

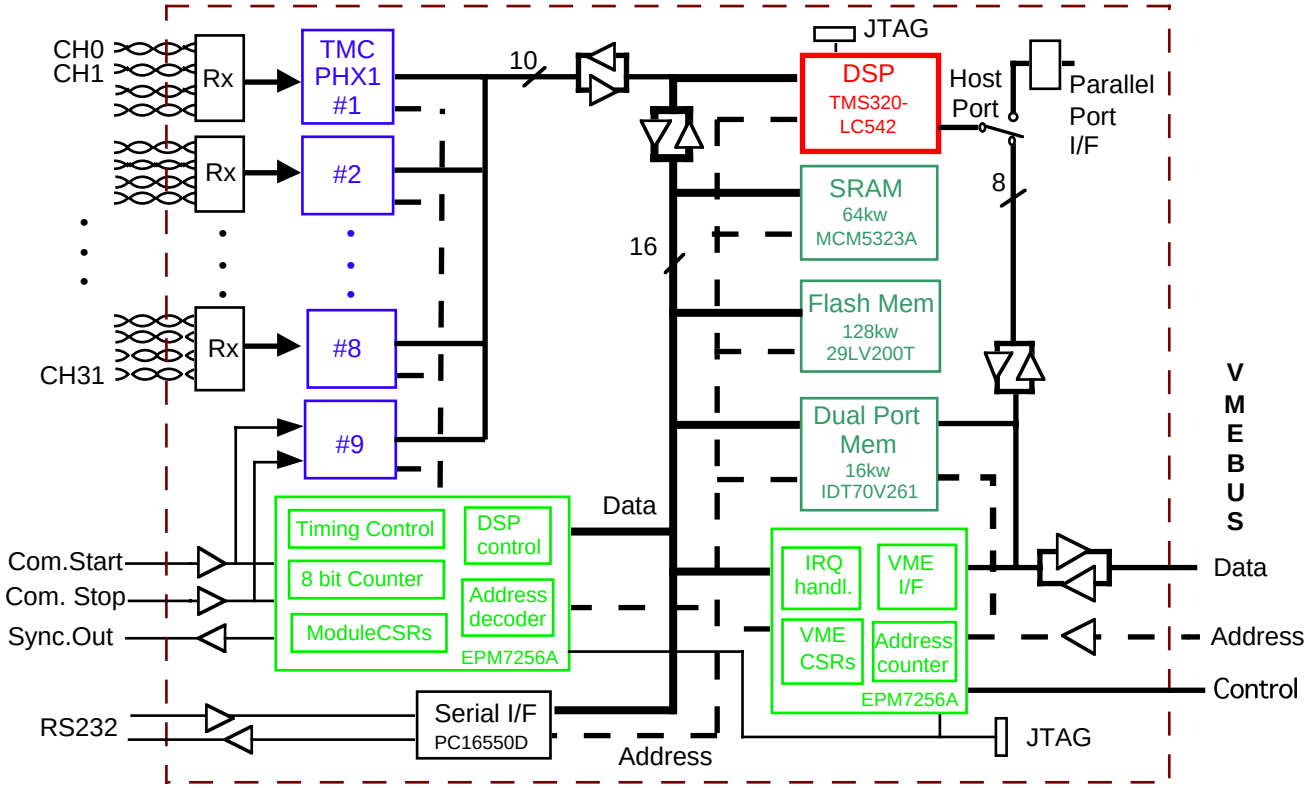

Figure 2. Block diagram of the TDC-PHX1 module.

II. Circuit Design

A. *TMC-PHX1 chip*

Specification of the TMC-PHX1 chip [4] is summarized in Table 1. There are 4 input channels in the chip. Each channel has a TMC core circuit, a PLL, two encoders, a 256-word dual-port memory (L1 buffer) and a 128-word readout FIFO.

The trigger FIFO is 8 words deep. When a trigger occurs, an internal sequencer writes header information and corresponding data to the readout FIFO. Shared data are duplicated during the data transfer. Thus an entire event is reconstructed with header information.

To get a sub-ns time resolution, the TMC core uses an asymmetric ring oscillator which is stabilized with a Phase Locked Loop (PLL) circuit. The taps of the ring oscillator are used to record input signal.

The chip records both leading and trailing edge timings. To get good successive pulse resolution, two encoders are provided covering a half clock cycle (12.5 ns) each. The leading edge timing is digitized in 0.78 ns/bit, and the trailing edge timing (which does not require high-resolution) is digitized with 1.56 ns/bit precision. If both leading and trailing edge occur in the same half cycle, only the leading edge timing is stored.

Table 1. Specification of the TMC-PHX1 chip.

• Least Time Count	0.78 ns/bit (leading edge), 1.56 ns/bit (trailing edge)
• Time Resolution	300 ps rms (leading edge), 500 ps rms (trailing edge)
• Diff./Int. Linearity Error	< 0.1 LSB
• No. of Channels	4 channels
• Level 1 Buffer	256 words (6.4 μs) deep
• Double Pulse Resolution	< 12.5 ns
• Trigger FIFO	8 words deep
• Readout mode	Synchronous or Asynchronous, Zero Suppress mode
• Readout FIFO	128 word deep
• Technology	0.5 μm CMOS Sea-of-Gate Gate-Array 9 mm x 9 mm, 76 k gate used.
• Package	0.8 mm lead pitch, 100-pin plastic QFP

B. *Module Structure*

Specification of the TMC-VME module are summarized in Table 2. We used Texas Instruments TMS320LC542 16 bit fixed-point DSP. It is based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses and performs 40 MIPS at 40 MHz clock. The DSP has three address space: Program, Data, and IO space.

Figure 3 shows the address map of the DSP space.

In addition to the internal 10-kword memory, there are three kinds of external memories; a static memory (50 kword), a dual port memory (16 kword) and a flash memory (128 kword).

The static memory can be accessed with one wait cycle, so it is used as an additional workspace to the internal memory. The dual port memory is mainly used for communication with VME master by exchanging run parameters and data. The flash memory is used as storing a boot program, a data taking program and test programs. It is also possible to store run parameters in this memory. Although the size of the Flash memory is 128 kword, only 16 kword is mapped at a time on DSP data space and VME address space. The mapping selection can be done through a VME control and status register (VCSR).

TMC data consist of two 5-bit data. If the zero-suppression logic is not activated, two 5 bits fine timing is derived from the output. Coarse timing can be calculated from the sequence of the data. If the zero-suppression logic is activated, the fine time plus 8 bit coarse time are derived from the output.

Most of the devices in the module are operated at 3.3 V power supply voltage, which is generated on-board DC-DC converter, except VME interface part. Although both the TMC and the DSP runs at 40 MHz clocks, the clock frequency can be changed independently by replacing crystal oscillators. This eases the selection of timing resolution and faster DSP chip.

The module has a serial (RS-232C) port in a front panel and an 8-bit parallel host port in the VME space and on-board connector. Input signals are received by fast comparators (MAX901) which receive ECL or small differential signals ($> \Delta 100$mV) in a common voltage range of ± 3V.

The bus timing for the various address spaces can be selected individually in the DSP. The DSP internal memory is naturally accessible in no wait cycle, and external memories except the flash memory can be accessed in one wait cycle. Three wait cycles are necessary for accessing the flash memory.

There are several interrupt sources to the DSP. In addition to the interrupt created within the DSP chip (stack error, software interrupt, etc.), the serial port and host port can cause interrupts to the DSP.

For an interrupt to the VME, there is an interrupt signal, which is controlled by the VCSR. This interrupt is provided to communicate with the VME master for handling event data.

Table 2. Specifications of the TMC-VME module

• TMC chip	TMC-PHX1 (40 MHz)
• DSP	TMS320LC542 (40 MHz)
• Static RAM	MCM5323A (64 kword, 50 kword mapped)
• Flash Memory	29LV200T (128 kword, 16kword page)
• Dual-Port Memory	IDT70V261 (16 kword)
• I/O	RS-2323C Serial and 8-bit host port from VME.
• Signal Inputs	32ch (ECL) differential.
• Start/Stop Inputs	NIM level. Lemo connectors.
• VME I/F	P1 connector. A24/D16 Interrupt to/from VME Block transfer
• Packaging	6U x 160mm (double-height, single-width)
• Power Consumption	< 5W (+5V x 1.0 A)

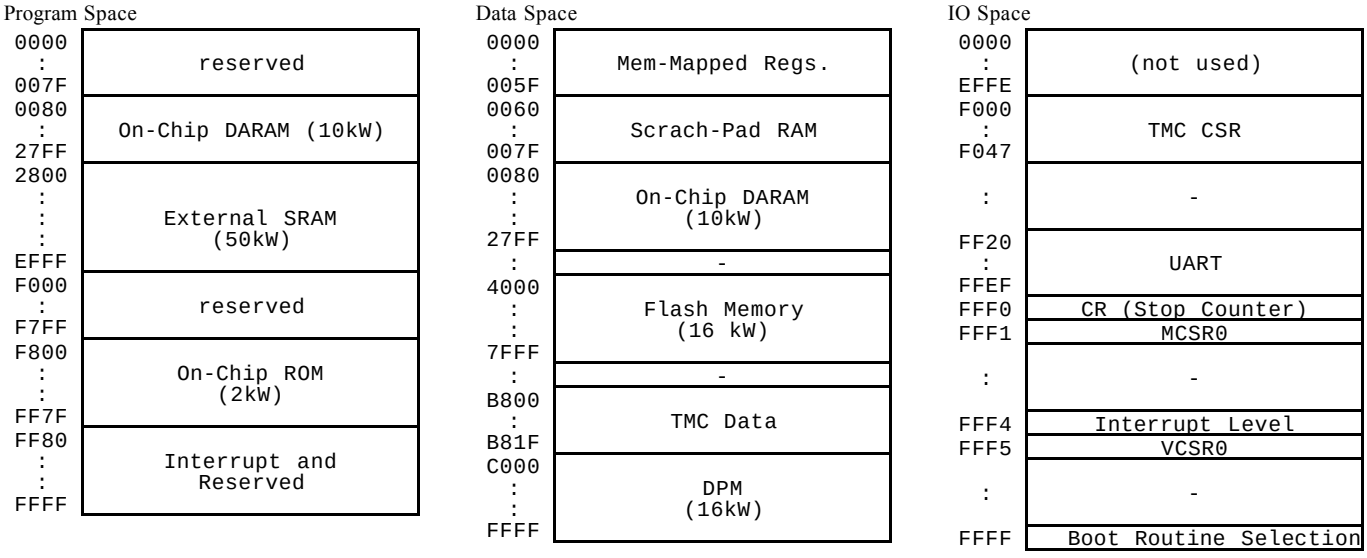

Figure 3. Address map of the DSP space.

C. TMC Interface

TMC interface part is implemented in a CPLD, and functions as a DSP address decoder, a TMC start/stop controller, a module control and status register (MCSR), and a time counter. The CPLD (EPM7256A) has 5000 usable gates, 256 macrocells and 164 I/O pins.

There are 8 TMC chips for 32 channel inputs, and one additional TMC chip for recording start and stop signals.

In a common stop mode, input signals are recorded in the TMC until the common stop signal arrives. In a common start mode, an 8-bit stop counter implemented in the CPLD is used. The counter is decrement for each TMC clock, and the data recording stops when the count reaches zero.

D. VME Interface

The module has an A24/D16 address/data size. Switches for the upper 8-bit address signals (A23 ... A16) set the base address of the module. Thus, the module uses a 16-bit VME address space (64-k byte). The address map of the VME space is shown in Figure 4.

The VME interface is implemented in another CPLD, and has the functions of a VME slave controller, an interrupt handler, a block-transfer controller and a VME control and status register (VCSR). To generate an internal address in the VME block-transfer mode, an 8-bit word counter is implemented. Table 3 shows the bit assignment of the VCSR. A reset signal is asserted by setting the MRST bit of the VCSR. Interrupt is handled with INTM and INTMEN bit. Access to the Flash memory and the host port is controlled with ENFRAM and ENHPI respectively. Mapping of the Flash memory is selected with FRAMx (x=0, 1, 2) bits. This register can be accessed from both DSP and VME.

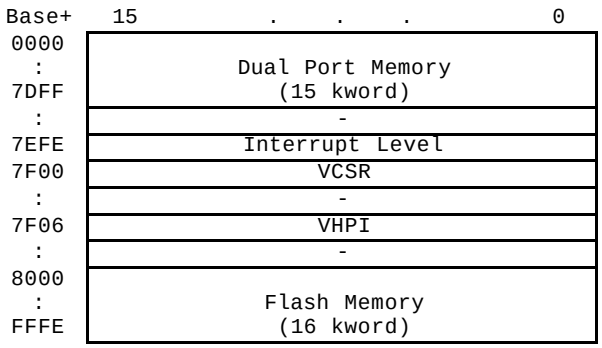

Figure 4. VME-space address map. Switches for the upper 8-bit address bit (A23 .. A16) set the base address. Page of the flash memory can be changed through the VCSR register.

Table 3. VME CSR bit assignment. This register is acceded both from the DSP and the VME.

Bit	from DSP	from VME	Contents	Name
0	R W	R W	0 Module Reset (no latch)	MRST
1	R/W	R/W	INTM Interrupt Status	INTM
2	R/W	R/w	INTM Interrupt Enable	INTMEN
3	R/W	R/W	Enable FRAM access from VME	ENFRAM
4	R/W	R/W	Enable HPI access from VME	ENHPI
3-7	R	R	0	
8	R/W	R/W	FRAM page select 0	FRAM0
9	R/W	R/W	FRAM page select 1	FRAM1
10	R/W	R/W	FRAM page select 2	FRAM2

III. Development System

All the programming and debugging for the DSP and the CPLD are done with a PC.

The CPLD is programmed through on-board JTAG connector which is connected to a printer port of the PC with a special cable. Logics of the CPLD are written in ABEL language and simulated with a Verilog simulator.

To debug the DSP system, the JTAG interface of the DSP is used to control and monitor the DSP operation. We used a PCMCIA JTAG interface card [6], and a development system software [7]. The development system can control and monitor the DSP, and displays the contents of DSP registers and memories.

All the software until now is written in assembler language, but C language is also available.

IV. Status and Prospect

Most of the hardware components are checked and the DSP is booted and successfully running. However, programs are not yet fully developed and high rate data taking test are not yet done.

Although the TMC chip is designed to operate without any deadtime, the TDC module has some limitation in bandwidth of the data transfer at the internal bus and the VME bus.

Since the TMC-PHX1 has two buffers inside, and the module has another buffer (dual port memory), the deadtime will not reveal until these buffer becomes full.

Thus the new module could be used in higher rate experiment than the previous module. In addition, the cost of TMC and DSP chips are reduced much compared with those of the previous module. Thus the price of the module can be lowered significantly in a mass production.

VI. Acknowledgments

We wish to thank to Y. Suzuki and M. Sagara of AMSC Co. for their technical support to the module development.

VII. References

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