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Time Memory Cell VLSI for the PHENIX Drift Chamber

Y. Arai[1], M. Ikeno[1], M. Sagara[2] and T. Emura[2]
[1]KEK, National High Energy Accelerator Research Organization,
Institute of Particle and Nuclear Studies, Tsukuba, Ibaraki 305, JAPAN
[2]Tokyo University of Agriculture and Technology, Koganei, Tokyo 184, JAPAN

Abstract

A high-precision Time-to-Digital-Converter VLSI, TMC-PHX1, was developed for the PHENIX drift chamber. The chip contains 4 channels of TDC with two stages of data buffering and one level of trigger buffering required in very high rate experiments. In addition to a fixed data size readout, the chip also supports a zero-suppression mode readout.

The chip records both rising and falling edge timings, and has a least timing count of 0.83 ns/bit and 1.66 ns/bit respectively. A level 1 buffer has a recording depth of 6.8 μsec and a readout FIFO has a depth of 128 words. High precision timing was derived from an asymmetric ring oscillator stabilized with a PLL. The chip runs at 4 times faster clock (37.6 MHz) of the RHIC bunch clock, and was fabricated with 0.5 μm CMOS gate-array technology.

I. Introduction

A high-precision and dead time less Time-to-Digital Converters (TDCs) are widely required in recent high-energy and nuclear physics experiments. We have established a high-resolution CMOS TDC technique with self-calibrating Delay Locked Loop (DLL) and Phase Locked Loop (PLL) circuits. We developed several custom TDC LSIs called Time Memory Cell (TMC) [1, 2, 3] and VME modules [4, 5]. After our circuit had proven its effectiveness, it triggered developments of similar CMOS TDC circuits by many groups [6, 7, 8].

The performance of the TMC LSI is well matched to the requirements of the drift chamber readout of the PHENIX experiment at the RHIC accelerator. However, the PHENIX experiment is more demanding on two track separation and multi-trigger capability to accommodate its very high rate and a large multiplicity environment caused by the heavy ion collisions. It also requires longer buffer length and two stages of data buffering to reduce cost, power and the area for the frontend electronics.

A new TMC chip, TMC-PHX1, was developed for the PHENIX drift chamber readout based on the existing TMC architecture. Since the TMC chip was designed using a gate-array technology, modification of the circuit is relatively easy. The new chip contains 4 channels in a chip, and records both leading and trailing edge timing. The chip implements two levels of data buffering; a Level 1 (L1) buffer and a readout FIFO. Trigger information is also buffered in trigger FIFO to eliminate dead time when multiple triggers occur in a short period. Shared data for two or more triggered events are duplicated during a data transfer from the L1 buffer to the readout FIFO.

The chip runs at 4-times faster clock speed (37.6 MHz) than the RHIC bunch crossing frequency. Although the PHENIX experiment uses only fixed-size data readout mode, the chip also supports a zero-suppression readout mode. The chip was fabricated in a 0.5 μm CMOS gate-array technology and packaged in a 100-pin plastic QFP.

II. System Consideration

The PHENIX online system is designed to be a fully pipelined dead time less system. The system basically runs at the 9.4 MHz beam crossing frequency, and some of the electronics runs at a multiple of the 9.4 MHz. The system is able to read out data at a maximum Level 1 trigger rate of 25 kHz, and the trigger latency is 40 beam crossing (4.24 μsec). Maximun hit rate of a channel of the drift chamber is expected to be ~2.5 kHz.

The frontend electronics must keep the data for the trigger latency time, and buffer up to 5 Level 1-accepted events waiting for readout. Since the beam crossing time (106 ns) is shorter than the maximum drift time (460 ns), shared data in two or more successive triggers must be duplicated to build an event.

To get double track separation better than 1.5 mm, the TDC must have double pulse resolution of better than 30 ns. Furthermore, to help pattern recognition, trailing edge timing must be measured in addition to the leading edge timing measurement. The DAQ system requires event data to be assembled into one data block for post processing.

The specification of the TMC-PHX1 chip is shown in Table 1. An internal clock is generated from a PLL circuit. The internal clock frequency can be either the same or 4 times higher than the external clock.

The chip has a level 1 buffer of 256 words (6.8 μs = 64 beam crossing). As described above, the chip must store up to 5 events. Since data in the L1 buffer are moved to the readout FIFO right after receiving a trigger signal, 256 words are sufficient for handling the 5 events in the chip. The depth of the readout FIFO is 128 words which is also sufficient for keeping 5 events (each event needs a header word and 20 data words).

The trigger FIFO is 8 words deep. Shared data are duplicated during the data transfer from the L1 buffer to the readout FIFO.

Thus an entire event is reconstructed with header information. When a readout occurs, an internal sequencer sends out header information and channel data.

The chip records both leading and trailing edge timings. To get good successive pulse resolution, two encoders are provided covering a half clock cycle (13 ns) each. The leading edge timing is digitized in 0.83 ns/bit (300 ps rms resolution), and the trailing edge timing (which does not require high-resolution) is digitized with 1.66 ns/bit precision. If both leading and trailing edge occur in the same half cycle, only the leading edge timing is stored.

Table 1. Specification of the TMC-PHX1 chip that runs at 37.6 MHz (4-times RHIC) clock

• Least Time Count	0.83 ns/bit (leading edge), 1.66 ns/bit (trailing edge)
• Time Resolution	300 ps rms (leading edge), 500 ps rms (trailing edge)
• Input signal level	Single-end or Differential (clock and channel input) / CMOS level (other signals)
• Diff./Int. Linearity Error	< 0.1 LSB
• External Clock	10 - 40 MHz (x1 mode) 2.5 - 10 MHz (x4 mode)
• No. of Channels	4 channels
• Level 1 Buffer	256 words (6.8 μs @37.6 MHz) deep
• Double Pulse Resolution	< 14 ns
• Trigger FIFO	8 words deep
• Readout mode	Synchronous or Asynchronous, Zero Suppress mode (optional).
• Readout FIFO	128 words deep
• Supply Voltage	3.0 ~ 3.7 V
• Technology	0.5 μm CMOS Sea-of-Gate Gate-Array 9 mm x 9 mm, 76 k gate used.
• Package	0.8 mm lead pitch, 100-pin plastic QFP

III. Circuit Description

A. Circuit Block

A Block diagram of the TMC-PHX1 is shown in Figure 1 and a photograph of the chip is shown in Figure 2. There are 4 input channels in the chip. Each channel has a TMC core circuit, a PLL, two encoders, a 256-word dual-port memory (L1 buffer) and a 128 words readout FIFO.

Signal levels for time-critical inputs (system clock and channel inputs) is selectable to be either single-ended or differential (ΔV_{in} > 200 mV, 1.4 V < V_{center} < 2.4 V). There are 8 Control-and-Status Registers (CSRs) which can be accessed through an 8-bit control bus.

To control various operations, 4 sequencers are implemented; a write sequencer, a trigger sequencer, a readout sequencer and an output sequencer. These sequencers run at the internal clock frequency except the output sequencer which runs at the speed of an external signal.

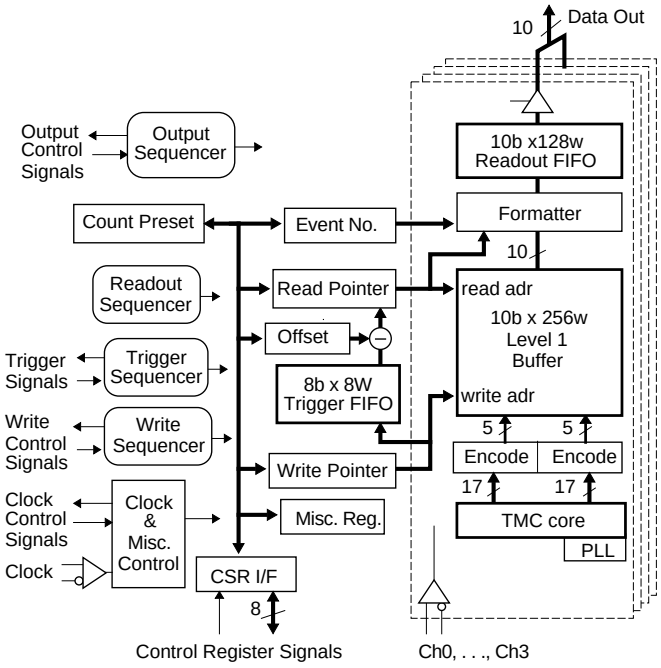

Figure 1: Block diagram of the TMC-PHX1 chip.

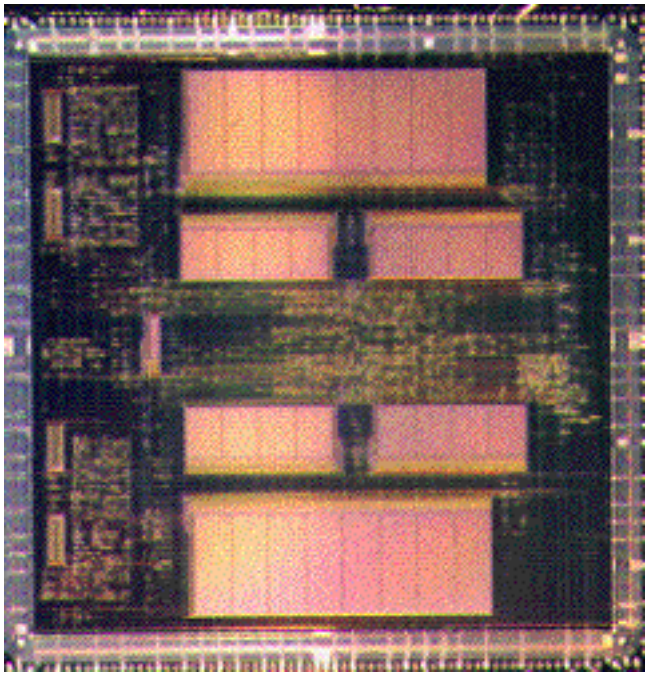

Figure 2: Photograph of the TMC-PHX1 chip. Four small rectangular areas at left side are the TMC core cells. Two large rectangular areas are the L1 buffers, each of which is shared by two channels. Four rectangular areas at center are the readout FIFOs.

B. Digitization and Data recording

In each clock cycle, the input signal is digitized in a TMC

core circuit, then the digitized data are stored in the L1 buffer after synchronization and encoding stages as shown in Figure 3. Since the outputs of the filp flops change at every 0.8 ns, the synchronization stage, which delay the timing of half of bits, is implemented [3] to latch the outputs stably.

The L1 buffer is made of a dual port memory and works as a pseudo-FIFO. Write and read operation can be performed at the same time so that there is no dead time for readout.

After receiving a trigger signal, the corresponding data set is moved from the L1 buffer to the readout FIFO.

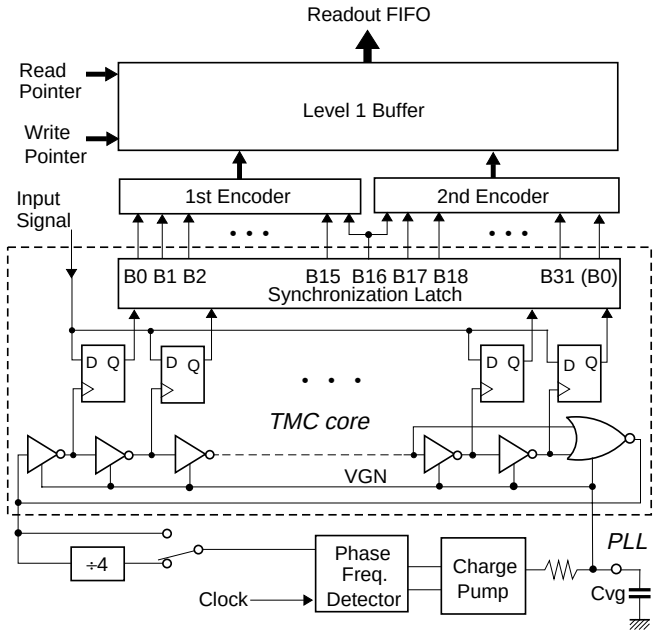

Figure 3: Block diagram of the digitizer, encoders and data recording sections.

C. TMC Core Circuit

The TMC core circuit consists of an asymmetric ring oscillator, flip flops and a synchronization stage. Only this part is laid out manually to achieve high precision timing. The circuit is almost the same as that used in the TMC-TEG3 chip [3]. Small modifications in layout were done to get better differential non-linearity. In addition, a method to halt the oscillation for measuring quiescent current of the device was implemented.

The schematic of the asymmetric ring oscillator [9] and its timing diagram are shown in Figure 4 (a) and Figure 4 (b) respectively. Normally a ring oscillator is composed of odd number of inverter stages. As shown in the timing diagram in Figure 4 (b), the asymmetric ring oscillator can generate 32 equally spaced timings (Ttap). Two switches (S1 and S2) are inserted in a delay control voltage (VGN) line to halt the oscillation. This eliminates an additional gate in the oscillation loop, and keep the circuit in very orderly structure that nicely fits to the gate-array technology.

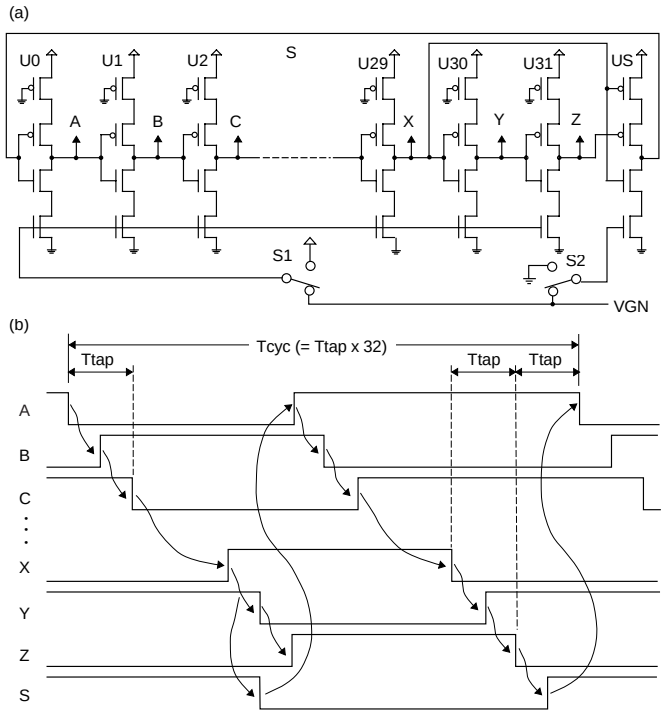

Figure 4: (a) Schematic of the asymmetric ring oscillator, (b) timing diagram of the ring oscillator.

Table 2. Data Encoding Scheme

TMC Out (0 1 2 3 4 5 ••• 13 14 15 16 / (16 17 18 19 20 21 ••• 29 30 31 0*)	Encoded Data (4 3 2 1 0)	Comment
0 0 0 0 0 0 ••• 0 0 0 0	0 0 0 0 0	All 0
1 1 1 1 1 1 ••• 1 1 1 1	0 0 0 0 1	All 1
	0 0 0 1 0	Header ID
	0 0 0 1 1	(not used)
	0 0 1 0 0	(not used)
	0 0 1 0 1	(not used)
	0 0 1 1 0	End of Data
	0 0 1 1 1	Data ERROR
	(8 codes)	Trailing edge
1 x 0 0 0 0 ••• 0 0 0 0	0 1 0 0 0	between bit 0 and 2
1 1 1 x 0 0 ••• 0 0 0 0	0 1 0 0 1	between bit 2 and 4
1 1 1 1 1 x ••• 0 0 0 0	0 1 0 1 0	between bit 4 and 6
: : : : : : : : : : :	:	
1 1 1 1 1 1 ••• x 0 0 0	0 1 1 1 0	between bit 12 and 14
1 1 1 1 1 1 ••• 1 1 x 0	0 1 1 1 1	between bit 14 and 16
	(16 codes)	Leading edge
0 1 x x x x ••• x x x x	1 0 0 0 0	between bit 0 and 1
0 0 1 x x x ••• x x x x	1 0 0 0 1	between bit 1 and 2
0 0 0 1 x x ••• x x x x	1 0 0 1 0	between bit 2 and 3
: : : : : : : : : : :	:	
0 0 0 0 0 0 ••• 0 1 1 x	1 1 1 0 1	between bit 13 and 14
0 0 0 0 0 0 ••• 0 0 1 x	1 1 1 1 0	between bit 14 and 15
0 0 0 0 0 0 ••• 0 0 0 1	1 1 1 1 1	between bit 15 and 16

x = don't care. (*) bit 0 of one cycle later.

D. Data Encoding

The 32-bit output of the TMC is divided into two 17 bits data. Not to miss the signal transition at the boundary of encoders, 16 bits plus one next bit is provided to the encoders. Each 17-bit data is encoded into a 5-bit code as shown in Table 2.

For the case of a 0 to 1 (leading edge) transition in the 17 bits, the first transition point is encoded into 16 different codes. Other transitions after the first edge are ignored. (see Table 1)

In the case of a 1 to 0 (trailing edge) transition in the 17 bits, only one transition point is encoded into 8 different codes. For wire chamber applications, the trailing edge timing is much worse than the rising edge timing. Therefore less number of codes for the trailing edge timing are assigned to reduce data size.

In the remaining 8 codes, 5 codes are assigned to represent "All 0", "All 1", "Header ID", "End of Data" and "Data Error" conditions, and 3 codes are not used.

E. Trigger and Readout

When a trigger signal is received by the chip, a write pointer value is loaded in to the trigger FIFO. The trigger FIFO status is checked by the readout sequencer in each clock cycle. If the trigger FIFO is not empty, a data transfer cycle will start. At first, the read pointer is set to the trigger FIFO value minus offset value. This offset corresponds to the trigger latency.

Then a header word is written to the readout FIFO (see Figure 5). Each channel gets a unique header word, so that there are 4 different header words. Finally, data pointed to by the read pointer are pushed to the readout FIFO. In the fixed data size mode, a fixed number of data words set in the Count Preset register are moved. Each data word is transferred in one clock cycle and contains two 5-bit data words (1st and 2nd encoder output).

If zero suppression mode is selected, only data which has a transition-timing information is transferred to the readout FIFO. For each transition, both a recorded value (fine time) and a read pointer value (coarse time) are pushed to the readout FIFO.

There are two external readout modes; asynchronous and synchronous mode. In the asynchronous mode, timing is fully controlled with external input signals and the readout FIFO absorb the timing difference.

In the synchronous mode, readout proceeds sequentially from channel 0 through channel 3 controlled by the output sequencer. The data stream in the synchronous mode is also shown in Figure 5. The timing is synchronous to an output clock signal. Although the output clock signal can be different from the internal clock, same 37.6 MHz clock will be used for PHENIX readout.

G. Control Registers

There are eight Control and Status Registers (CSRs) which set/show the operating conditions. Bit assignments for the registers are shown in Table 3. Brief description of the registers is given below.

CSR0 : Offset Register. The offset value stored in this register is used to calculate the read out position from the trigger FIFO data. Conceptually, this corresponds to the trigger latency.

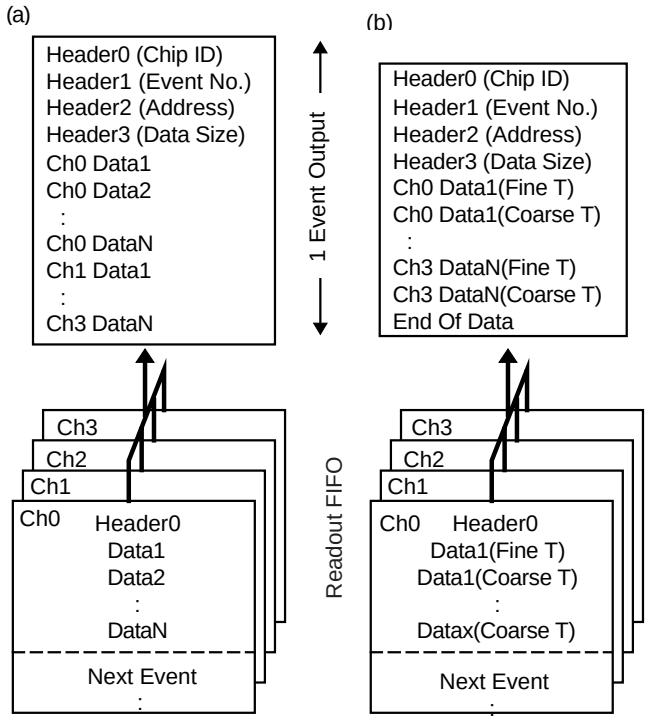

Figure 5: Contents of the readout FIFO and Output Data stream in the synchronous readout mode. (a) Fixed data size mode, (b) Zero Suppress mode.

CSR1 : Read Pointer Register. Read pointer is an 8-bit up-counter storing an address of the read(write) port of the L1 buffer. This register is automatically set to an event position when a trigger is asserted.

CSR2 : Write-Pointer Register. Write pointer is an 8-bit up-counter storing an address of the write port of the L1 buffer. During measurement, this register value is automatically incremented in each cycle.

CSR3 : Count-Preset Register. This register contains the number of data words to be written to the readout FIFO.

CSR4 : Event Number Register. This 8 bits register keeps an event number. The event number is a part of the header data and incremented on each trigger. In a test mode, this register is also used to count the PLL oscillation. After a prefixed time of PLL free running, the content of the register is compared with an expected value.

CSR5&6 : Miscellaneous control. These registers contain option, status, 5-bit Chip ID, and test bits.

CSR7 : Test Data Register. Lower 5 bits of this register is duplex and selected by ENTDR bit. ENCH0~3 are used to enable/disable each channel. Other bits are used for chip test. The test data register is used to write and read test patterns to/from internal memories.

Table 3 Bit assignment of CSR

bit	7	6	5	4	3	2	1	0
CSR0	Offset Register							
CSR1	Read Pointer Register							
CSR2	Write Pointer Register							
CSR3	Count Preset Register							
CSR4	Event Number Register							
CSR5	DPMER	OFIFUL	TFIFUL	-	ZSUPP	BYPFIFO	ENWPUP	ENTDR
CSR6	SOUT	SIN	SHIFT	Chip ID Register				
CSR7 ENTDR=0	SELH	TCH1	TCH0	ENOSC	ENCH3	ENCH2	ENCH1	ENCH0
ENTDR=1				Test Data Register				

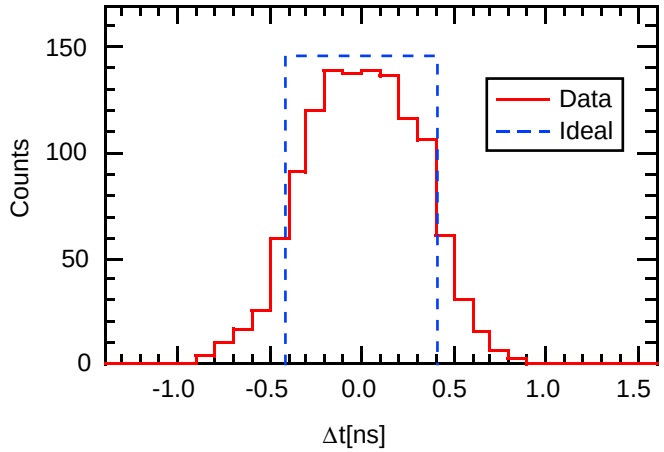

Figure 6: Time-resolution measurement of the TMC-PHX1 at 37.6MHz. RMS value of the data is 305 ps which includes a measurement error of ~100 ps.

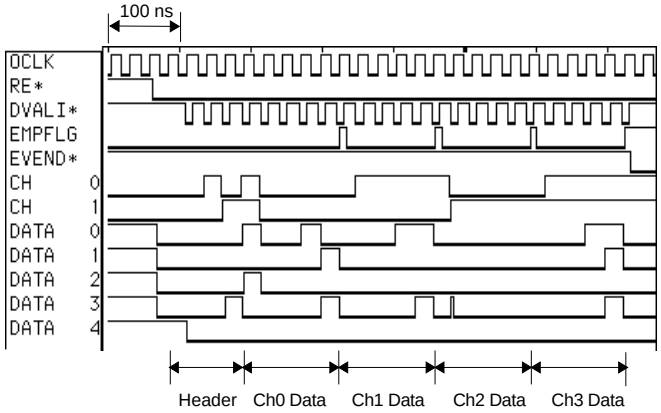

Figure 7: An example of the synchronous readout timing. Preset count is 5 words, the output clock (OCLK) is 37.6 MHz.

IV. Test Results

All functions are confirmed to work in a test setup, and the test results agreed with our simulation results. Result of a time resolution measurement is shown in Figure 6. RMS value of the data is 305 ps which includes a measurement error of ~100 ps, thus the timing resolution of the chip is less than 300 ps. An example of the synchronous readout timing is shown in Figure 7.

The power consumption of the chip depends on the input rate, trigger rate, and readout rate. Normally, the power consumption is around 50 mW/channel and goes up to 100 mW/channel in a very heavy trigger/input rate condition.

IV. Summary

A new time-to-digital converter chip, TMC-PHX1, was designed and tested which is a modified version of the TMC-TEG3 chip. In addition to the same high performance as of the previous TMC chips, it has a factor of two larger buffer depth and additional readout FIFOs. Furthermore, it has a capability to handle multiple triggers.

These extended capabilities will be very useful in high rate experiment such as PHENIX.

V. Acknowledgments

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VI. References

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