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# Development of a New TDC LSI and a VME Module

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**Abstract--A new TDC LSI and a TDC VME module have been developed. The TDC LSI (called AMT-2) is developed for precision muon trackers of the ATLAS experiment. The AMT-2 chip has 24 input channels and 280 ps RMS resolution. It is processed using 0.3 μm CMOS technology.**

**The TDC module (called AMT-VME) has 64 channels and a wide timing range (~100 μsec) with a 0.78 ns/bit timing resolution. The module also contains a DSP for controlling data acquisition and manipulating data. Acquired data is read out through the VME bus via a dual-port memory bank.**

**The designs of the chip and the module are presented, and a test result is shown.**

## I. Introduction

A high-precision deadtime-less Time-to-Digital Converter (TDC) module is a common instrument in recent high-energy and nuclear physics experiments.

In the past, we developed a high-performance TDC LSI (TMC304 [1]) and a TDC VME module (TMC-VME [2]). They have been widely used in many experiments. However, the ICs used in the module are already difficult to obtain since most of them become obsolete. Furthermore, there are more demanding requests for a higher trigger rate, a longer time range and lower cost.

On the other hand, a new TDC LSI (AMT: ATLAS Muon TDC [3, 4, 5]) has been developed for a precision muon tracking detector (MDT) of the ATLAS experiment. The development project was started in collaboration with CERN microelectronics group in 1996. After the common architecture study, both group designed their own chips; CERN group put emphasis on higher precision with full custom design [6], while we put emphasis on mass production and lower cost with gate-array technology.

Although the mass production of the AMT chip has not yet started, a working chip is already available. We have thus started a new TDC module development project using the AMT-2 chip. Although the design of the module is totally new with enhanced performance, we tried to keep compatibility with the TMC-VME module as much as possible.

The AMT chip was developed using a 0.3 μm CMOS Gate-Array technology (TC220G, Toshiba Co.). It contains 24 input channels, a 256-word level-1 buffer, an 8-word trigger FIFO and a 64-word readout FIFO. Both leading and trailing edge timings can be recorded. The recorded data is matched to the trigger signal timing, and only matched data is transferred to the output. By using an asymmetric ring oscillator [1] and a Phase Locked Loop (PLL) circuit, it achieves a 280 ps RMS timing resolution.

Due to the new AMT-2 chip, the AMT-VME module has a wider timing range (~100 μsec; the previous module has 4 μsec) and high density (64 ch/module; previous 32 ch/module). Furthermore, we expect the cost per channel to be greatly reduced.

Photographs of the chip and the module are shown in Fig. 1, and a block diagram of the module is shown in Fig. 2. For manipulating data and controlling data acquisition, a DSP (Digital Signal Processor, TI TMS320VC5402) is implemented on the module. Formatted data is stored in dual-port memories that are accessible both from the DSP and the VME bus. Interface to the VME bus and AMT chips are realized in two complex PLDs. The VME interface can also handle the block-transfer mode.

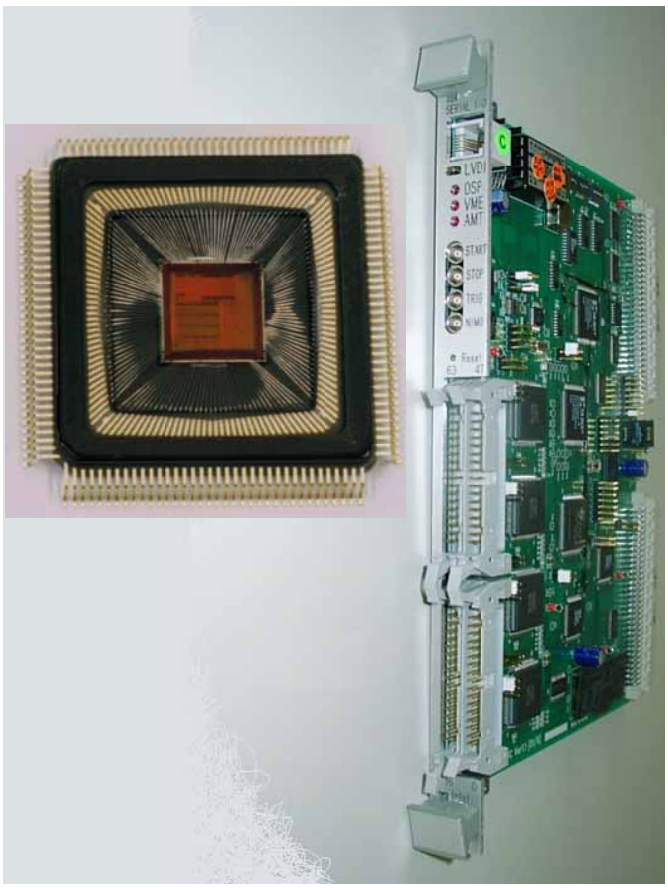


Fig. 1. Photograph of the AMT-2 chip and the AMT-VME module.

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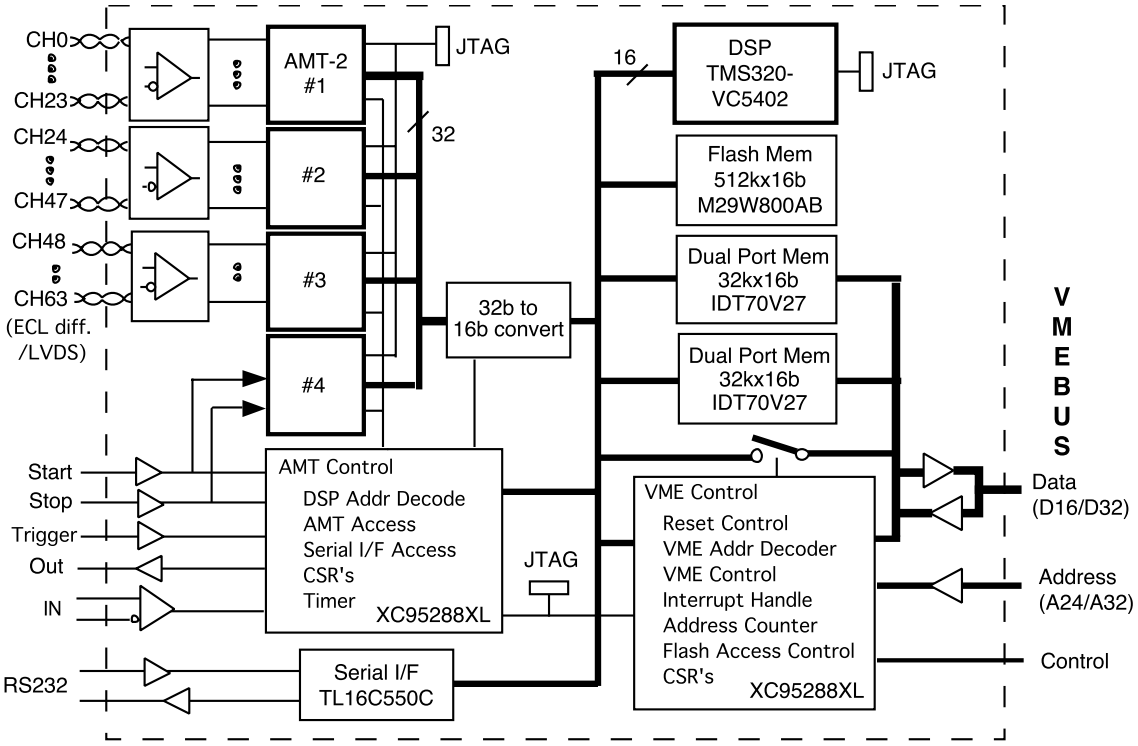


Fig. 2. Block diagram of the AMT-VME module.

## II. The AMT-2 Chip

A block diagram of the AMT-2 chip is shown in Fig. 3, and the specifications of the chip are summarized in Table I.

The asymmetric ring oscillator produces a double-frequency clock (80 MHz) from a 40 MHz clock. By dividing the 12.5 ns clock period into 16 intervals in the oscillator, a time bin size of 0.78125 ns is obtained.

A hit input signal is used to store fine and coarse time measurements in individual channel buffers. The time of both the leading and trailing edges of the hit signal (or leading edge time and pulse width) can be stored. Each channel has a 4-word buffer where measurements are stored until they can be written into the common level 1 (L1) buffer.

The L1 buffer is 256 hit deep and it is written in a circular buffer fashion. Reading from the buffer is by random access such that the trigger matching can search for data belongings to the received triggers.

Trigger matching is performed as a time match between a trigger time tag and the time measurements themselves. The trigger time tag is taken from the trigger FIFO and the time measurements are taken from the L1 buffer. Hits matching the trigger are passed to the read-out FIFO. As an option, the trigger matching can be disabled. In this case, all of the recorded data will be transferred to the read-out FIFO.

Both serial and 32-bit parallel output ports have been implemented in the AMT-2 chip. In the ATLAS experiment, where the chip is attached to a detector, the serial output is used. In the AMT-VME module, the parallel output port is used.

The jitter of the ring oscillator was measured based on the time distribution between the input clock edge and the PLL clock edge (Fig. 4). The jitter at the operating point (3.3V, 80MHz) is 150 ps RMS. This value is sufficiently low compared with a digitization error of 225 ps. The total timing resolution for a single edge measurement is about 280 ps. Fig. 5 shows the jitter variation to the oscillating frequency (Fosc) and the power supply voltage (Vdd). This indicates sufficient margins around the operating point.

Table I. Specification of the AMT-2 chip.
(values are for a clock frequency of 40MHz).

| | |
|---|---|
| LSB Count | 0.78125 ns/bit (rising and falling edge) |
| Time Resolution | 280 ps RMS |
| Dynamic range | 13 (coarse) + 4 (fine) = 17 bit |
| Max. Trigger Latency | 16 bit (51 μs) |
| Int./Diff. Non Linearity | < 80 ps RMS |
| No. of Channels | 24 Channels |
| Level 1Buffer | 256 words |
| Read-out FIFO | 64 words |
| Trigger FIFO | 8 words |
| Double Hit Resolution | <10 ns |
| Data Output | Serial (10-80 Mbps) or 32-bit parallel |
| Hit Efficiency | 100% @400 kHz (single edge)<br>>99.8%@400kHz(two edges) |
| Hit Input Level | LVDS |
| CSR access | JTAG or 12 bit control bus. |
| Power | 3.3+-0.3V, ~360 mW |
| Process | 0.3 μm CMOS Sea-of-Gate.<br>110 k gates used. |
| Package | 144 pin plastic QFP |

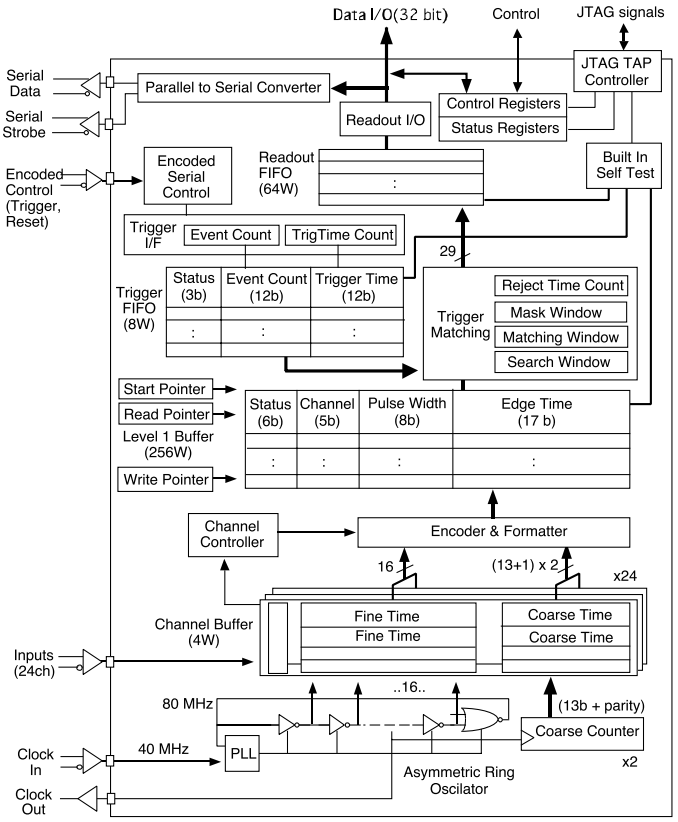


Fig. 3. Block diagram of the AMT-2 chip.

## III. Module Structure

The specifications of the AMT-VME module are summarized in Table II. We used a 16-bit fixed-point DSP clocked at 20 MHz. An on-chip PLL generates the 100 MHz internal clock used by the processor. Several registers are implemented to control and show the status of the module. Some of the registers are accessible both from the DSP and the VME

### *A. Memories*

In addition to a DSP internal 16-kword memory, there are two kinds of external memories: a dual-port memory (32 k x 16 bit x 2) and a flash memory (512 k x 16bit).

The dual-port memory is used mainly as a data buffer between the DSP and a VME master. The flash memory can be used for storing a boot loader and data-taking programs, test programs and experimental settings. This memory can be accessed from both the DSP and the VME.

### *B. External I/O*

The module has a serial (RS-232C) port, general-purpose NIM output and a LVDS input in addition to a Start, Stop and Trigger inputs (NIM level) in a front panel. Those general-purpose I/Os are connected to a CPLD, and are programmed depending on the experimental requirements.

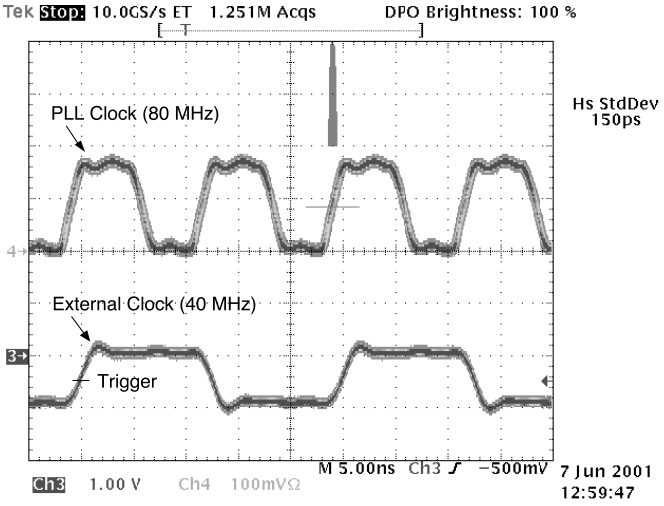


Fig. 4. PLL clock output waveform and jitter measurement. PLL clock jitter was measured relative to the external clock edge.

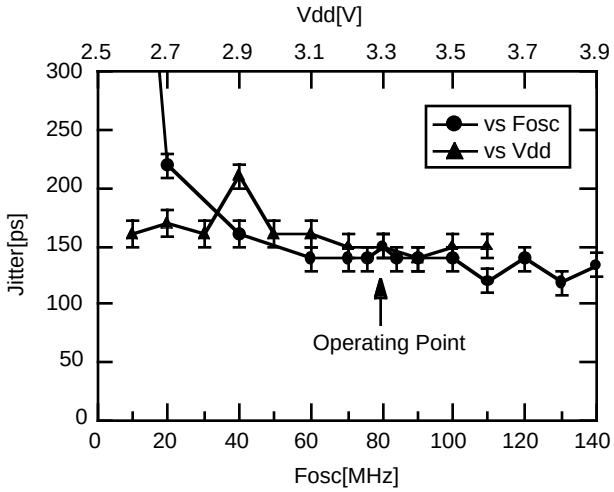


Fig. 5. PLL jitter vs. internal clock frequency and supply voltage. The operating point is shown by the arrow.

Although the AMT-2 has LVDS inputs for hit signals, separate differential receivers (SN65LVDT32B) are used to accommodate both the ECL differential and the LVDS signals and to protect AMT-2 chips from external damage. One of the LVDS pin of the AMT-2 is fixed to 1.6 V and the other pin is connected to the receiver output through 270 ohm resistor. The receiver can accept differential signals with more than 100mV amplitude in a common voltage range between -2V to 4.4V.

### *C. AMT Control*

The AMT control part and the DSP address decoder are implemented in a CPLD. It also contains a 12-bit timer, which is used in the common start mode.

There are 4 AMT-2 chips in the board. Three of them are used for recording the 64-channel input (remaining 8 channels are not used), and one additional AMT chip is used for recording start and stop signals only. This special AMT for start/stop recording ease the control of data acquisition.

Table II. Specifications of the AMT-VME module.

| | |
|---|---|
| TDC chip | AMT-2 (40 MHz) x 4 |
| DSP | TMS320VC5402 (100 MHz) |
| Flash Memory | M29W800AB(512k x 16b) |
| Dual-Port Memory | IDT70V27 x 2 (32 k x 16b x 2) |
| I/O | RS-2323C Serial, NIM output, LVDS input, NIM inputs (Start, Stop and Trigger) |
| Signal Inputs | 64ch differential. (ΔV>100mV @-2 ~ 4.4V) 16 ch x 4 connectors. |
| Timing resolution | ~380 ps. for 0-1 μsec delay |
| VME I/F | A24/A32, D16/D32<br>Interrupt to/from VME<br>Block transfer |
| Packaging | 6U x 160mm (double-height, single-width) |
| Power Consumption | 9W (+5V x 1.8 A) |

Since the AMT-2 output data width is 32 bits, while the DSP has only a 16-bit data bus, shadow registers are implemented to convert the 32 bits data to 16-bit words requiring two clock cycle.

In a common stop mode, input signals are recorded in the AMT-2 until a common stop signal arrives. In a common start mode, the 12-bit stop counter determines the length of the recorded time window. The start and stop signals are connected to trigger inputs of the AMT LSIs so that only matched data can be transferred outside.

On the other hand, continuous mode where all hit timing are stored is also supported. Furthermore it is also possible take data before start or after stop like an logic analyzer since the AMT-2 is continuously running.

### *D. VME Interface*

The module is accessed with the A24 or A32 address mode, while the module uses an internal address space of 19 bits. The dual-port memory is accessed with the D16 or D32 mode, and the flash memory and the internal registers are accessed by only the D16 mode. Block transfer is supported in addition to a single transfer mode.

The VME interface is implemented in another CPLD, and has the functions of a VME slave controller, an interrupt handler, a block-transfer controller and so on. To generate an internal address in the VME block-transfer mode, an 8-bit word counter is provided.

### *E. Power*

The module works with a 5V single supply. Several kinds of voltages are generated within the module with DC-DC converters and linear regulators. Most of the devices are operated at 3.3 V, while the DSP uses 1.8 V and the NIM level signal requires -5.2 V. The total current drawn by the module is about 1.8 A at 5 V.

## IV. TEST RESULTS

Ten modules were produced, and debugging of the DSP was successfully done through the JTAG port and a commercial emulator software. Module control program of the DSP was developed in C language. The program continuously checks parameter block of the dual-port memory, and if a new parameter(command) is written a job is performed depending on the command. These parameter setting can be done both from VME bus and the serial port. Output data from AMTs are stored in the dual-port memory as a circular multi-event buffer.

Timing resolution was measured by using HP5359A Time Synthesizer. A VME master module set delay time and issues a trigger command to the Time Synthesizer through a GP-IB interface. Recorded data is read through the VME bus.

Below we show an example of data measured in a common start mode and leading edge time measurement. Delay between the start signal and hit signal ranges from 0 ns to 1000 ns in 0.1 ns step. The acquired data is fit by a line. A part of the residual distribution is shown in Fig. 6. In every 7 ~8 points, an regular structure which reveals the digitization error can be seen .

Histogram of the residual data is shown Fig. 7. The RMS value of the data distribution is 380 ps. Since both start and hit signals are asynchronous to the AMT-2 clock, the ideal distribution, which only includes the digitization error, becomes triangular shape.

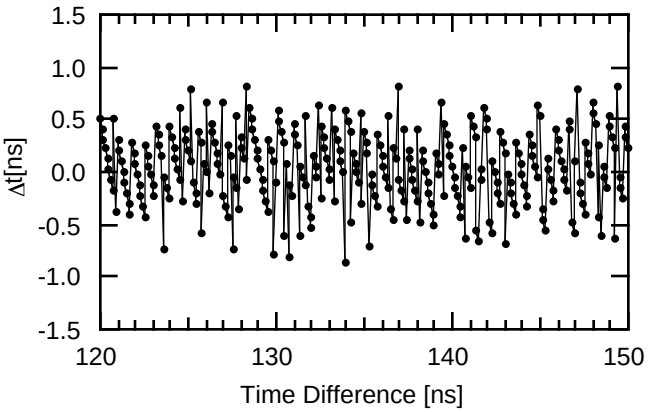


Fig. 6. Residual from a line fit. Data are taken in 0.1 ns step. A regular structure of digitization error (every 7~8 points) can be seen.

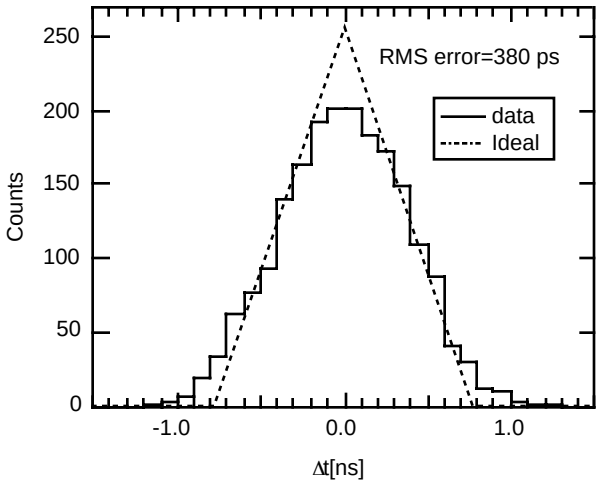


Fig. 7. Result of a time-resolution measurement (Time difference measurement between start and hit). Delay time between two pulses ranges from 0 ns to 1000ns in 0.1 ns step and fit by a line. The RMS error of the data is 380 ps. The dashed line shows ideal case distribution (digitization error only). The single-measurement error was derived to be about 270 ps.

The RMS error is a combination of two measurement (start and hit) errors. Assuming a Gaussian distribution of the errors, a single measurement error is obtained as 270 ps by dividing it by √2. This value is consistent with the AMT-2 timing resolution of 280 ps. Note that the main source of this error come from a digitization error of 225 ps (= 1 LSB / √12).

Almost same results are also obtained for other modes (common stop, falling edge time measurement etc.). However, the resolution becomes a little bit worse (~420 ns) for longer time range (~50 μsec) measurement. We are not sure main source of the increased error is caused by instrumentation or the module.

## V. CONCLUSION

We have developed a new TDC module using a new TDC chip which is developed for the ATLAS experiment. The module has adequate resolution for drift time measurement. Since the design of the module has large flexibility due to the AMT, CPLD logics and DSP processing, it also can be used in many applications.

## VI. ACKNOWLEDGMENTS

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## VII. REFERENCES

[1] Y. Arai and M. Ikeno, "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution", IEEE J. of Solid-State Circuits, vol. 31, no. 2, pp.212-220, Feb. 1996.

[2] H. Shirasu, Y. Arai, M. Ikeno, T. Murata and T. Emura, "A VME 32 ch Pipeline TDC Module with TMC LSIs", IEEE Trans. Nucl. Sci. vol. 43, no. 3, pp. 1799-1803, 1996.

[3] Y. Arai, "Development of Frontend Electronics and TDC LSI for the ATLAS MDT", Nucl. Instr. Meth. vol. A453, pp. 365-371, 2000.

[4] Y. Arai, Y. Kurumisawa and T. Emura, "Development and a SEU Test of a TDC LSI for the ATLAS Muon Detector", Proceedings of the 7th Workshop on Electronics for LHC Experiments, pp. 185-189. CERN 2001-005, Oct. 2001. Available also from http://lhc-electronics-workshop.web.cern.ch/LHC-electronics-workshop/.

[5] AMT LSI home page, http://atlas.kek.jp/tdc/.

[6] J. Christiansen, M. Mota. "A high-resolution time interpolator based on a delay locked loop and an RC delay line"、IEEE J. of Solid-State Circuits, pp. 1360-1366, vol. 34, no. 10, Oct. 1999.