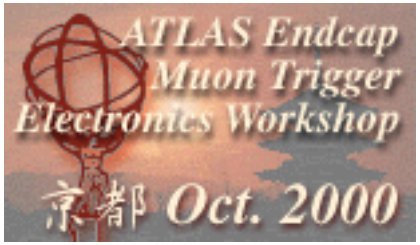


LSI Design and MDT Electronics

Oct. 26, 2000
ATLAS EC Trigger WS
@Kyoto

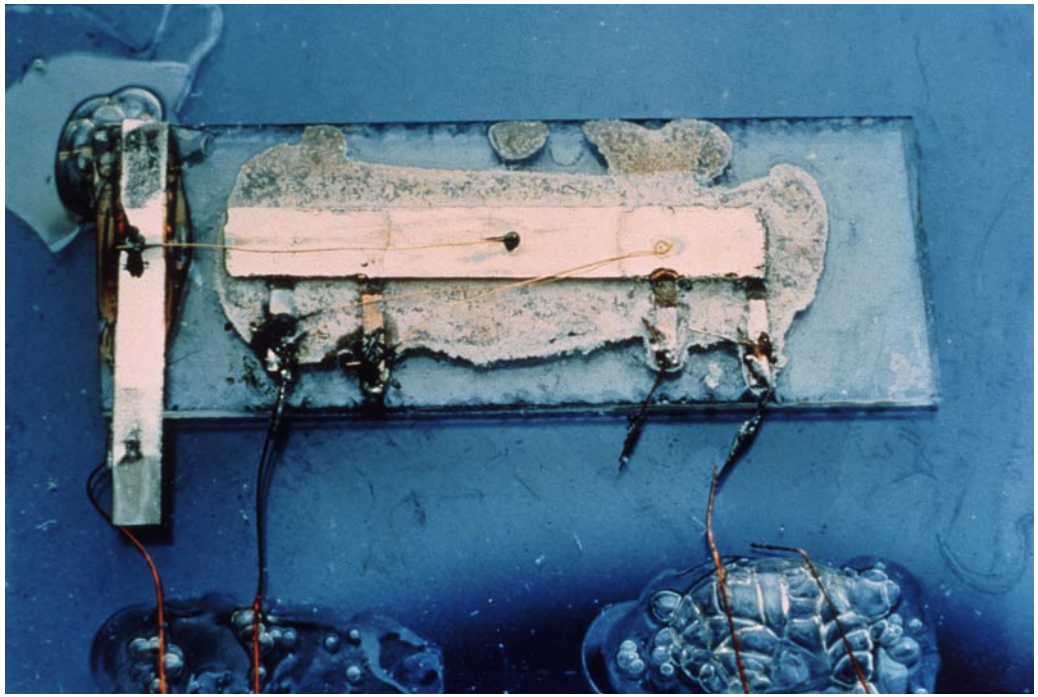
Yasuo Arai (KEK)
yasuo.arai@kek.jp
http://atlas.kek.jp/~araiy/

I'm not working on TGC Electronics,
but I'd like to show you something about

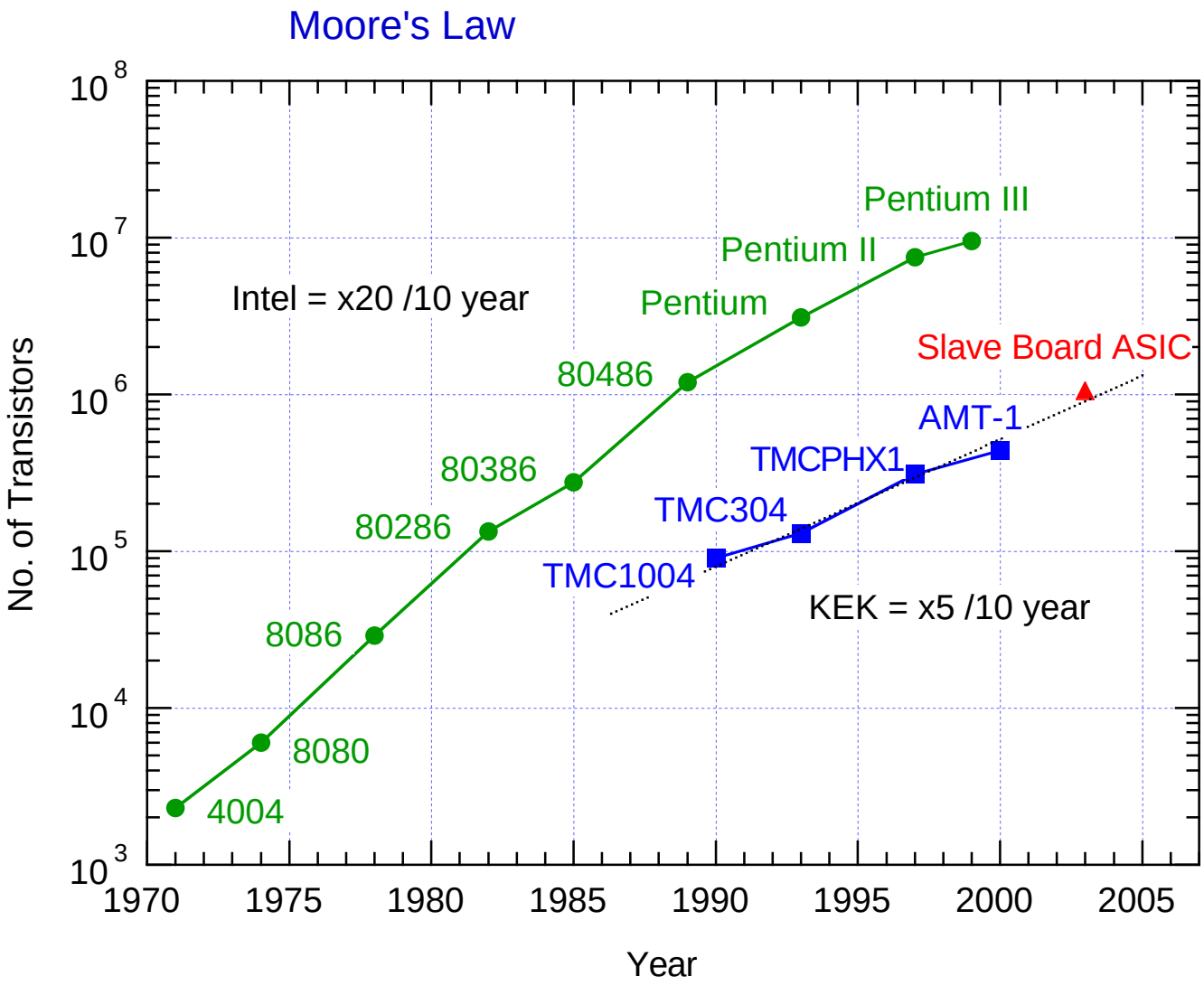
- LSI Design
- MDT Frontend Electronics
- ATLAS Muon TDC

First Integrated Circuit

Nobel Prize in Physics, Jack Kilby,
the invention of the integrated circuit.



A transistor and other components on a slice of germanium,
7/16-by-1/16-inches in size. (1958)

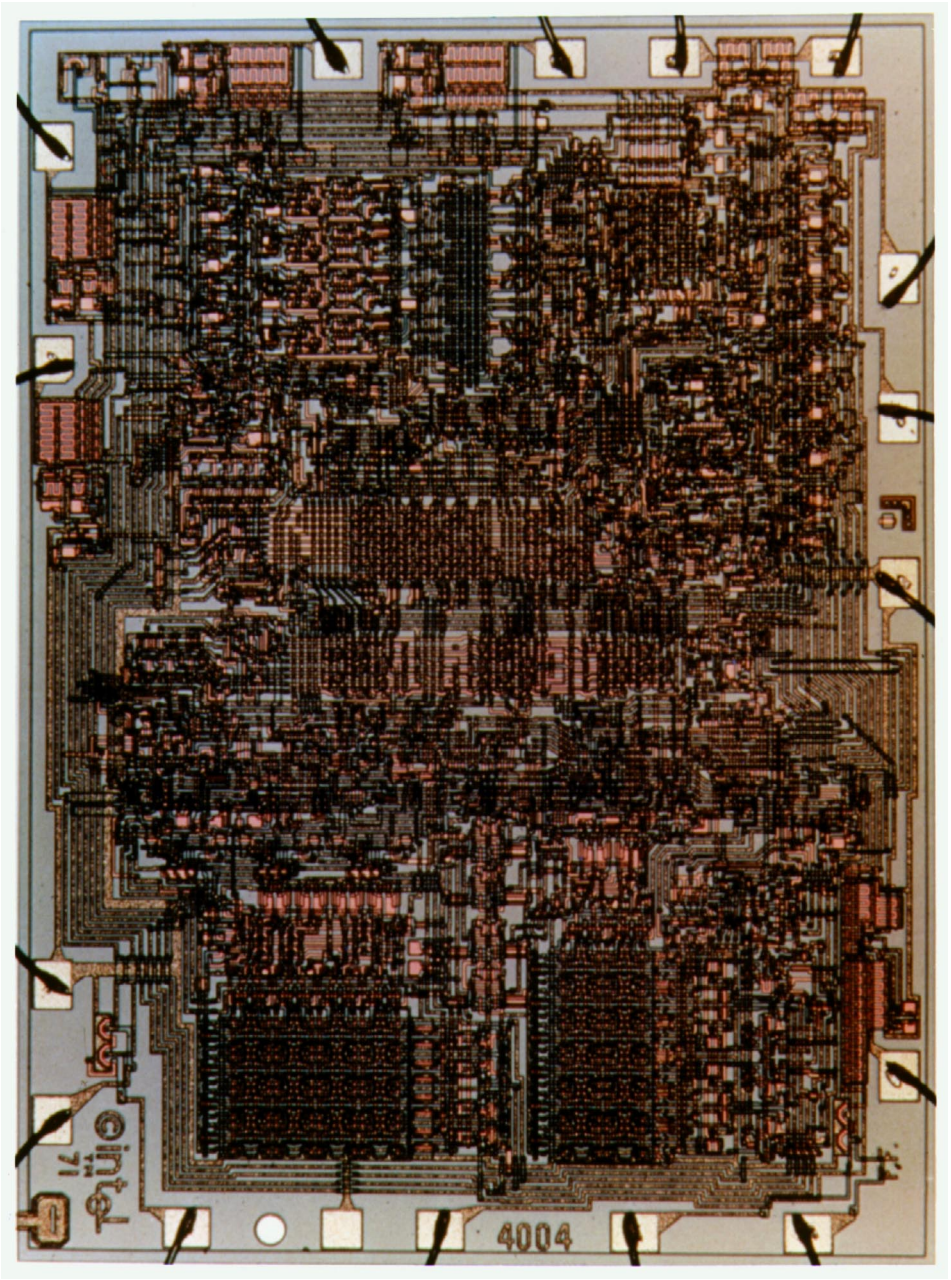

Moore's Law
No. of Transistors
Year
10^8
10^7
10^6
10^5
10^4
10^3
1970
1975
1980
1985
1990
1995
2000
2005
4004
8080
8086
80286
80386
80486
Pentium
Pentium II
Pentium III
Intel = x20 /10 year
TMC1004
TMC304
TMCPHX1
AMT-1
Slave Board ASIC
KEK = x5 /10 year

First Microprocessor

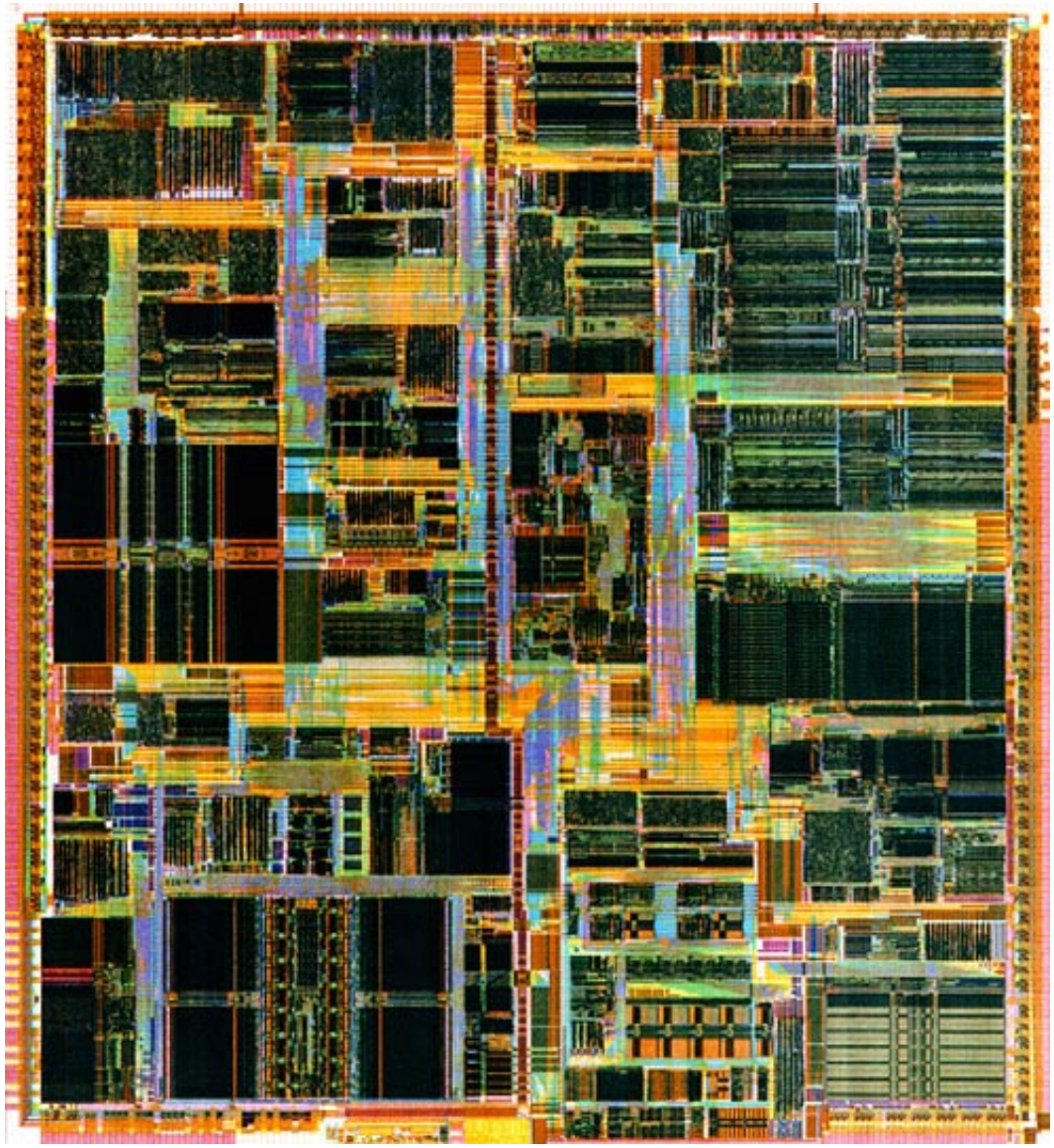
Year 1971

2300 transistors

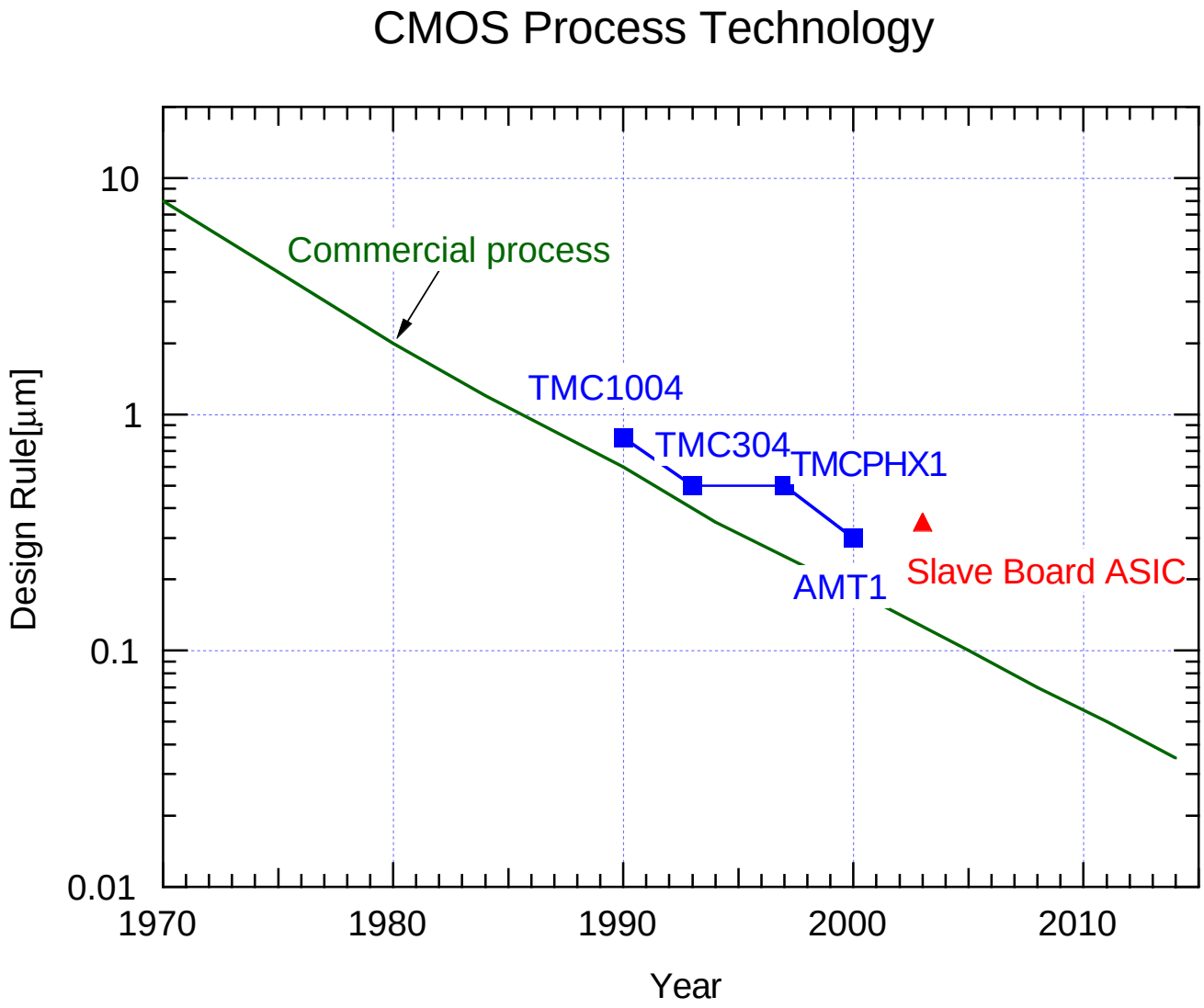
10 μm technology



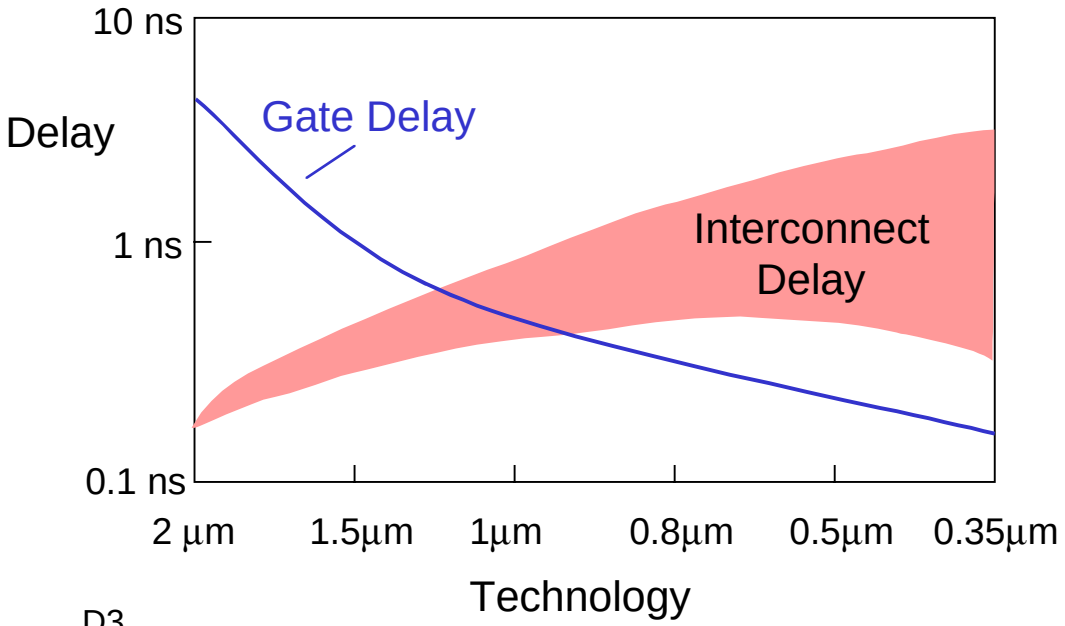
Then ....



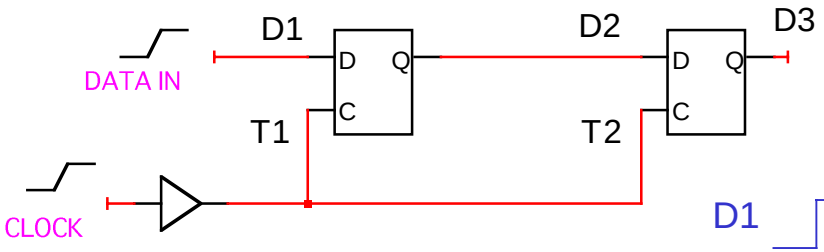
Pentium II

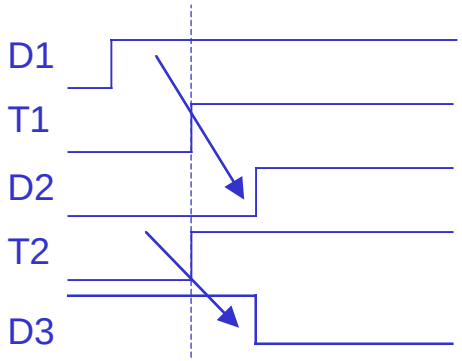

CMOS Process Technology
Design Rule[μm]
10
1
0.1
0.01
1970
1980
1990
2000
2010
Year
Commercial process
TMC1004
TMC304
TMCPHX1
AMT1
Slave Board ASIC

Gate Delay and Interconnect Delay

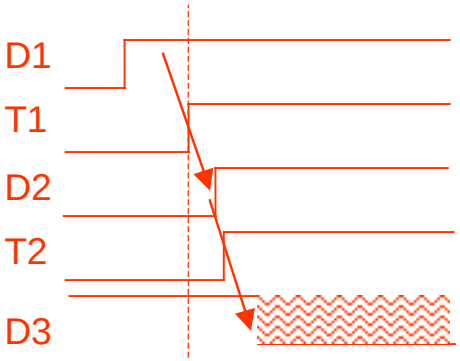


Simple Shift Register

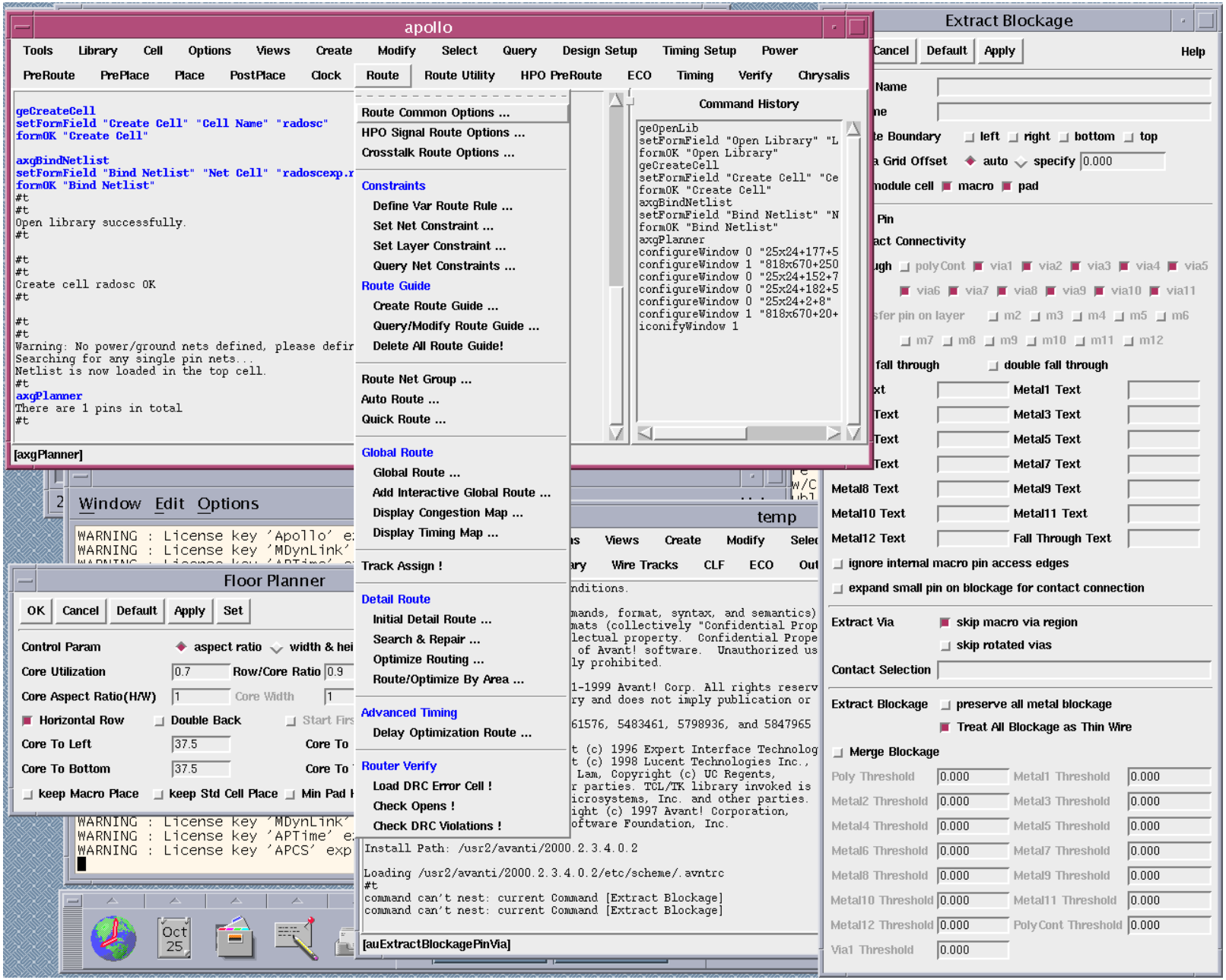




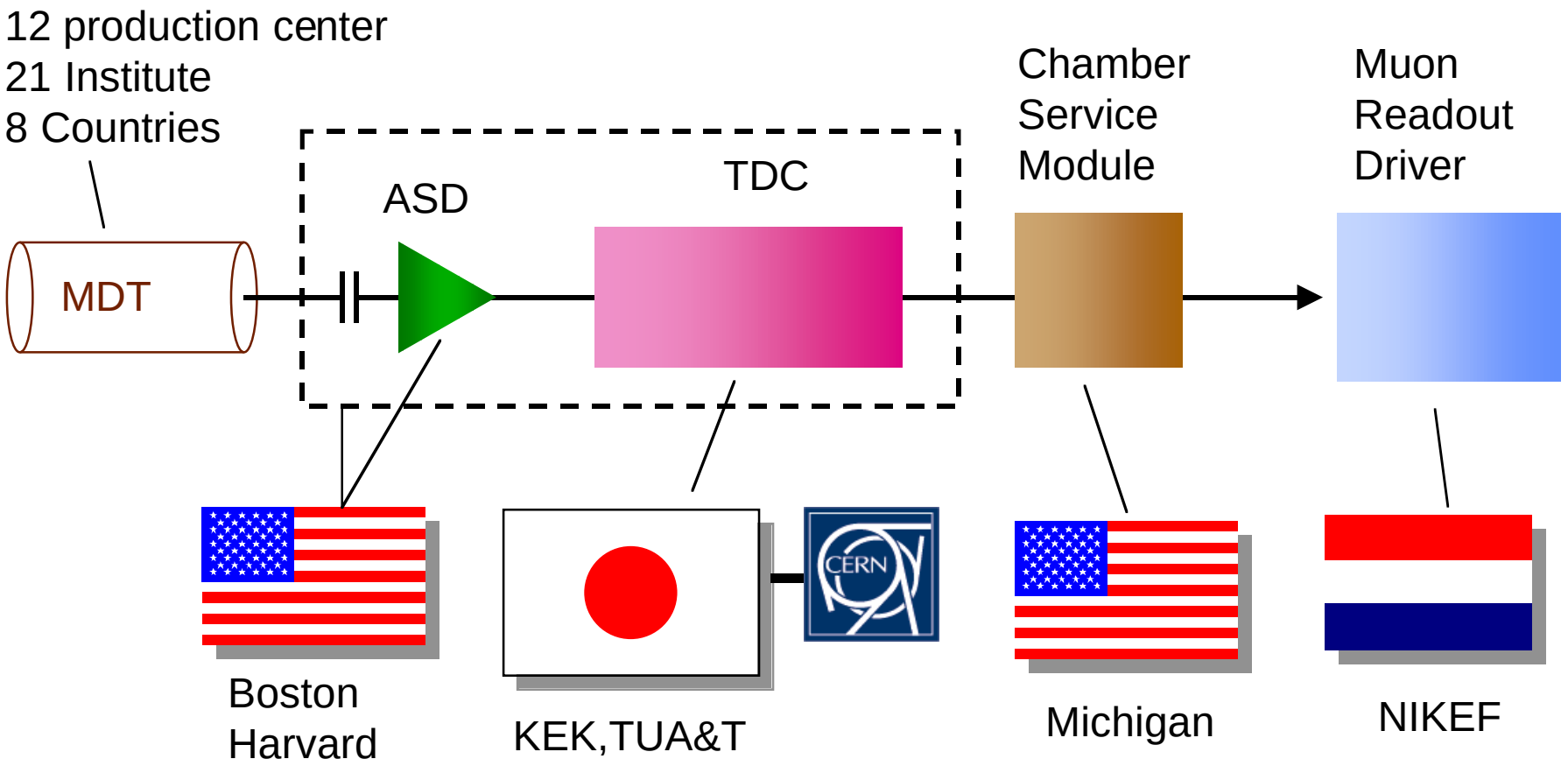
Good Old Days

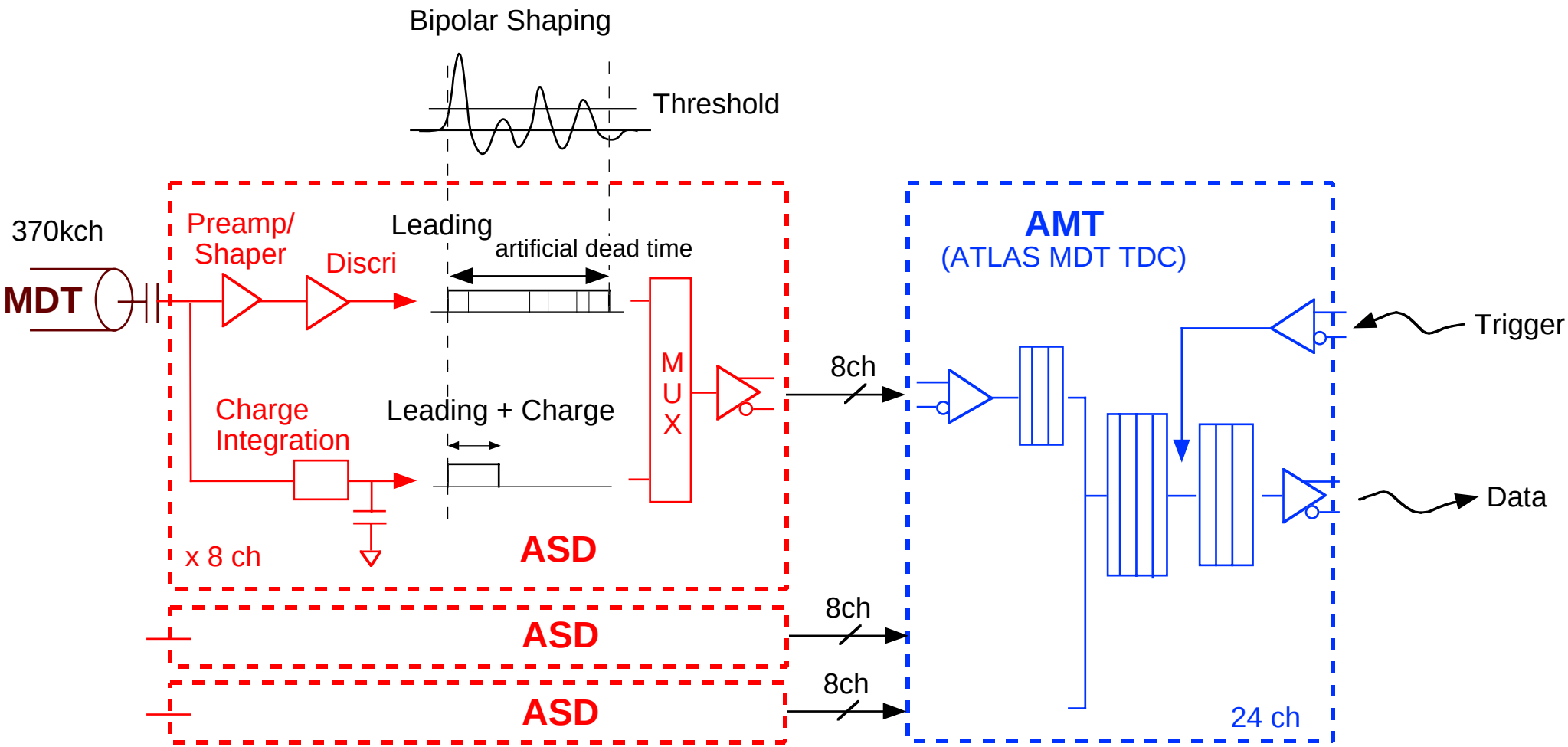


Nowadays


apollo
Tools Library Cell Options Views Create Modify Select Query Design Setup Timing Setup Power
PreRoute PrePlace Place PostPlace Clock Route Route Utility HPO PreRoute ECO Timing Verify Chrysalis
Route Common Options ...
HPO Signal Route Options ...
Crosstalk Route Options ...
Constraints
Define Var Route Rule ...
Set Net Constraint ...
Set Layer Constraint ...
Query Net Constraints ...
Route Guide
Create Route Guide ...
Query/Modify Route Guide ...
Delete All Route Guide!
Route Net Group ...
Auto Route ...
Quick Route ...
Global Route
Global Route ...
Add Interactive Global Route ...
Display Congestion Map ...
Display Timing Map ...
Track Assign !
Detail Route
Initial Detail Route ...
Search & Repair ...
Optimize Routing ...
Route/Optimize By Area ...
Advanced Timing
Delay Optimization Route ...
Router Verify
Load DRC Error Cell !
Check Opens !
Check DRC Violations !
Command History
[axgPlanner]
Extract Blockage
Cancel Default Apply Help
Floor Planner
OK Cancel Default Apply Set
Window Edit Options
temp
[auExtractBlockagePinVia]

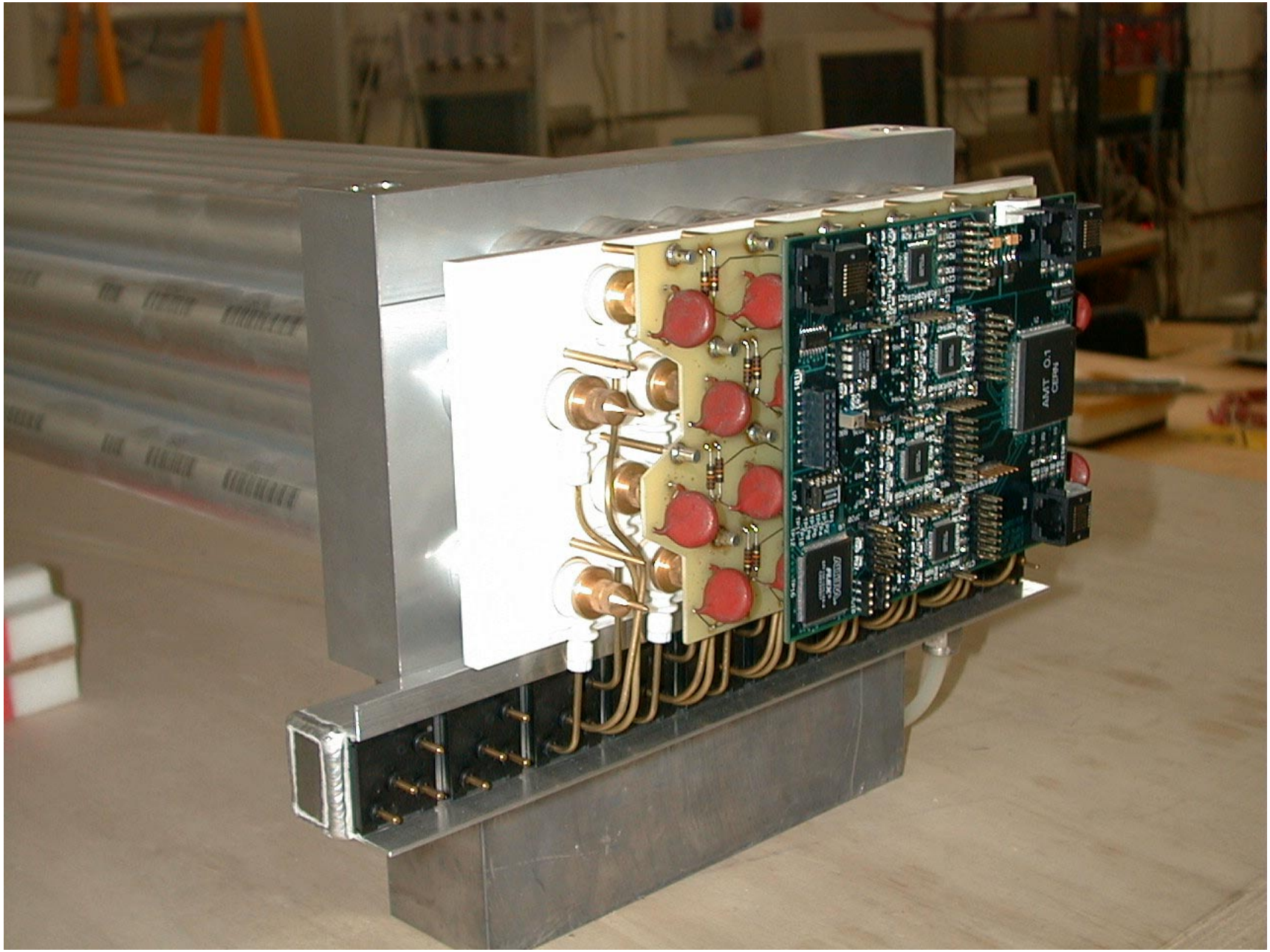
MDT Electronics Collaboration

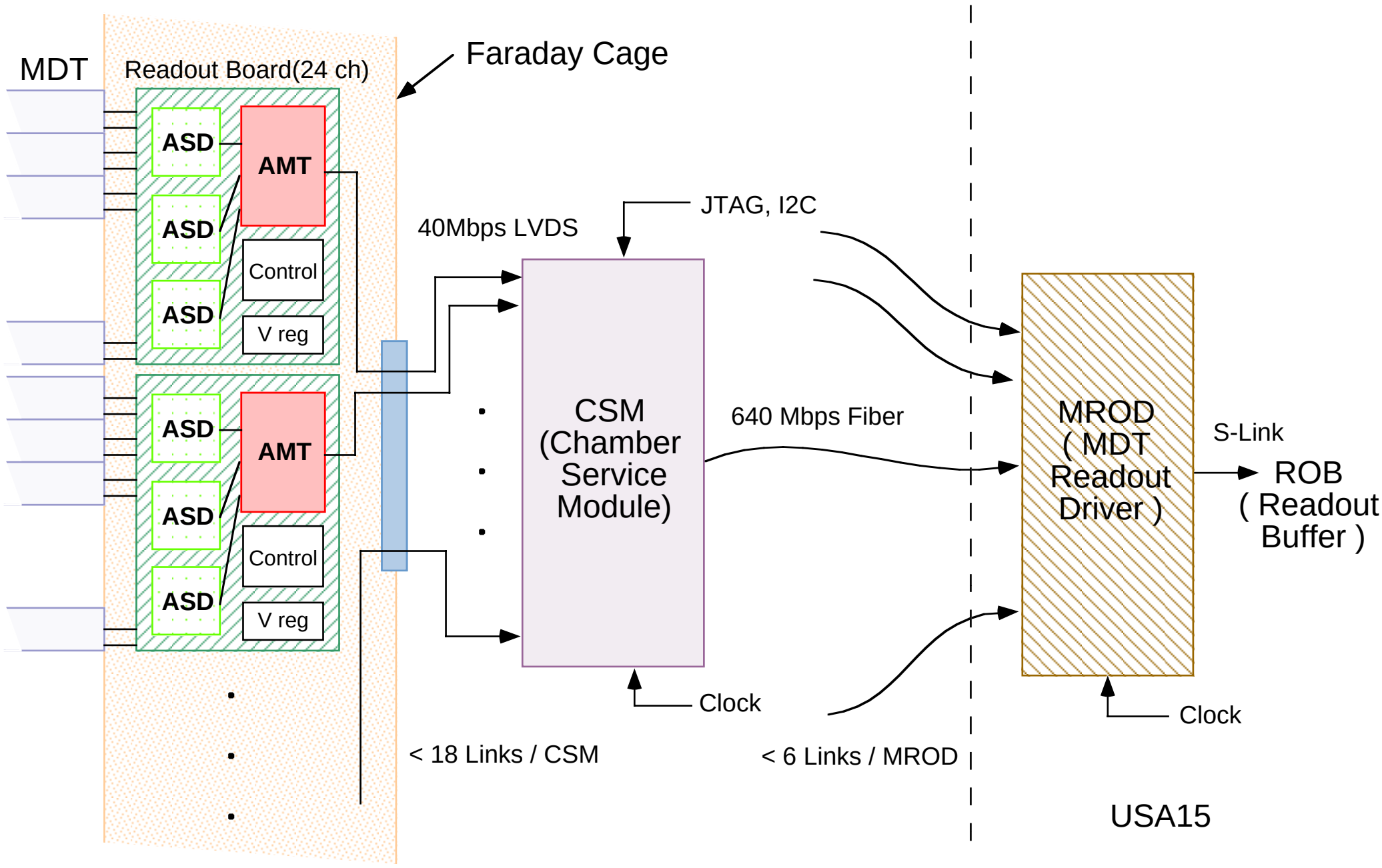




ATLAS MDT Frontend Electronics

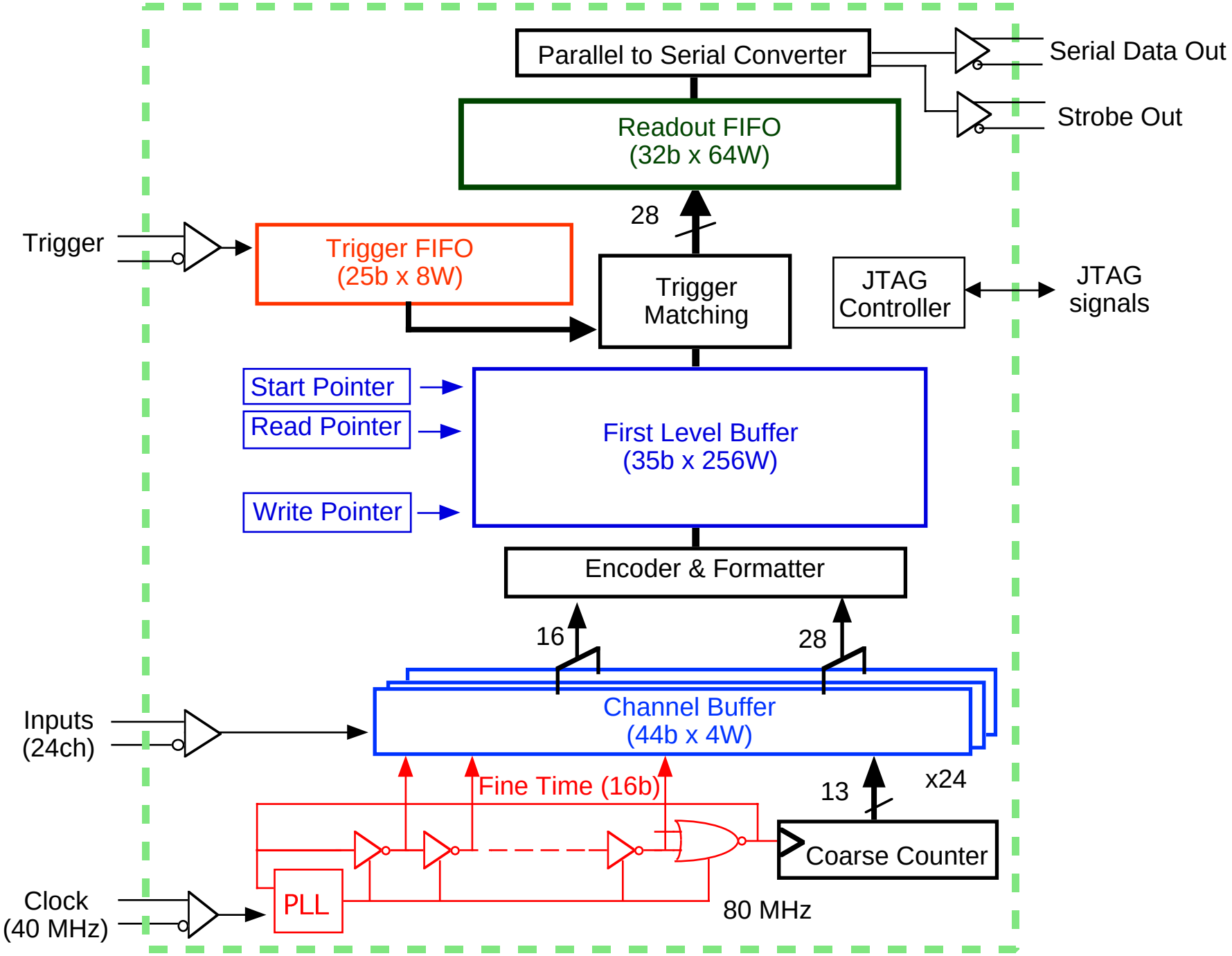
99.11.12 Y.A.


AMT 0.1
CERN



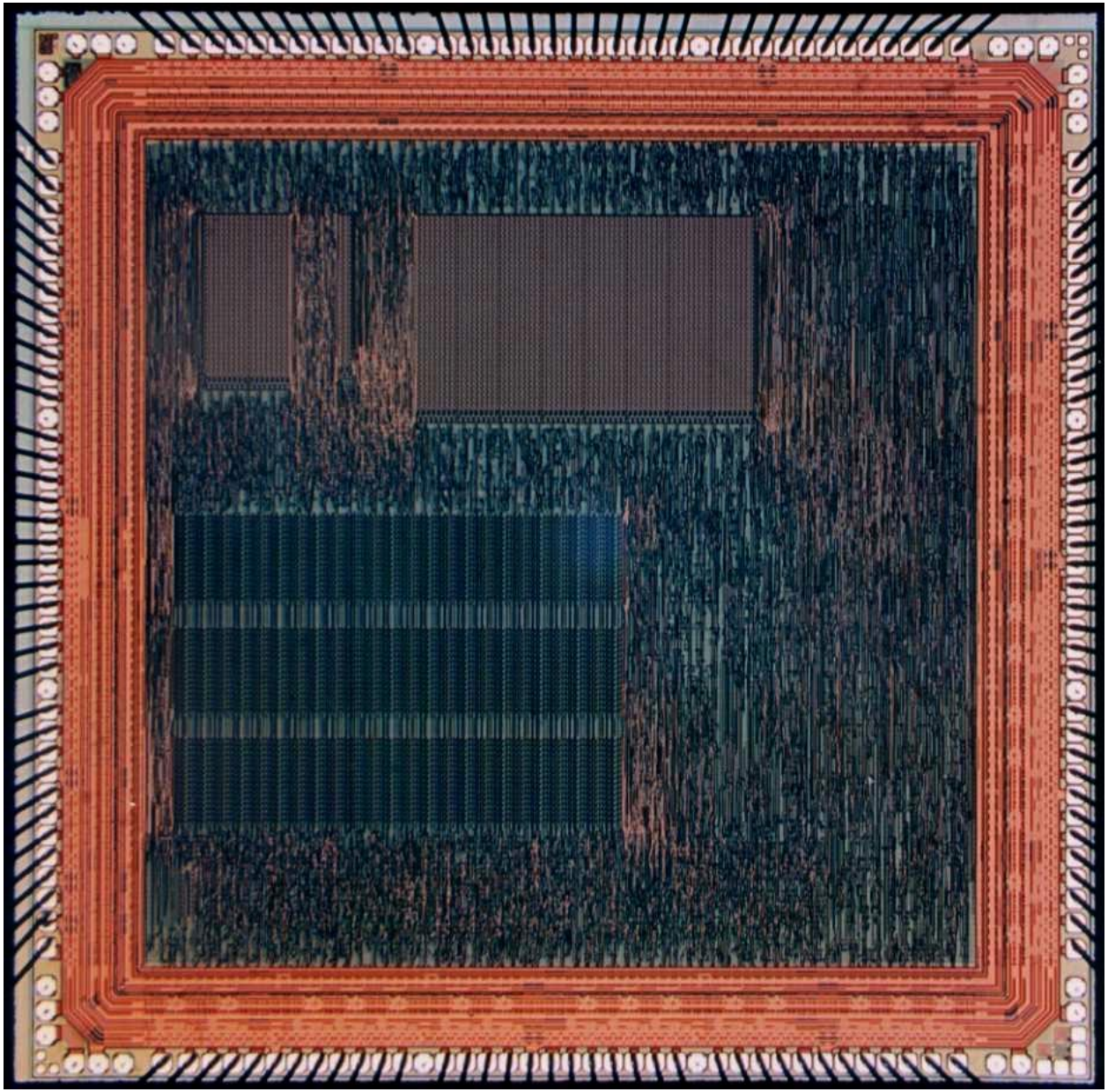
MDT Readout Flow

99.11.12 Y.A.



Block Diagram of the ATLAS Muon TDC

99.11.17 Y.Arai



Photograph of the AMT-1 chip

Development of ATLAS MDT TDC (AMT)

- ~370 k channels, 400 kHz input rate, 100 kHz trigger rate.
- Sub-ns timing resolution.
- Leading and trailing edge time measurement.
- Low-cost, Low-power & High-density (24 ch/chip).
- LVDS interface, JTAG control.
- Radiation Tolerant (~11 krad, 1.2×10^{13} n/cm^2).

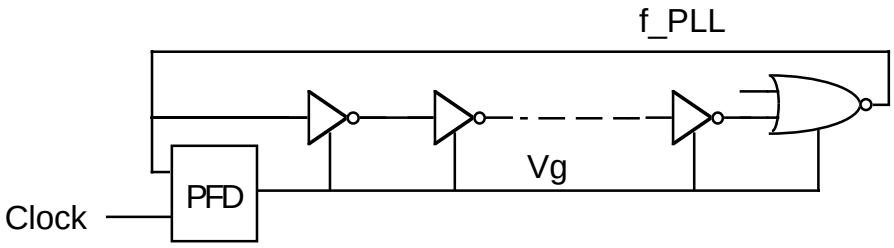
→ Design study in collaboration with CERN/EP -MIC group.

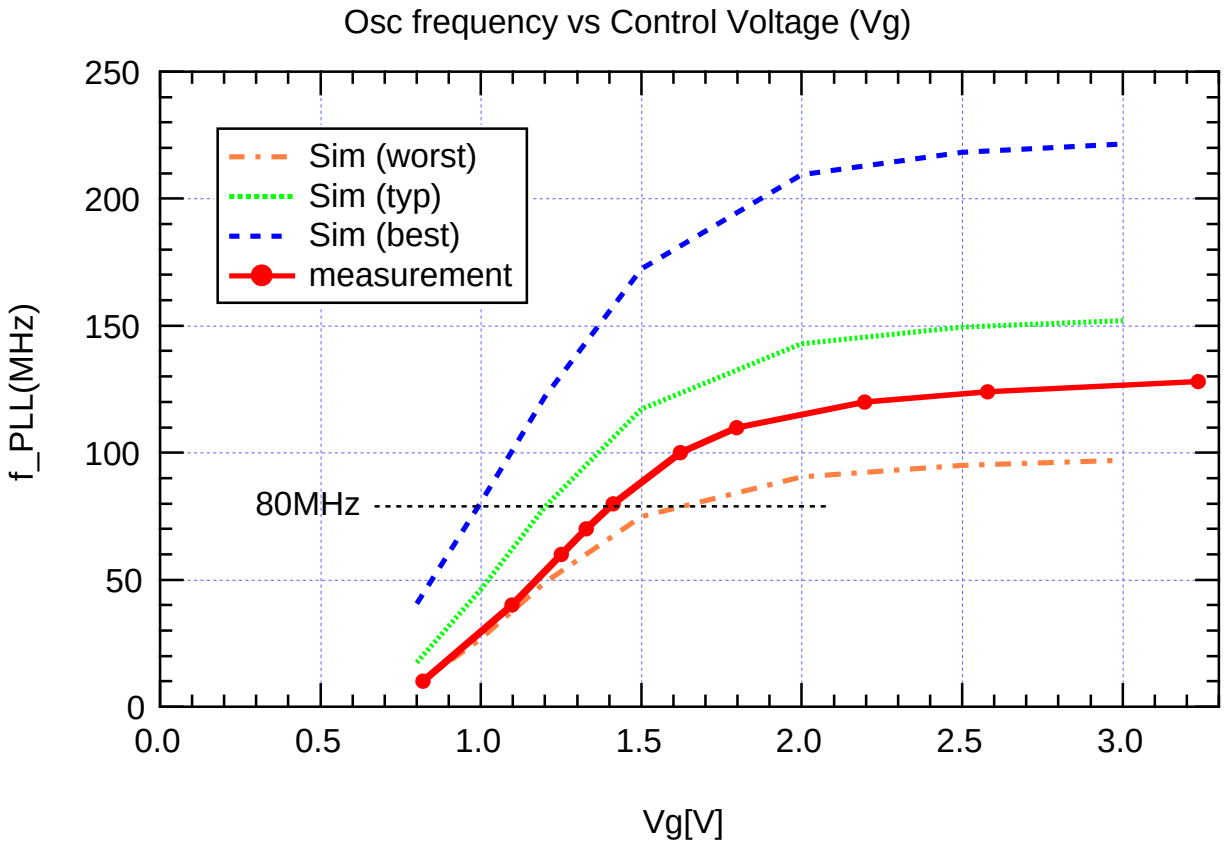
→ Quick test chip (AMT-0) in a 0.7 μm process.(10 kch)

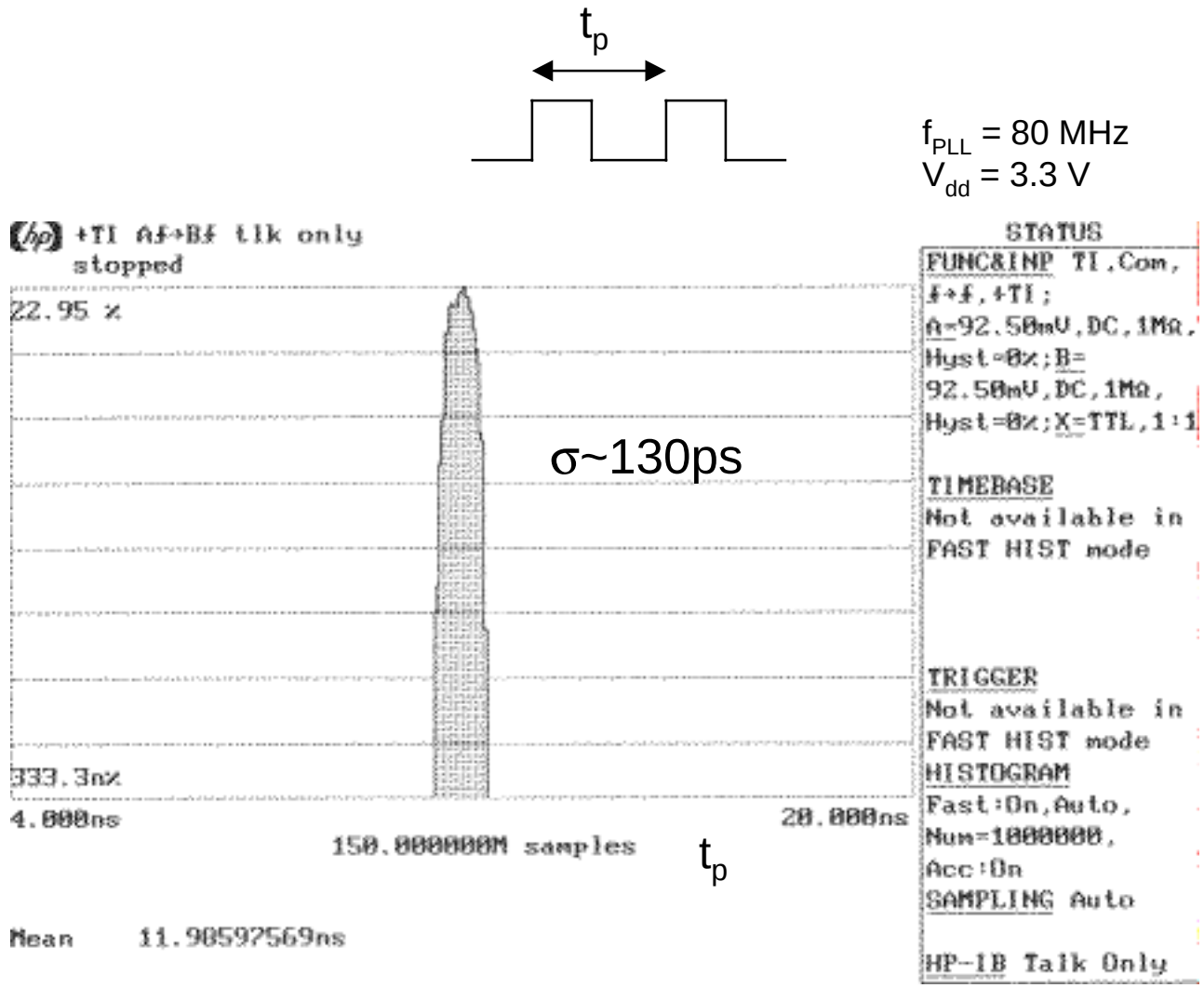
→ Develop a test element group chip (AMT-TEG) in a new 0.3 μm process (Toshiba Gate-Array) which will be used in a final chip.

→ Circuit performance test and radiation tolerance test was done.

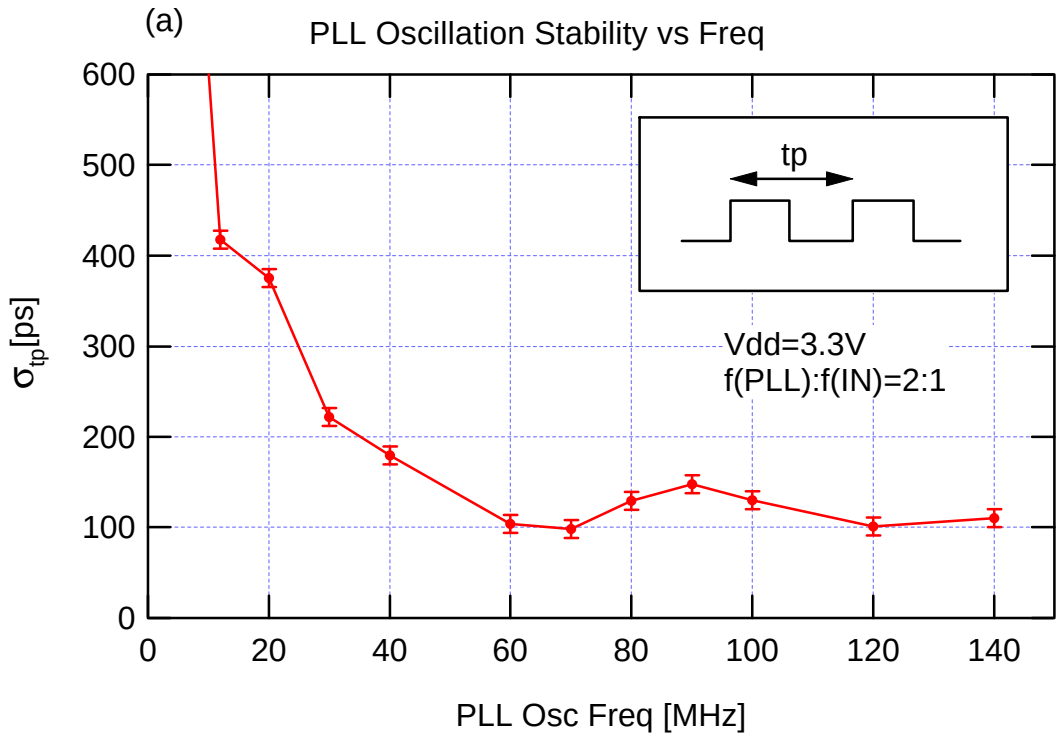
Voltage Controlled Ring Oscillator

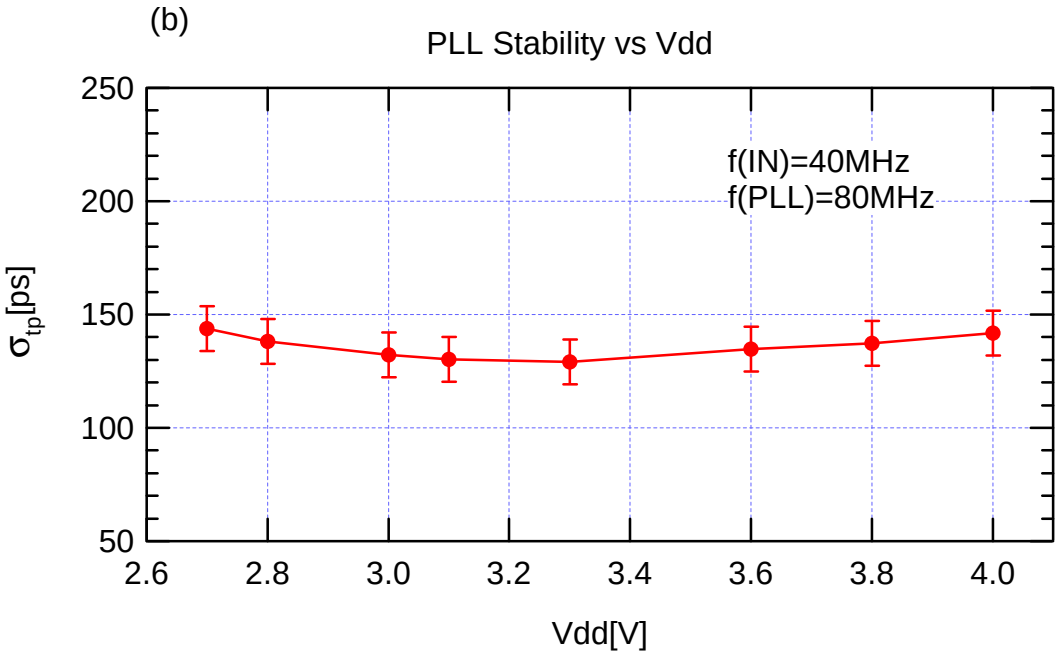




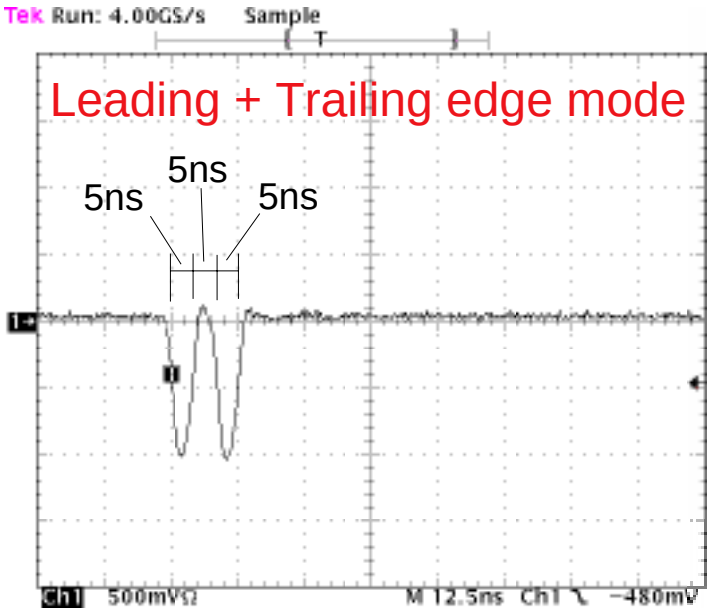


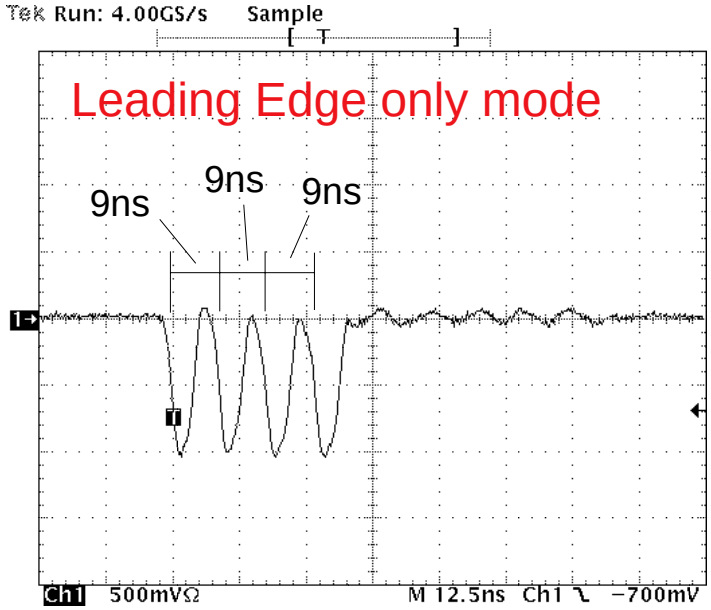
PLL Oscillation Jitter Histogram


(a)
PLL Oscillation Stability vs Freq
600
500
400
300
200
100
0
0
20
40
60
80
100
120
140
σtpd[ps]
PLL Osc Freq [MHz]
tp
Vdd=3.3V
f(PLL):f(IN)=2:1

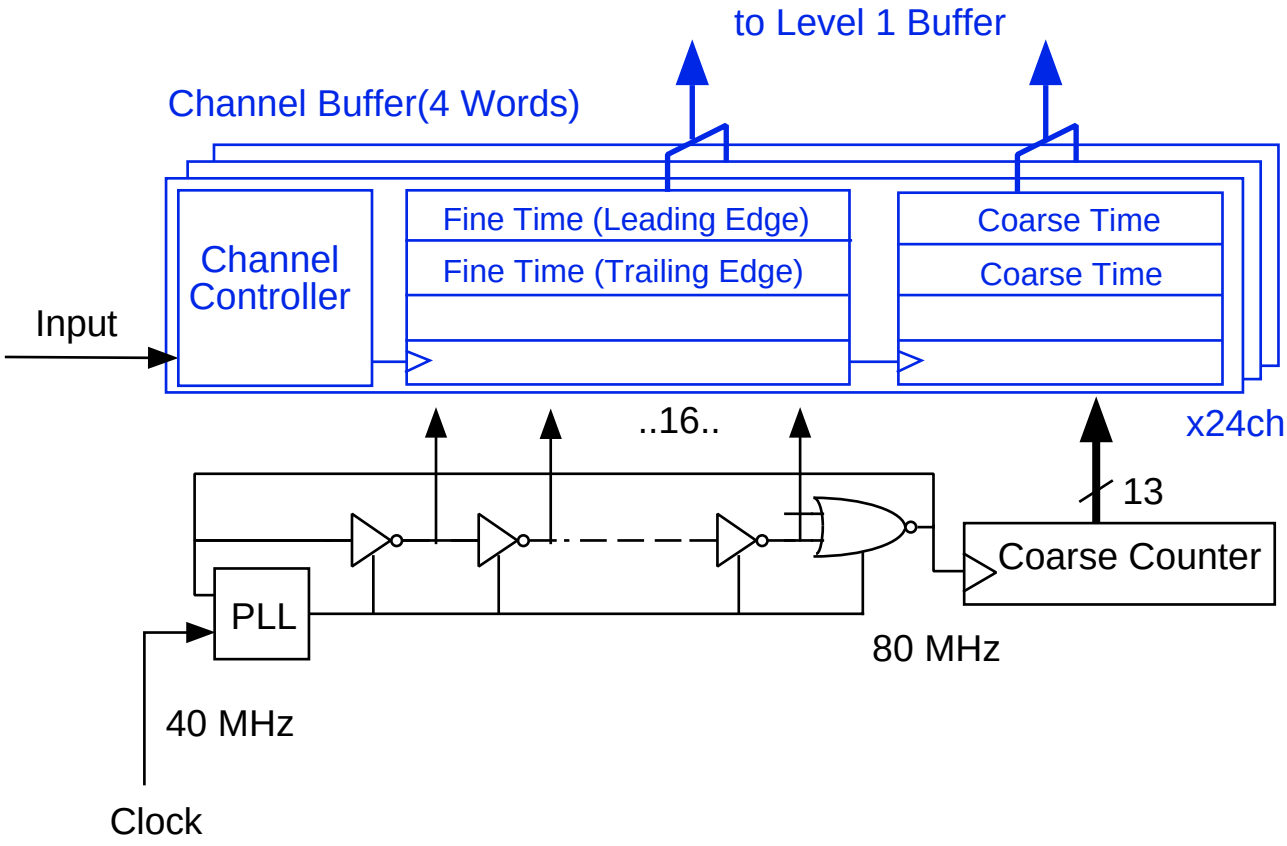

(b)
PLL Stability vs Vdd
250
200
150
100
50
2.6
2.8
3.0
3.2
3.4
3.6
3.8
4.0
σtpd[ps]
Vdd[V]
f(IN)=40MHz
f(PLL)=80MHz

Channel Buffer Speed

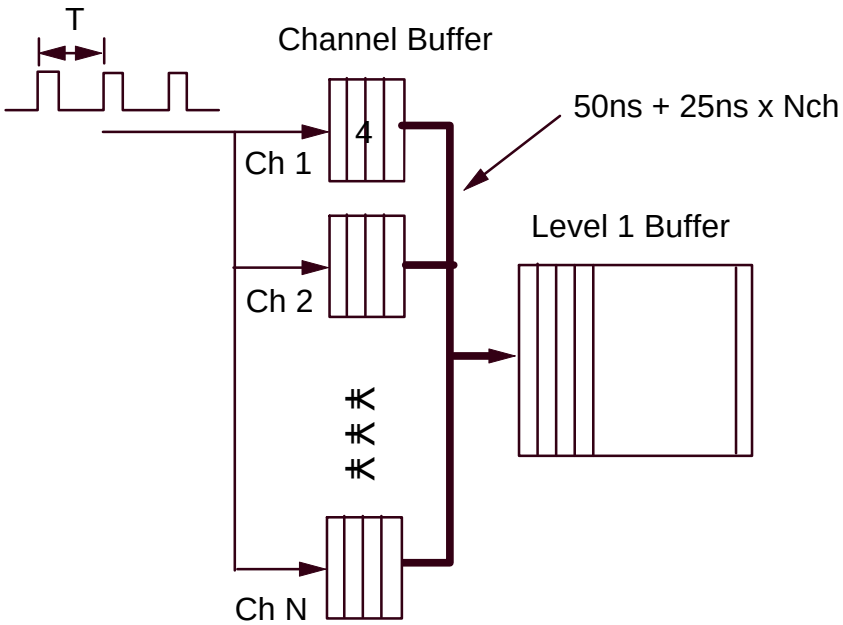


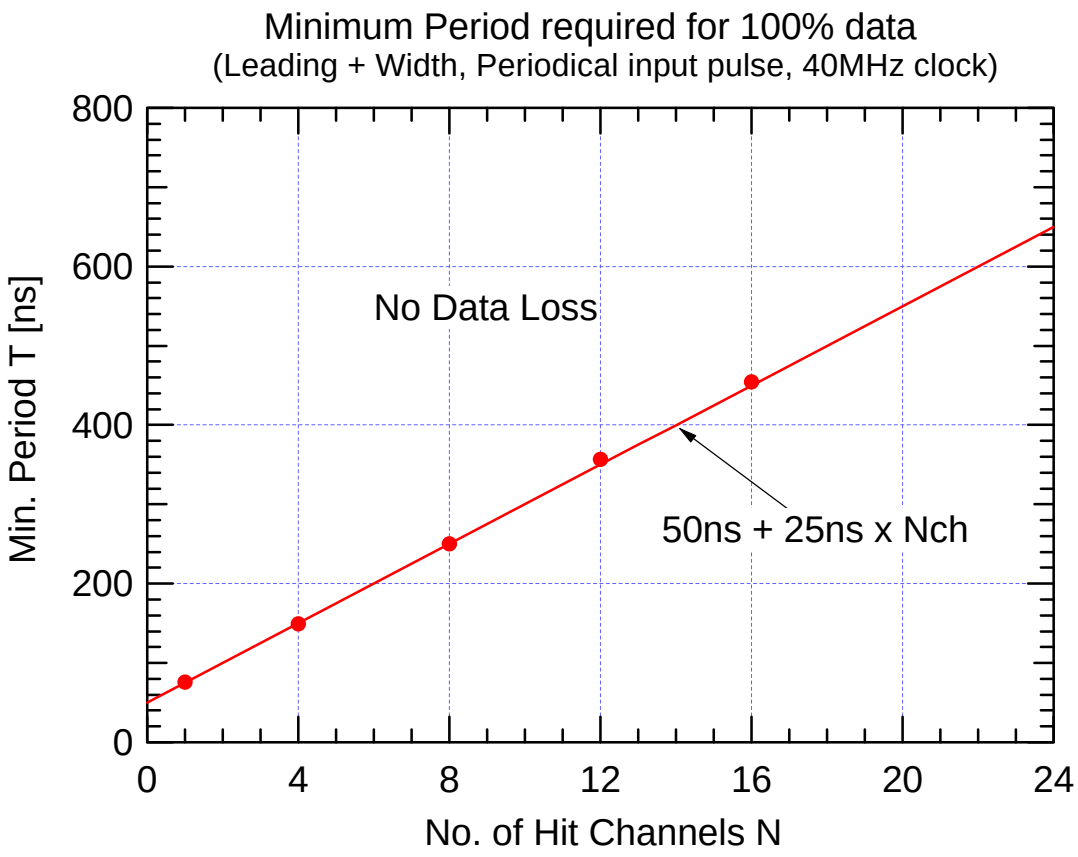


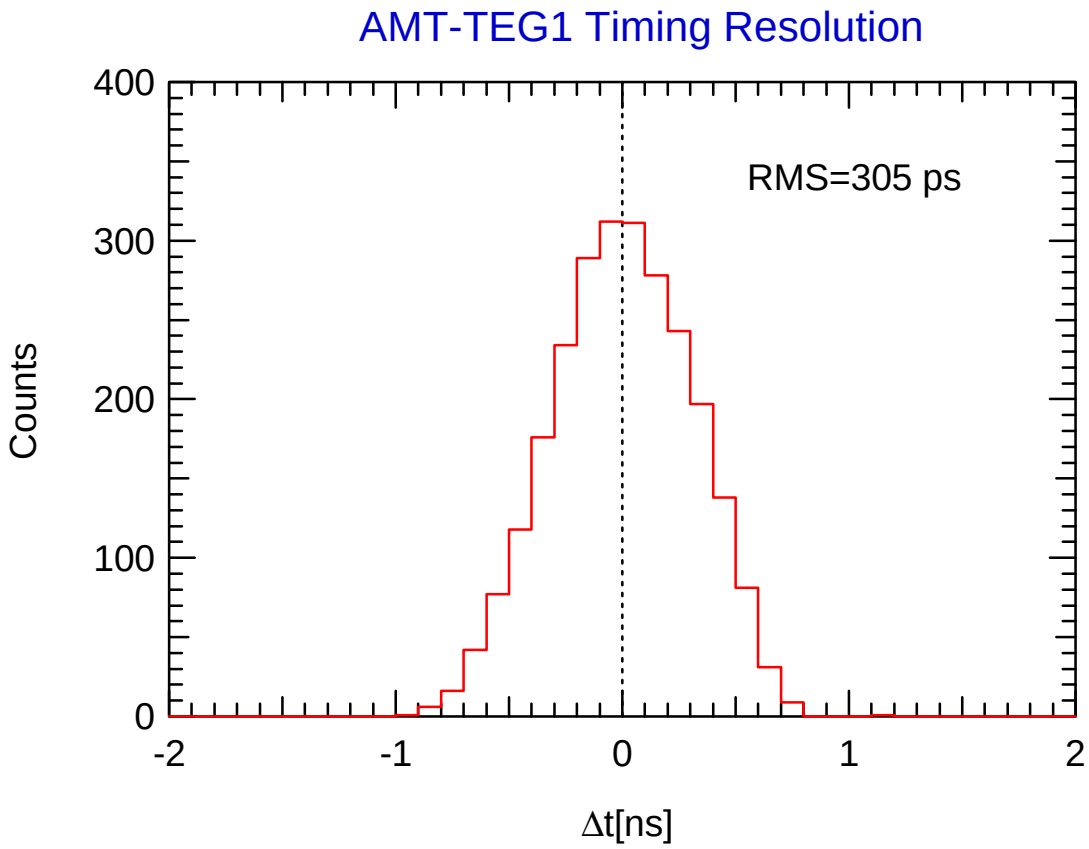
Multiple Edge Resolution = 5 ns (Double Edge)
= 9 ns (Single Edge)



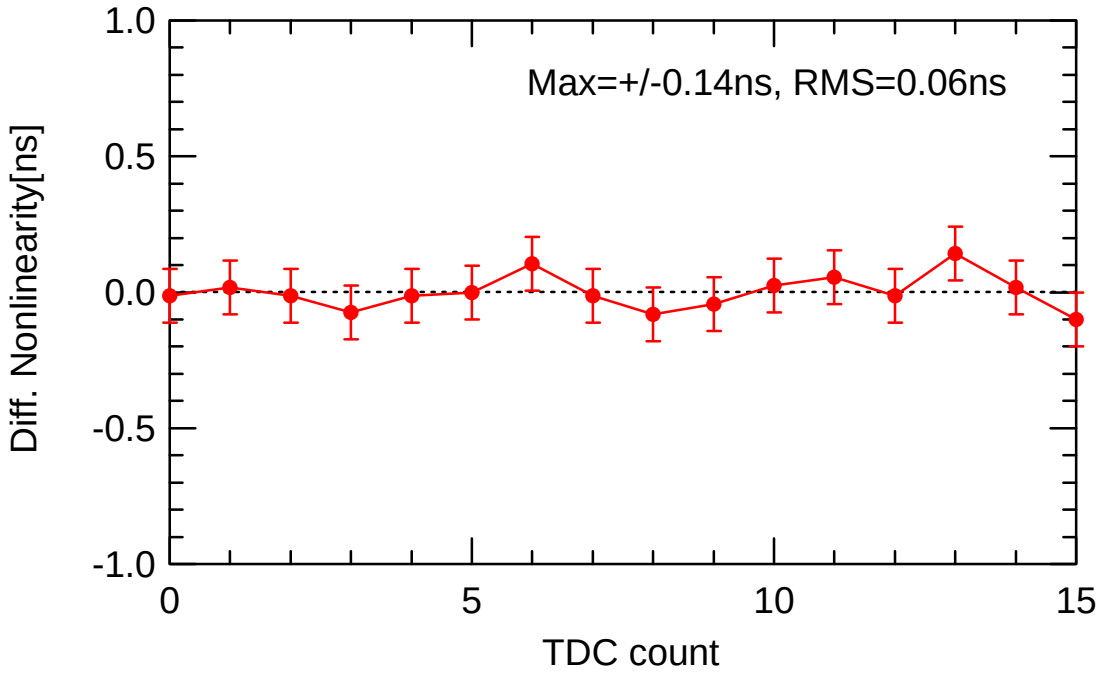
Data Transfer Rate to L1 Buffer



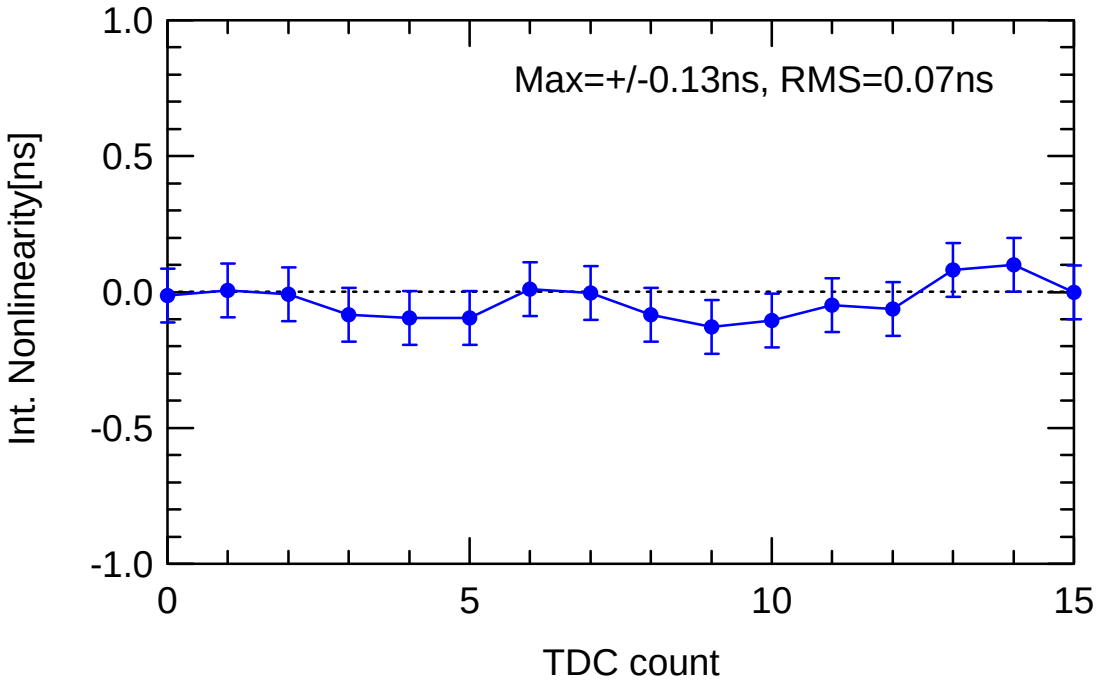



AMT-TEG1 Timing Resolution
RMS=305 ps
Counts
400
300
200
100
0
-2
-1
0
1
2
Δt[ns]

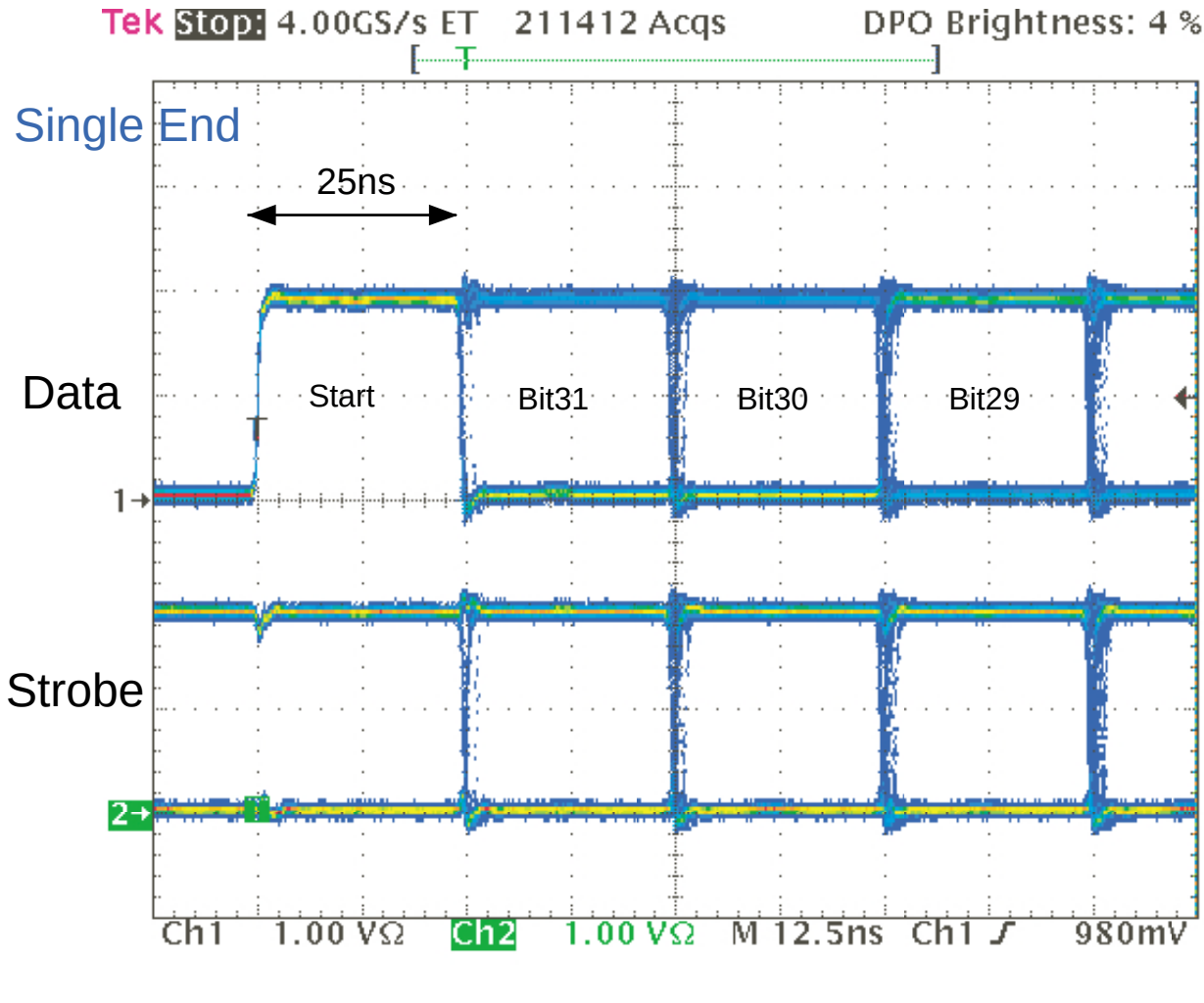
AMT-TEG1 Differential Nonlinearity

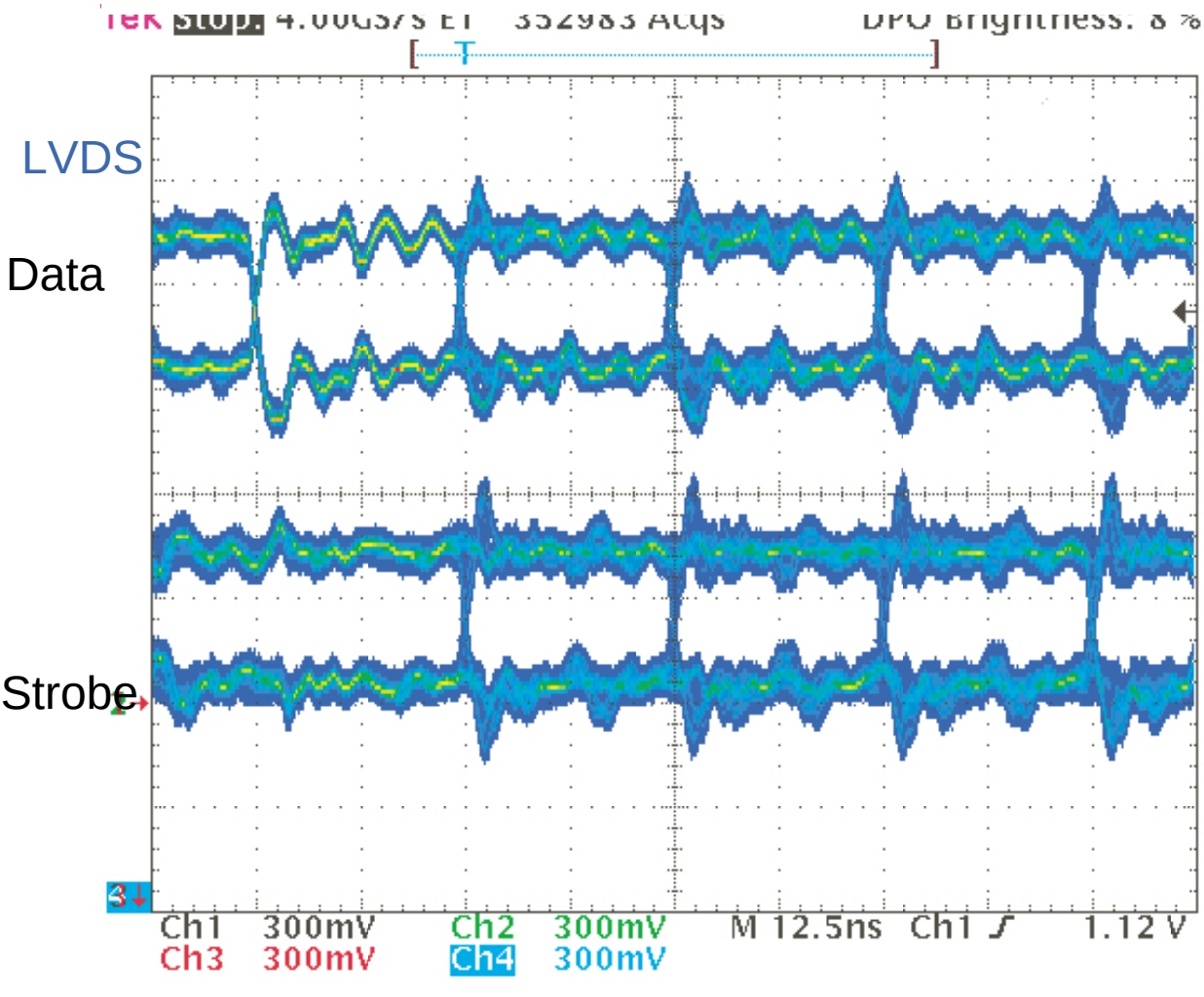


AMT-TEG1 Integral Nonlinearity



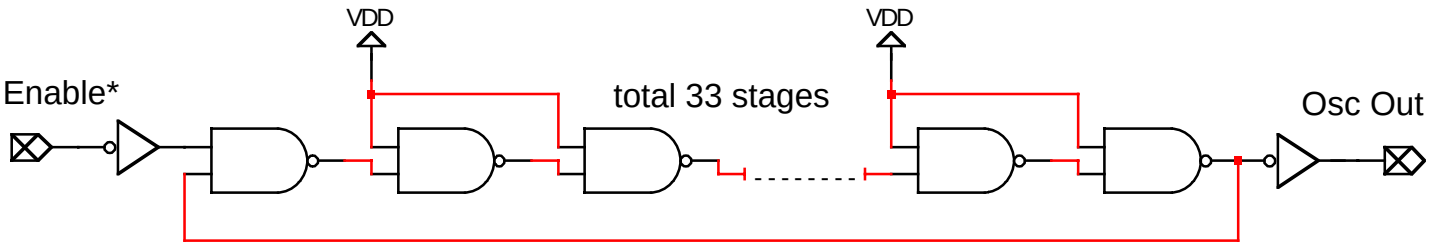
LVDS Serial Output

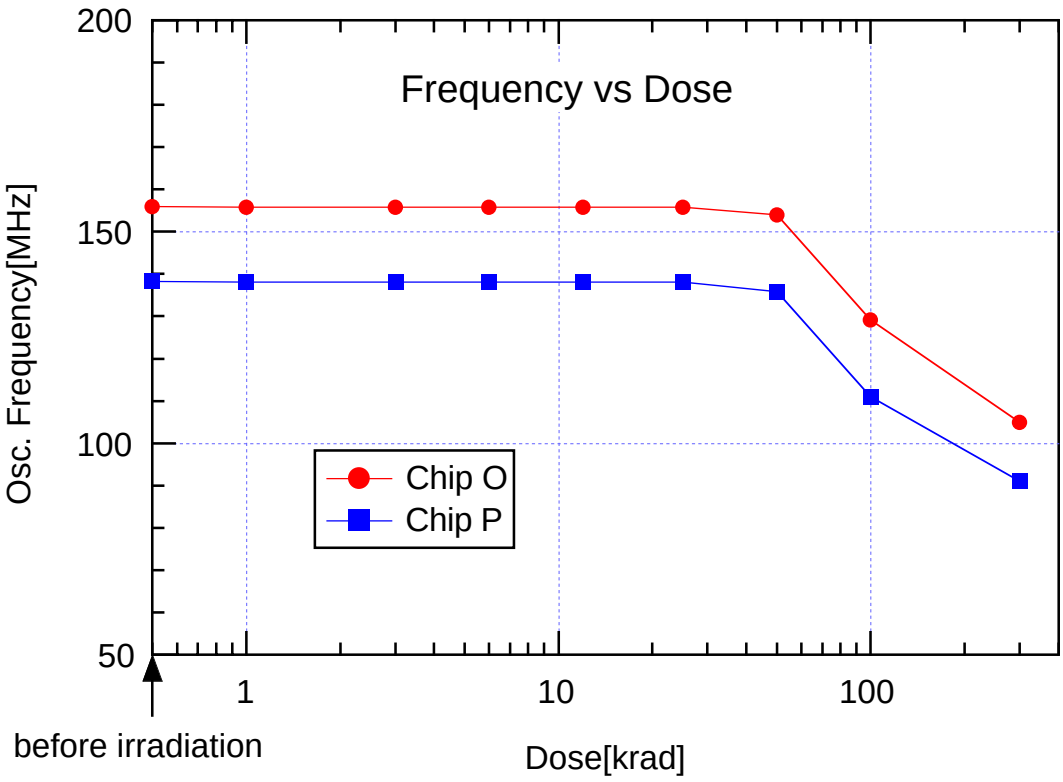


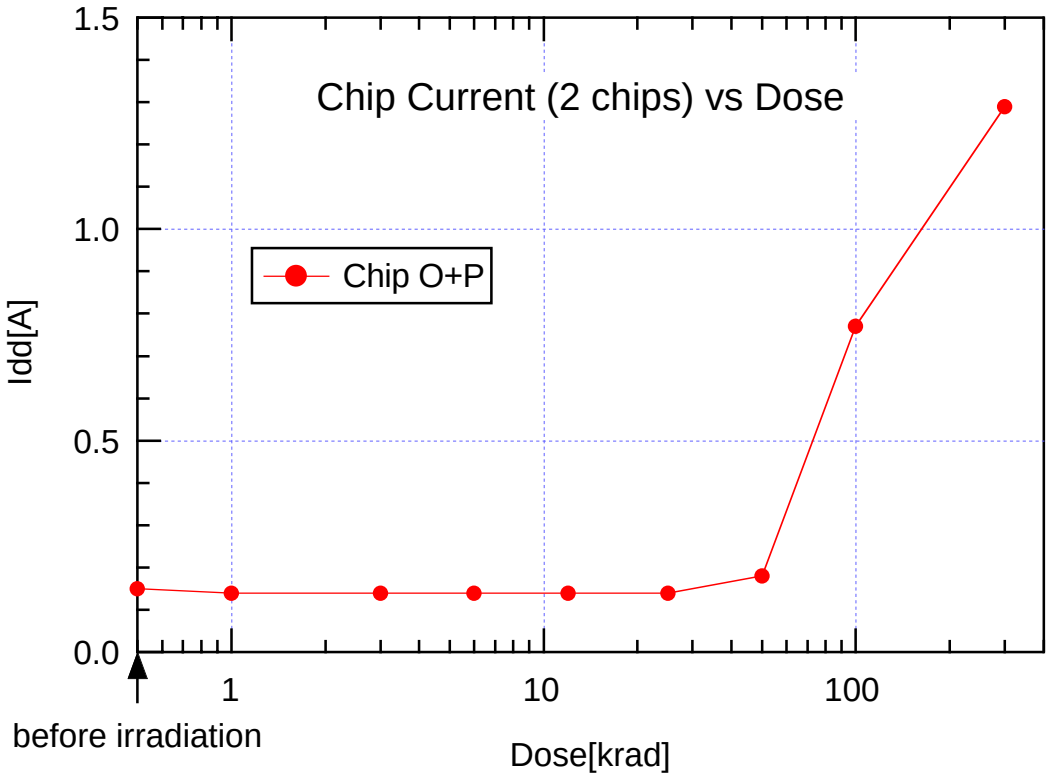


00.05.02 Y.A.

AMT-TEG1 Ring Oscillator







Summary of Measurements

	Measurements	Requirements
PLL	Freq. = 40 ~ 120 MHz Vdd = 2..8 ~ 3.8V	80 MHz 3.3V
Coarse Time Counter	120 MHz	> 80 MHz
LVDS receiver: ΔV Vcm	> 100 mV 0.2 ~ 2.2 V	> 100 mV 0.2 ~ 2.2V
LVDS driver (6.5m cable)	> 100 MHz	> 50MHz
Multiple edge resolution	< 5 ns	< 30 ns
L1B input speed	(2 + N) clocks	< (5 + N) clocks
Time Resolution	305 ps RMS	< 500 ps RMS
Diff./Int. Non-linearity	< 70 ps RMS	< 300 ps RMS
Radiation hardness for γ	> 30 krad	> 11 krad
Radiation hardness for n	> 1.6 x 10^{13} n/cm^2	> 1.2 x 10^{13} n/cm^2

Power Consumption

Simulation:

400 mW (Internal Circuit)

+ 480 mW (16mW x 30 LVDS receivers)

= ~900 mW/chip

Measurement:

3.3V x 148 mA = 488 mW/chip (20mW/chan)

(@400kHz hit, 100kHz Trigger)

LVDS receiver:

New Low Power design will be designed at Toshiba.

Thus more reduction in power is expected.

Summary

- LSI technology will advance beyond year 2015.
- Design methodology is also changing rapidly.
- We must keep up with this change.
- Chanlenge to Cost, Complexity, Testability, Radiation damage...

- MDT electronics group are now making 10k channels for MDT test.
- Start system tests in many places.
- AMT-1 chip is working and any serious flaw is not found.
- Final AMT chip (with Low Power LVDS receivers) will be completed in next spring.