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A CMOS Time to Digital Converter VLSI for High-Energy Physics

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Abstract

A Time to Digital Converter VLSI chip for high-energy physics experiment is developed. A low-power and high-density characteristics of the chip are attained by using submicron CMOS process and a new circuit technique which use memory cells and gate delay. In order to achieve excellent stability of time measurement, an internal feed-back circuit is also introduced.

Introduction

Time measurement is one of the important technique in high-energy physics experiments and is also applicable for other fields of time measurement. For example, time information of $\sim 10^6$ channels with nano second resolution is required in the next generation of experiments. In addtion to that, data buffering is also required to use the detector under high-counting rate ($\sim$ 60MHz) environment. This requires the use of low-power and high-density VLSI chips for Time to Digital Converter (TDC). High-speed shift-register is one of the good candidates to make a multi-hit TDC module, but is not suitable for a large system because of high-power consumption and formidable noise radiation due to the high-frequency common clock ($\sim$ 1GHz). In this paper, we present the design of a new VLSI chip called TMC (Time Memory Cell/Chip [1][2]), main components of which are memories and delay lines (gate delay). Use of the high-density CMOS technology and a lower frequency clock make the TMC be low-power consumption. To get high accuracy for timing information, the delay time of a line of delay elements is compared with external clock, and a correction is made for each cycle.

Radiation hardness of electronics is also very important item in recent accelerator experiments ($10^4 \sim 10^6 rad/year$). We used static circuits as much as possible to enhance the radiation hardness.

We implemented test circuits in a TEG (Test Element Group) chip, which will be used to evaluate the design.

Circuit Description

A series of memories where write signals are connected to a line of buffers with delay $\Delta\tau$ could record timing information with the corresponding resolution. However, gate delay time varies more than 10% because of silicon process instability, supply voltage variation and temperature drift. In a VLSI process, uniformity of the gate delay in a same chip is fairly good. We can get high accuracy by measuring the delay time of a series of gate and comparing it with external clock period and making feed-back. In our process, the simulation result of a delay time is about 0.8ns for each delay element. We connected 20 delay elements in a series (a column memory), so each column covers 16ns time range. This means clock period needed is 16ns, not 0.8ns.

This lower frequency gives its lower power consumption, because the power consumption P of a CMOS chip is expressed as;

$$P = C \times V^2 \times f$$

where C is a load capacitance, V is a supply voltage and f is switching frequency. Furthermore, basic element of our circuit is a memory, so only a small fraction of the circuit will switch at once, whereas in a shift register all the circuits will switch simultaneously.

The circuit of the basic cell (a memory and a delay element) of the TMC is shown in Fig. 1. M1, M2, M3 and M4 are cross coupled inverters (full CMOS memory). M9, M10, M11 and M12 make a delay element, and M13 controls the rise time of the first inverter, so

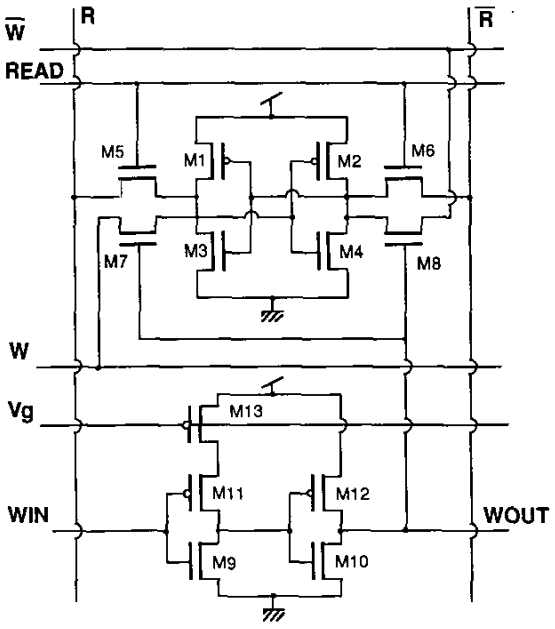

Fig. 1 Schematics of the basic cell of the TMC.

the delay time of the falling edged is controled via gate voltage (Vg) as shown in Fig. 2. More than 30% of delay time is controlled by changing the Vg.

Fig. 3 shows the feed-back circuit. When a clock sets two flip/flop's, capacitors C1 and C2 will be started to charge up. The charging of C1 will be stopped by the end pulse of a column of delay element. On the other hand, the charging of C2 will be stopped by the next clock. So the voltage difference between C1 and C2 is proportional to the lag of a column element. The FBCOMP compares input voltages and Hi or Lo output is asserted if the difference is more or less than ~20mV. This two threshold comparison is introduced to stabilize the feed-back circuit. If the delay time of a column is less than the clock period, charging of the C3 will occur during the store period. This will speed up the delay time of the column at the next cycle. If the delay time is larger than the clock period, discharging of the C3 will occur.

Summary

We have designed and simulated test circuits on the TEG which has basic functions needed in the final design. The TMC will be used as a key element in a multi-hit TDC which has a better than 1ns resolution. Intelligent I/O functions will be implemented in production chips. The low-power characteristic of TDC part and intelligent I/O functions implemented on the same chip enables us to build new generation detector which is coverd with many silicon chips.

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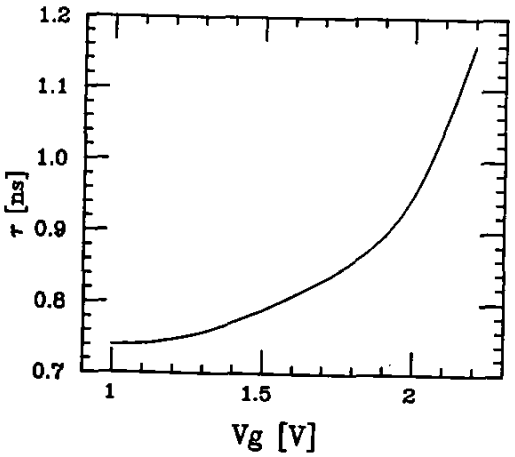

Fig. 2 SPICE 2G simulatinon for the delay time of falling edge in a delay element versus the gate voltage (Vg). Model of SPICE2G was modified to fit our process.

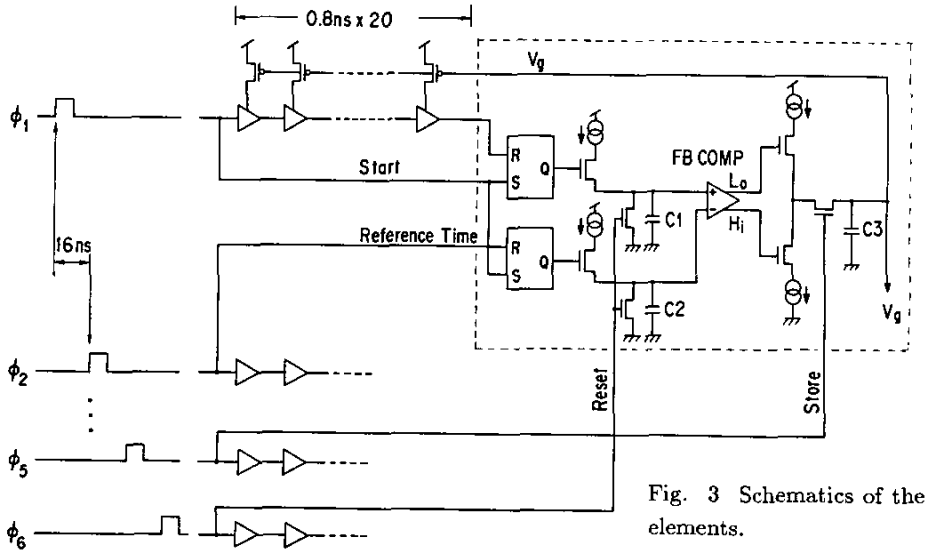

Fig. 3 Schematics of the feed-back circuit and deley elements.