

AN IDEA OF DEADTIMELESS READOUT SYSTEM BY USING TIME MEMORY CELL

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Abstract

We propose a deadtimeless readout system for the tracking device at SSC. Essential part of this scheme consists of a development of an LSI named Time Memory Cell which sits on the detector and holds time information in digital. Preliminary design and results of circuits simulation of the LSI are presented. Possible configuration of readout system for the central tracking device is also shown.

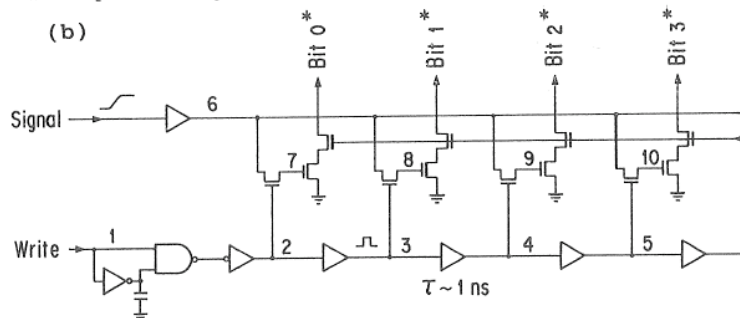
Introduction

Tracking device will still be main component of the SSC detector. However, there are many severe problems in readout electronics;

1. Beam crossing interval (~ 16 ns) is much shorter than the decision time of the first level trigger (~ 500 ns). All the information from detector must be stored for the duration.
2. Total number of readout channel is expected to be more than 100k to achieve high level tracking probability under extremely high multiplicity and high radiation environment. This number is ten times larger than that of the existing big detector.

Signal cables of 100k channels will amount to about 1 m² cross section. This may cause engineering difficulty to built in and large cracking in the calorimeter. Development of readout microchips and installation of these chips on the detector is a possible way to solve these problems. The microchip stores signals until trigger decision, it processes signals to reduce their data size and send them to outside with multiplexing after trigger decision. Those chips must be very low power device to avoid elaborative cooling system.

We propose an microchip named TMC (Time Memory Cell). which can be made with CMOS LSI of current state of art technology. It would be low power device and has time resolution better than 1 ns. We have made a preliminary design and simulation of the TMC.



We also describe an idea of readout scheme for SSC central tracking device using the TMC.

Time Memory Cell

CMOS has two types of FET's in a chip, NMOS and PMOS, and both work like a switch. Leakage current is very low (< 1 nA), so the power consumption is almost negligible under static condition. Power is consumed when the transition occurs in a gate; to charge and discharge load capacitance. We choose series of memories to record timing information instead of shift registers moving fast. Because power consumption would be minimized by reducing number of switching elements

Fig.1 - (a) shows structure of the basic time memory cell and Fig.1 - (b) shows a row memory cell which consists of series of basic memory cell. The basic memory cell consists of a delay element (two abutting inverters) and a memory (Three-Transistor RAM [1]). Propagation delay of 1 ns for each delay element can be achieved by recent CMOS technology. Charge is stored in the gate capacitance of M2 (~ 0.02 pF) when the write gate is on and the signal is high.

Fig.2 shows waveform studied by SPICE2G electric circuit simulator[2]. Node capacitance and line resistance are estimated from possible layout, and MOS FET parameters are taken from reference [3]. Pulse of 2 ns width runs series of delay element (node 2-5) which opens gate of each memory cell in succession. Little charge is stored in the off-timing

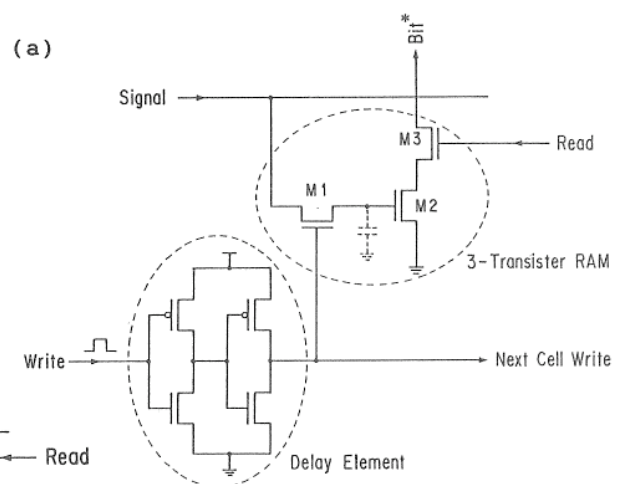


Fig.1 (a) Basic Time Memory Cell. Charge is stored in the gate capacitance of M2 Transistor. (b) Row Memory Cells. Numbers indicated are node numbers.

cell (node 7), but enough charge to switch on the transistor M2 is stored in the on-timing cell (node 8-10). Leakage current is low enough for keeping information until trigger decision time. These information are read from bit line by opens read gate (Fig.3).

Uniformity of Delay

The most critical item of the TMC is uniformity of delay time in the delay chain. Absolute value of each delay element is not so important, if we can calibrate each chip or channel. Deviation around the mean value of delay must be suppressed within $\pm 10\%$ to achieve less than ± 0.5 ns deviation at 16th memory cell. Careful layout of each element and special treatment to control line-width at the silicon process may be required.

Drift of Delay

Considerable source of drift of delay are change of carrier mobility due to temperature shift, and change of drain current due to drift of supply voltage. Carrier mobility is depend on temperature as follows[3];

$$\mu(T2) = \mu(T1) \times (T1/T2)^M ,$$

where μ is a characteristic mobility, T1 and T2 is temperature, and M is an empirical constant ($M \approx 1.6$ [3]). Since gate delay (τ) is roughly proportional to the mobility, we have

$$d\tau/dT \approx 0.5 \%/degree \quad (\text{around } 300K).$$

Drain current is roughly proportional to the drain-source voltage of FET, the deviation of gate delay ends up with inversely proportional to deviation of supply voltage. Change of the supply voltage will

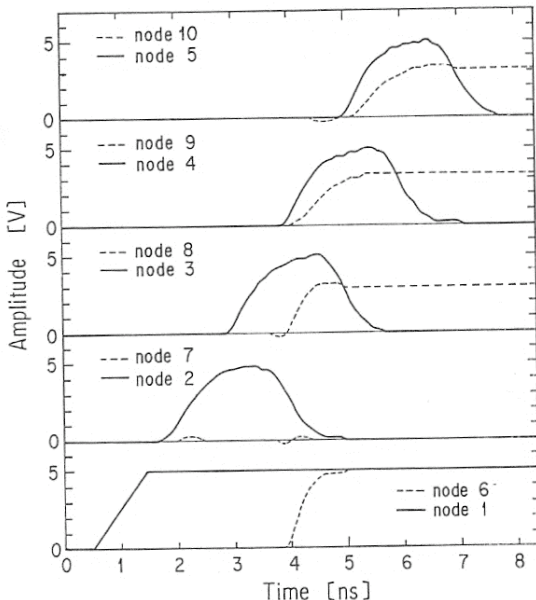


Fig.2 Waveform of each node from simulation of SPICE2G. Circuits and node number are shown in Fig.2. Node 1 : a write clock (beam-crossing signal), Node 2-5 : waveform of delay element chain, Node 6 : an input signal, Node 7-10 : signal and stored voltage in each memory cell.

also occur locally inside the chip. So the design of the chip layout must be careful to reduce voltage drop in the power and ground lines. The delay is not affected much on the change of threshold voltage because of fast rise time and symmetric structure of CMOS.

The drift of delay is accumulated linearly for 16 elements, so that drift of delay for each element should be controlled within $\pm 3\%$. With careful design and operation, we can handle the drift of delay within ± 0.5 ns.

TMC Chip Design for Central Tracker

Fig.4 shows block diagram of the TMC. Following conditions are considered in designing the TMC for tracking device readout.

1. Multihit capability should be included. Any pulse separated more than 1 ns can be recorded in the memory cell, so that the TMC have multihit capability.
2. Beam crossing time is 16 ns, and required time resolution for the tracking device is about 1 ns. So the required depth of one row of the memory cells is 16.
3. Maximum drift time is less than 100 ns, so the number of row need to store one event is about 6.
4. The information must be stored until the first level trigger issued (~ 500 ns). So the number of row need to implement is more than 32.
5. It is desirable to implement 8 channel in a chip.
6. We assume the information from tracking chamber is not used for first and second level trigger. So we have $10 \mu s$ (second level trigger decision time) for readout. This enables us to send the data in serial.
7. The circuit should have several buffers to avoid deadtime.

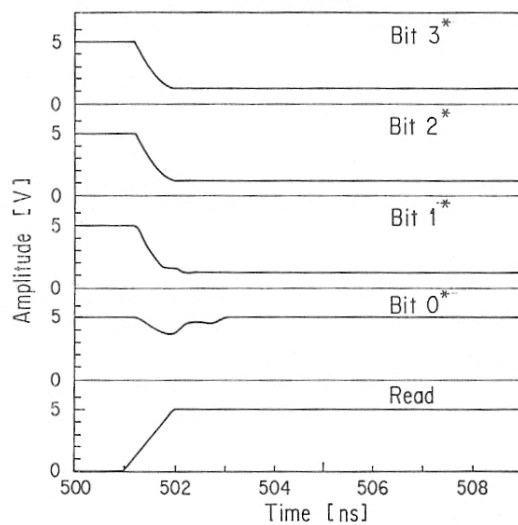


Fig.3 Read and Bit line signals at readout time. Bit 0* is read as 1, and Bit 1*, 2* and 3* are read as 0.

Power consumption of this TMC chip is estimated to be 0.1 W/chip (8 channel) as follows. Power consumption (P) of a CMOS gate is calculated from

$$P = C \times V^2 \times f$$

where C is load capacitance, V is supply voltage and f is switching frequency. Load capacitance in 2 μm CMOS process is estimated to be C ~ 0.08 pF for memory cell. In every 16 ns (62.5 MHz), 48 gates (3 gate/cell x 16 cell) and several buffers are switching in one channel. Then power consumption in memory cell part is

$$P_{ch} \cong 0.08 \text{ pF} \times (5 \text{ V})^2 \times 62.5 \text{ MHz} \times 48 \text{ gates} \\ \cong 0.006 \text{ W/ch}$$

Power consumption in other element, such as buffer and clock distributor is estimated to be the same order of that of memory part. That turn out to be 0.012 W/channel.

For 100k channel of central tracker, total power consumption of TMC amounts to 1.2 kW. This low power consumption sounds extremely attractive for SSC central tracker at the cooling point of view.

Readout Scheme for Central Tracker

We show a possible scheme of readout system for the SSC central tracking device in Fig. 5. Z-position (along the beam axis) is measured by stereo-wires, so all the information to read is timing. Signal from the tracking device through preamp, shaper and discriminator chain will enter the memory cell of the TMC. Row's of the memory cell make something like a ring buffer, and rotate every 16 ns.

If the first level trigger was issued at 500 ns later, the event information (16 bit x 6 row) which is stored 500 ns ago was sent to the FIFO-1. Writing speed of the FIFO-1 must be faster than 16 ns to make a deadtimeless operation. Then we wait for the second level trigger. The FIFO-1 should have two or more event depth to reduce deadtime.

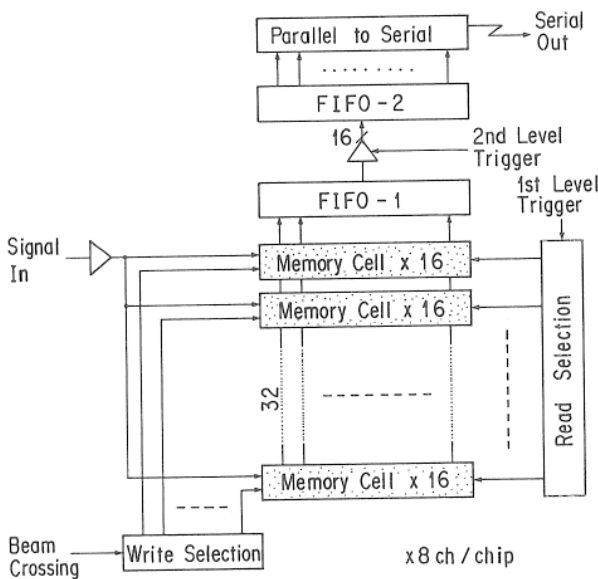


Fig.4 Block diagram of Time Memory Cell.

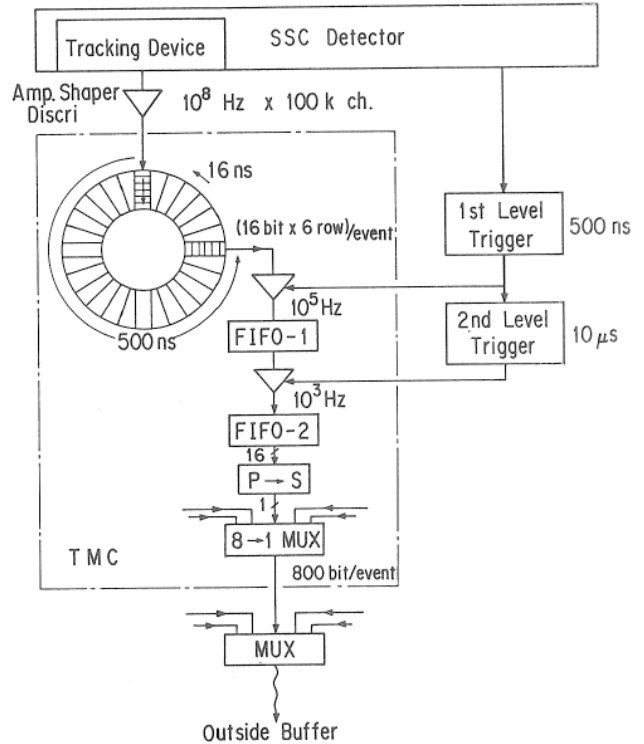


Fig.5 Readout scheme for SSC tracking device using the TMC.

If the second level trigger was issued at 10 μs later, the data was sent to the FIFO-2. The FIFO-2 also should have two or more depth. Contents of FIFO-2 memory are transferred to the parallel-serial translator, then 8 channels are multiplexed inside the TMC chip. As the data size produced in the TMC per event is estimated to be about 100 bit/channel, we may have additional multiplexing of 4 ~ 8 at outside chip. Even we have redundant system, the number of cables can be reduced factor 16 ~ 32.

Conclusion

We have proposed a readout scheme for the SSC central tracking device introducing a new idea of LSI chip "TMC". This readout scheme can be applicable to the other tracking device such as a forward tracker and muon chamber for SSC. Obviously substantial investigation is necessary to make realistic LSI. Further improvement in resolution can be expected by using new device such as GaAs.

Acknowledgement

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References

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