Application of Novel technologies for Development of the ATLAS End-cap Muon Trigger Electronics System at the Large Hadron Collider

A Dissertation

for the degree of Master of Science

in Physics

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January 2002

Acknowledgement

First of all, I am deeply thankful to Prof. Chikara Fukunaga who always encouraged strongly, taught carefully and helped constantly in all.

I also would like to especially thank Prof. Osamu Sasaki who teaches me valuable things concerned with electronics and study. I give my special thanks to Mr. Masahiro Ikeno who advises me the technique for actually creating electronics including development of circuits. I also really thank Prof. Takahiko Kondo, Prof. Hiroyuki Iwasaki, Prof. Tomio Kobayashi, Prof. Hiroshi Sakamoto, Prof. Hisaya Kurashige, Dr. Yasuo Arai, Dr. Kazumi Hasuko and Dr. Hiroyuki Kano for supporting me in various scenes. I want to be thankful ATLAS TGC chamber group members; Dr. Shuji Tanaka, Dr. Koji Ishii, Dr. Masaya Ishino, and Dr. Atsuhiko Ochi. And I would like to thank my companies who study together; Yuichi Katori, Yoshio Nakamura, Yu Matsumoto, Kentaro Mizouchi, Shinsuke Tsuji, and Ryo Ichimiya. And I also would like to thank Kenichi Tanaka and Satoru Komatsu who study together in the same laboratory.

I thank all members in ATLAS group.

Finally, I am thankful to my parents, brothers, and grandparents for continuous encouragement and supporting.

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Abstract

The ATLAS (A Toroidal LHC ApparatuS) experiment is an experiment using the ATLAS detector, which is a large-sized general-purpose detector installed in the LHC (Large Hadron Collider) that is now under construction at the CERN laboratory. The start of the experiment is planned from 2006. It is expected the discovery of the undiscovered particles, especially Higgs bosons that is only yet undiscovered particle predicted by the standard model using the proton collision energy of 14TeV in a center-of-mass system. In addition, it is expected that the discovery and analysis of various physical phenomena which are not well studied until now, such as supersymmetric particle search, top quark decay, and the CP-violation with b-quark decay.

In the ATLAS detector, although proton-proton collision will be occurred every 25ns, most of collisions will not be a head-on collision of proton-proton. The particles coming from the collisions other than head-on one become the noise called background. In order to suppress background and identify the particles coming from a head-on collision, an implementation of a sophisticated trigger system is essential. We have designed a so-called Level-1 Trigger System using muon to identify the head-on collision. Muon is known as stable, and long-lived particle. It has small interactional cross-section with the detector materials. To use muon, it has ideal to identify the event from head-on collision.

In order to take out these information, the information what, when, and where particles are detected is required, and especially in order that particles may pass through a detector at high speed, it is needed the high-speed data processing and transmission. And high-speed data transmission is the important element in order to prevent lack of data, and the high-speed data link system for it is needed. Moreover, since the ATLAS detector is very large, when a gap arises at the time of event, it may become that adjustment with other physical phenomena cannot be taken and it cannot analyze even if a certain important physical target phenomenon occurs, or overlooking physical related phenomena. Therefore, it is necessary to set up a common time-axis, and the TTC (Timing,

Trigger, and Control) system is developed for it. However the common standard is only decided corresponding to all experiments using LHC, these systems are not the specialized systems in each detector.
In this research, the specialized system in the electronics for TGC (Thin Gap Chamber) which is one of the muon detectors in the ATLAS experiment is built. Moreover the required modules for the system and the TTC emulator for development of TGC electronics are developed.

Furthermore, although ICs used for these systems including TGC electronics are custom ICs and industrial purpose ICs which are generally sold, it needs to confirm whether these ICs are infected from the environment of the ATLAS experiment and especially generated various radiational particles.

In this research, the γ-ray irradiation experiment in the University of Tokyo and the proton irradiation experiment in Tohoku University are conducted, and these results are summarized.

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1, Introduction

The LHC (Large Hadron Collider) Project[1] is the largest scale of physics experiment that was not until today, and the LHC is an accelerator that brings protons and ions into head-on collisions at higher energies than ever achieved before. And this will allow us to penetrate still further into the structure of matter and recreate the conditions prevailing in the early universe, just after the "Big Bang".

The ATLAS (A Toroidal LHC ApparatuS) experiment[2] uses this Collider, and this detector is under construction at the CERN (European Organization for Nuclear Research) Laboratory in Geneva, Switzerland. Its goal is the discovery of Higgs particle, and exploring the fundamental nature of matter and the basic forces which shape our universe. For achievement of the goals, many highly precise detectors are required, and the number of the data collected from them will become huge quantity. Therefore, a data acquisition (DAQ) system which can choose efficiently only the data about the physical target phenomenon is needed. Moreover, it not only collects data efficiently by this DAQ system, but it is important whether the right data as a physical target phenomenon is collected. A trigger system is for judging whether the data is the physical target phenomenon. In ATLAS experiment, it has three steps of trigger systems, and it is designed so that efficient data acquisition can be performed by combining trigger and DAQ systems.

In the trigger system and DAQ system, control of the time-axis is important. For example, even if each group analyzes acquisitional data freely in each portion of ATLAS detector, the adjustment of data with other portions cannot be taken. Therefore important physical phenomena may be overlooked. Since it should not become such a thing, in the experiment which used LHC containing ATLAS, the system for forming a common time scale called TTC (Timing, Trigger, and Control) system is built. However, it is meaningless if it is not well made adapted for an actual experiment even if it only merely forms the system. Therefore the author improved so that the actual experiment might be suited (to TGC electronics which belongs in this case), and he created the emulator so that simpler handling could be performed.

[1] http://lhc.web.cern.ch/lhc/
[2] http://atlasinfo.cern.ch/Atlas/

Although TTC was explained, this is the system only for trigger, and the information about the trigger is added and this information is very large in the case of actual data collection. In order to send this to other modules or to collect data to form trigger signals, it is necessary to send large data quickly. Therefore, a high-speed data link system is required. There is the following system for high-speed data link; the G-Link system that can transmit data in gigabit rate, the LVDS system that can transmit data with little attenuation. These systems are already used by many scenes in the general environment. However there are few examples of using them in the experiment under special environment like the ATLAS experiment, especially radiation environment, and we don't know whether these system and electronics operate correctly or not. Therefore, it is necessary to confirm whether to be actually applying radiation and operating correctly.

It is described the physics goals of the ATLAS experiment at first in Chapter 2.
Next, In Chapter 3, it is made to explain through the whole image what role the trigger system and DAQ system including TTC system are bearing in the ATLAS experiment.
In Chapter 4, it explains in detail about the TTC system itself, and the research and work which the author performed are described. You would like to note how the emulator is simpler than the original system. In Chapter 5, many kinds of ICs are used in ATLAS TGC electronics system. However it is impossible to use unless we have clear ideas about characteristic of them for operation in high radioactive environment like vicinity of the detector. We have made a test environment for them in a special radioactive environment. The results of the test are summarized in this chapter.

2, Physics goals of the ATLAS Experiment

2.1 Target of LHC and ATLAS Experiment

The LHC (Large Hadron Collider) experiments including the ATLAS experiment are ones of the grand scales which have not reached until now. In the LHC the energy available in the collisions between the constituents of the protons (the quarks and gluons) will reach the TeV range, which is about 10 times that of LEP (Large Electron Positron Collider) and the Tevatron (Fermilab). In order to maintain an equally effective physics program at a higher energy E, the luminosity of a collider (a quantity proportional to the number of collisions per second) should increase in proportion to E^2. This is because the De Broglie wavelength associated to a particle decreases like 1/E and hence the cross section of the particle decreases like $1/E^2$. Whereas in past and present colliders the luminosity culminates around $L = 10^{32} cm^{-2} s^{-1}$, in the LHC it will reach $L = 10^{34} cm^{-2} s^{-1}$. This will be achieved by filling each of the two rings with 2808 bunches of 10^{11} particles each. The resulting large beam current (I_b = 0.53A) is especially challenge in a machine made of delicate super conducting magnets operating at cryogenic temperatures.

LHC and ATLAS have many goals of physics. One of the most important goals is measurement that will lead to an understanding of the mechanism of electroweak symmetry breaking. The high energy and luminosity of LHC offer a large range of physics opportunities, from the precise measurement of the properties of known objects to the exploration of the high energy frontier. The need to accommodate the very large spectrum of possible physics signatures has guided the optimization of the detector design. The desire to probe the origin of the electroweak scale leads to a major focus on the Higgs boson; ATLAS must be sensitive to it over the full range of predicted masses. Other important goals are searches for other phenomena possibly related to the symmetry breaking, such as particles predicted by supersymmetry or technicolour theories, as well as new gauge bosons and evidence for composite quarks and leptons. The investigation of CP violation in B decays and the precision measurements of W and top-quark masses and triple gauge boson couplings will also be important components of the ATLAS physics program. In this chapter, it is explained about Higgs boson and Supersymmetry (SUSY) particles.

2.2 Higgs boson of Standard theory

The Higgs boson is of critical importance in particle theories and is directly related to the concept of particle mass, therefore Higgs is related to all masses. Then we think why do the fundamental particles have mass, and why are their masses different? It is remarkable that a concept as familiar as mass was not understood until the proposal of the Standard Model.

The Standard Model proposes that there is another field not yet observed, a field that is almost indistinguishable from vacuum space. We call this the Higgs field. We think that all of space is filled with this field, and that by interacting with this field, particles acquire their masses. Particles that interact strongly with the Higgs field are heavy, while those that interact weakly are light.

The Higgs field has at least one new particle associated with it, the Higgs boson. The ATLAS detector must be able to detect this particle if it exists.

The main processes of Higgs generation are the following 4 processes.

- gg → H_{SM}^{0} (gluon fusion)

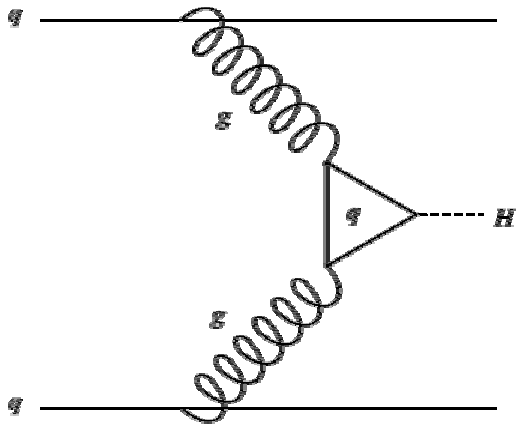

Figure 2-1 gluon fusion

Figure 2-1 shows gluon fusion reaction. The generation cross-section of this process through the loop of Top or Bottom quark is 20pb (M_H = 160GeV). However, since there is no High-pT particle in this process without the particles generated by decay of Higgs, there are many background particles and this process will be difficult to observe experimentally.

- qq → qq H_{SM}^0 (W/Z fusion)

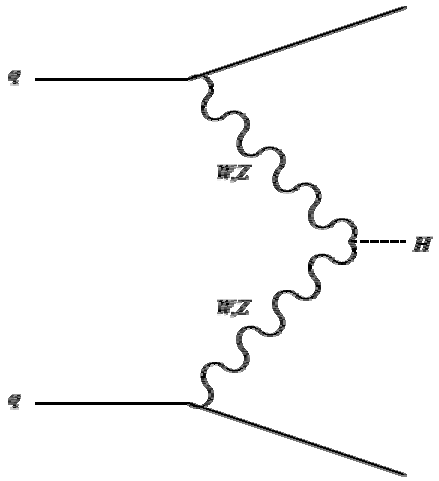

Figure 2-2 W/Z fusion

Figure 2-2 shows W/Z fusion reaction. The H_{SM}^0 is generated by two Gauge bosons emitted from two quarks. This cross-section is 3.5pb (M_H = 160GeV), and the two jets with High-pT resulting from the two quarks will be observed.

- qq → (W/Z) H_{SM}^0 (W/Z associate production)

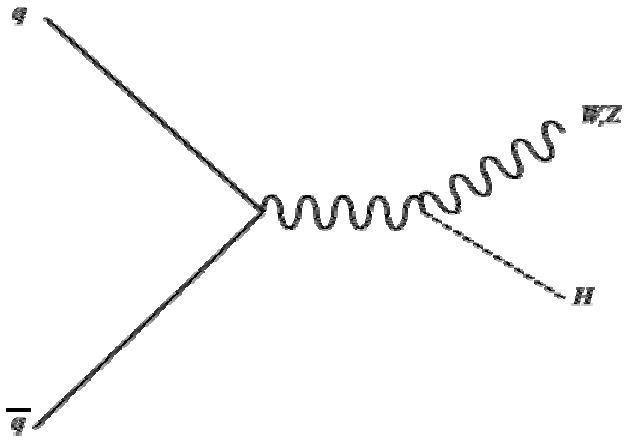

Figure 2-3 W/Z associate production

Figure 2-3 shows W/Z associate production. This process is H_{SM}^0 emission from Gauge boson generated by annihilation of quark pair, and this cross-section is 1.2pb (M_H = 160GeV). It has a character that Gauge boson (W/Z) is observed in the final state.

- qq/gg → tt H_{SM}^0 (top associate production)

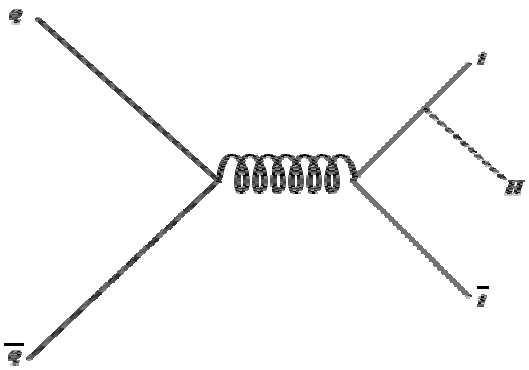

Figure 2-4 top associate production

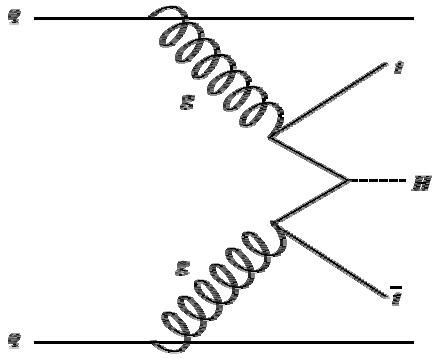

Figure 2-5 top associate production

Figure 2-4,5 show top associate production. This process is H_{SM}^0 emission from pair production of top quark. This cross-section is small as 0.16pb (M_H = 160GeV), however there are little background particles because of including the characteristic top quark in the final state. This is an important process for light H_{SM}^0.

In fig. 2-6[1] we show the cross-section dependences of the mass of Higgs boson for these processes.

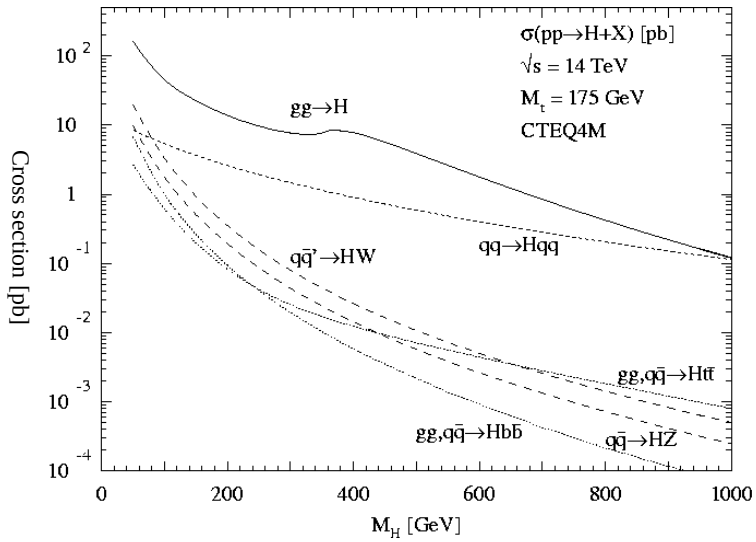

Figure 2-6 Cross-section of Higgs generation processes

[1] http://atlphy01.kek.jp/~asai/ATLAS/Higgs1.html

Figure 2-7[2] is the branching ratio of decay processes of the Higgs boson predicted in the standard model. If the mass of Higgs is lighter than 130GeV, Higgs decays to $b\bar{b}$ mainly. And if it is heavier than 130GeV, Higgs decays to WW or ZZ mainly. In the domain of Higgs mass (120-200GeV) which is the target mass for LHC, in order to change quickly for search mode for higgs, it is necessary to cover the five modes which are bb, WW, ZZ, ττ, and γγ completely.

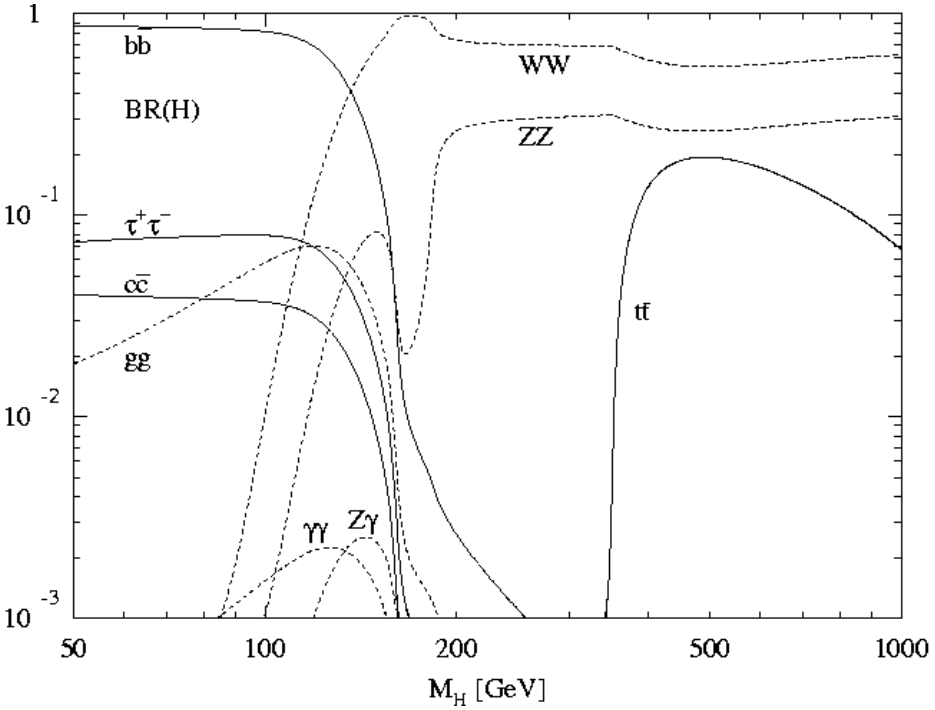

Figure 2-7 Branching ratio of decay process of Higgs boson

The detector sensitivity for the discovery of H_{SM}^0 in the ATLAS experiment is shown in Fig. 2-8[3]. The statistical significances are plotted for individual channels, as well as the combination of all channels, assuming integrated luminosities of $100fb^{-1}$. Depending on the numbers of signal and background events, the statistical significance has been computed.

[2] http://atlphy01.kek.jp/~asai/ATLAS/Higgs1.html
[3] ATLAS collaboration, *"ATLAS Detector And Physics Performance Technical Design Report"*, ATLAS TDR 15, CERN/LHCC 99-15, 25 May 1999.

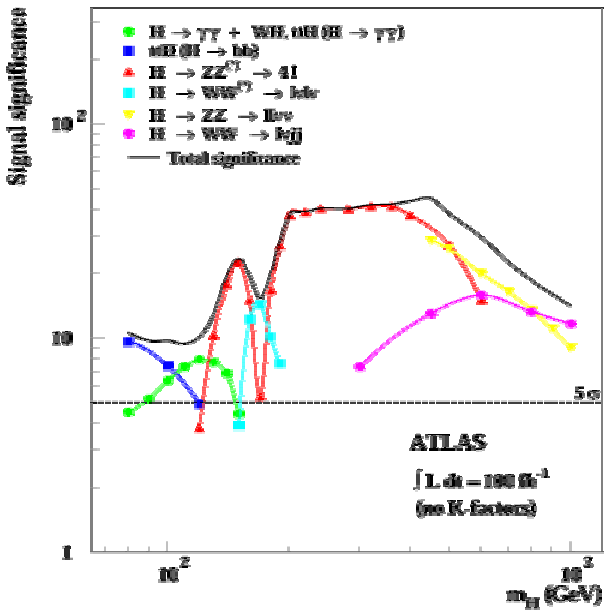

Figure 2-8 The detector sensitivity for the discovery of H_{SM}^0 in ATLAS experiment

2.3 Higgs boson of Supersymmetry

Since two Higgs doublets ($H_u=(H_u^+,H_u^0)$, $H_d=(H_d^0,H_d^-)$) are needed by Minimal Supersymmetric Standard Model (MSSM) in Supersymmetry (SUSY) theory, there are two charged and three neutral Higgs bosons ($H^\pm$, h^0, H^0, A^0). The following sentences explain characteristic decay process in MSSM.

- H/A → ττ

In the Standard theory, since H → ττ mode is low rate detection[4], it is not suitable for measurement. However, in MSSM, high rate detection is expected. In order to ensure two τ decay mode for the higgs decay, we have to look for two channels from ττ; the one is a mode of which the each τ decays into lepton, and the other one is a mode of which one τ decays into hadron(s).

[4] Optimistic recent theoretical estimates. D. Rainwater, D. Zeppenfeld, Phys. Rev. D59 (1999) 14037.

- H/A → μμ

The production decay of this mode is the same as the previous one of H → ττ. Although the branch ratio is smaller $(m_\mu/m_\tau)^2$ times than ττ process, it can be measured with sufficient accuracy since the muon detector system of the ATLAS detector is so well optimized to measure an isolated muon as described in the following section. Therefore compensating measurement in ττ process is expected.

- H → hh

The main decay process is H→hh → $bb\overline{bb}$, and this decay rate is predicted as low. Therefore efficient triggers cannot be performed in this process. It is expected that this process is observed in hh → $\gamma\gamma b\bar{b}$ process.

- A → Zh

The method of triggering by two leptons which produced by the decay of Z, such as Zh → $llb\bar{b}$, is effective.

2.4 The particles of Supersymmetry

In LHC, the discovery of supersymmetry particles, for example, the pair of squark ($\tilde{q}$) and gluino ($\tilde{g}$) that have strong interaction are generated in large quantities, is expected. From the R-parity preservation rule, supersymmetry particles are surely generated by the pair and decays to LSP (Light Supersymmetry Particle) which finally has the lightest mass in supersymmetry particles. Neutralino ($\tilde{\nu}$) which has the lightest mass among the Supersymmetric world can be considered as a candidate of LSP. Since this particle will not be detected and will appear as missing transverse energy E_T^{miss} in the analysis of events, it is searched by indexing this E_T^{miss} with many jets of final state.
There are the following main decay processes;

- Multi-jets + E_T^{miss}

$$(\tilde{g} \to \tilde{q}q + \chi_1^0 \to jets + E_T^{miss}), \quad (\tilde{g} \to q\tilde{\chi}_1^0 \to jets + E_T^{miss}), \quad etc.$$

- Two leptons in like charges

$$2\tilde{g} \to 2(q\bar{q}\tilde{\chi}^{\pm}) \to 2(q\bar{q}W^{\pm}\tilde{\chi}_i^0) \to jets + l^{\pm} + E_T^{miss}, \quad etc.$$

- Three leptons

$$\tilde{\chi}_1^{\pm}\tilde{\chi}_2^0 \to l\nu\tilde{\chi}_1^0 + ll\tilde{\chi}_1^0 \to 3l + E_T^{miss}, \quad etc.$$

There are many processes including leptons in decay processes of Higgs boson and Supersymmetry. Especially, since muon is comparatively easy to discriminate, it is certainly detectable in high accuracy. An experiment for the Higgs and SUSY searches must have a very sophisticated muon trigger and detection system with high momentum measurement precision.

3, Outlook of the Experiment

3.1 LHC (Large Hadron Collider)

LHC stands for Large Hadron Collider, and this is a particle accelerator facility of the CERN Laboratory (Switzerland). LHC is now under construction astride the France-Switzerland border at west of Geneva, and operation is due to be started in 2006. LHC is installed in the existing LEP (Large Electron Positron Collider) tunnel, which is built about 100m below ground.

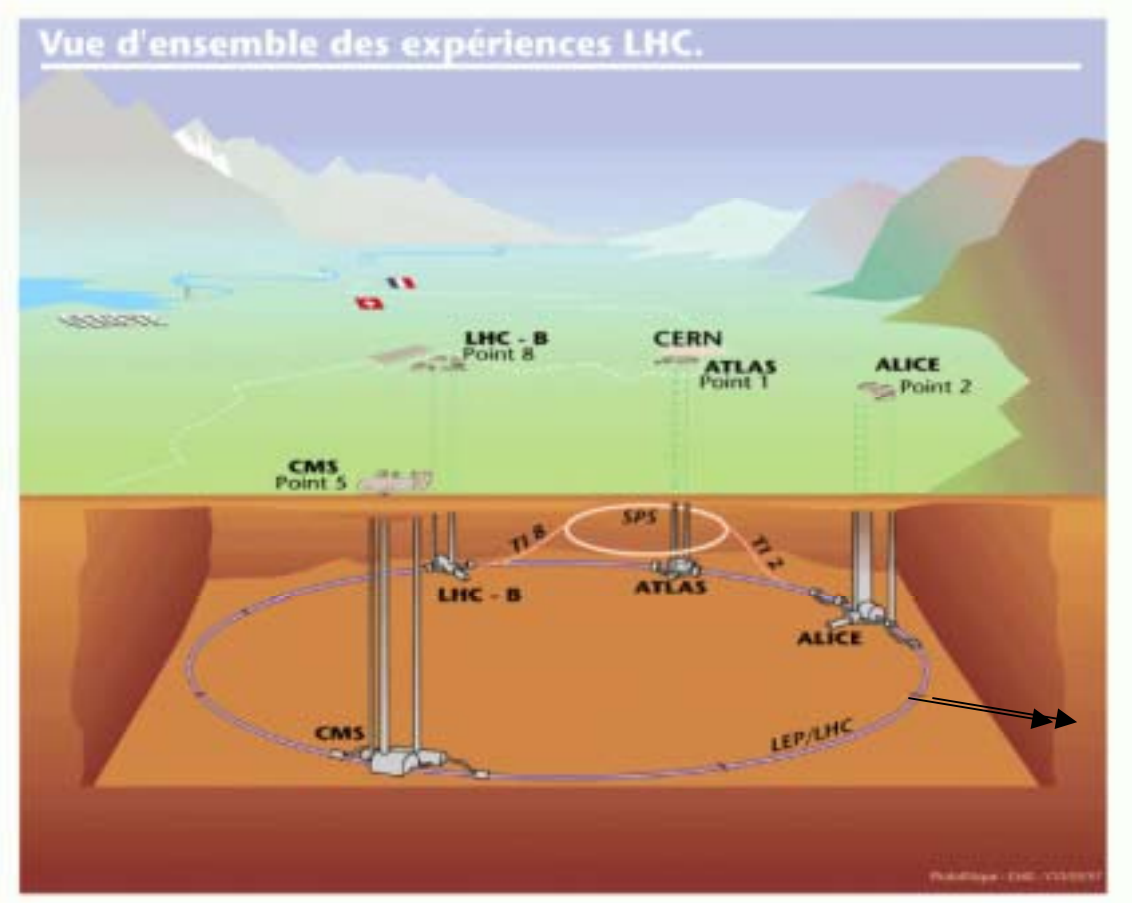

Figure 3-1 LHC Overview

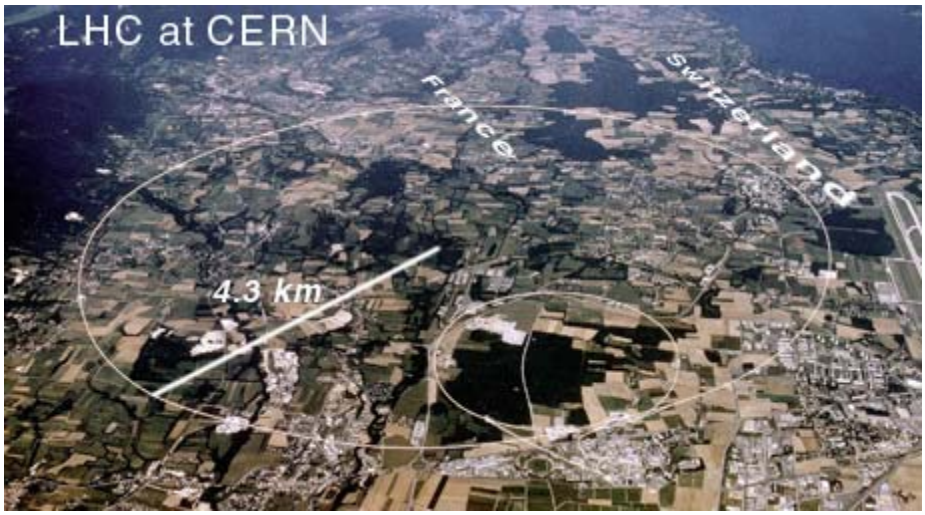

Figure 3-2 Bird's eye view of LHC

Table 3-1 is Main parameter of LHC.

Parameter	Unit	Low	Normal	High
Beam Energy	TeV		7	
No. of protons/bunch	10^{11}	0.17	1.1	1.67
No. of bunches		2808	2808	2808
Bunch separation	ns		24.95	
Bunch crossing rate	MHz		40.08	
Current	A	0.087	0.56	0.85
Luminosity	$10^{34}cm^{-2}s^{-1}$	0.1	1	2.3
Circumference	km	26.7		

Table 3-1 Main parameter of LHC

LHC has four bunch-collision points, and there is a detector per each point;

- ATLAS (A Toroidal LHC ApparatuS)

ATLAS is a general-purpose proton-proton detector designed to run at the highest luminosity at LHC. It is also well adopted for studies at the initially lower luminosity. The purpose is searching Higgs and studying physics in 14TeV proton-proton collision.

- CMS (The Compact Muon Solenoid)

CMS is also a general-purpose proton-proton detector. CMS has large solenoid coil, which allows all of the tracking devices and calorimetry to be placed inside the solenoid coil - resulting in a Compact overall detector. The purpose is searching Higgs and studying physics in 14TeV proton-proton collision.

- ALICE (A Large Ion Collider Experiment)

ALICE is an ultra-relativistic heavy ion collision detector to exploit the unique physics potential of nucleus-nucleus interactions. LHC will have facilities to circulate heavy ions and collide them beside proton-proton collision. The purpose is to study physics of strongly interacting matter at extreme energy densities.

- LHC-B (Large Hadron Collider Beauty experiment)

The purpose is to study CP violation and B physics. B mesons are most likely to emerge from collisions close to the beam direction, so the LHC-B detector is designed to catch low-angle particles.

The location of these detectors is shown in Fig. 3-1, The location of LHC is shown in Fig.3-2, and these overviews are shown in Fig. 3-3, 3-4, 3-5, and 3-6.

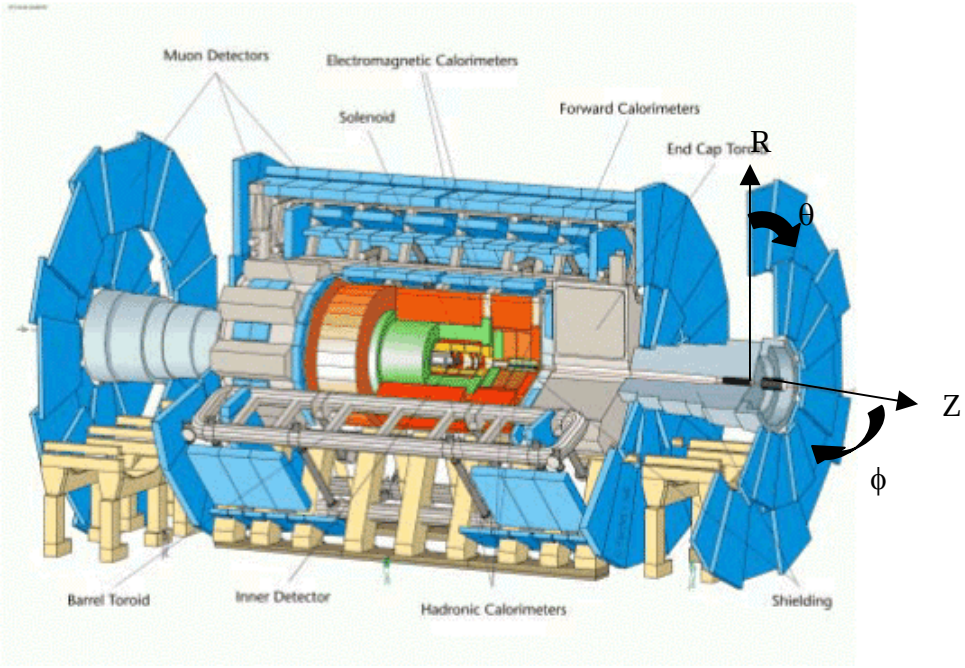

Figure 3-3 ATLAS

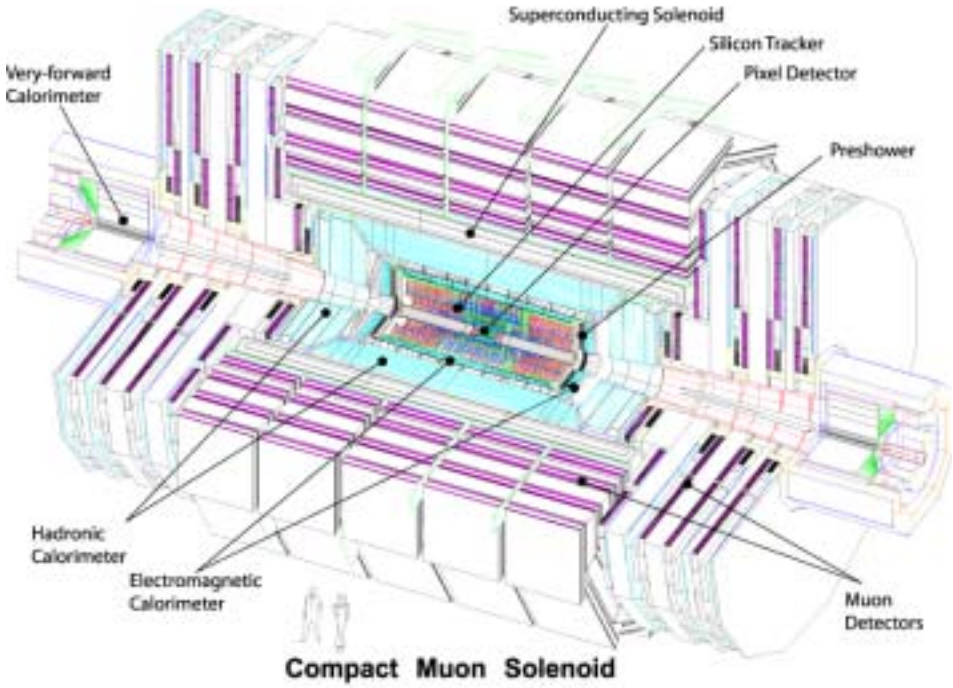

Figure 3-4 CMS

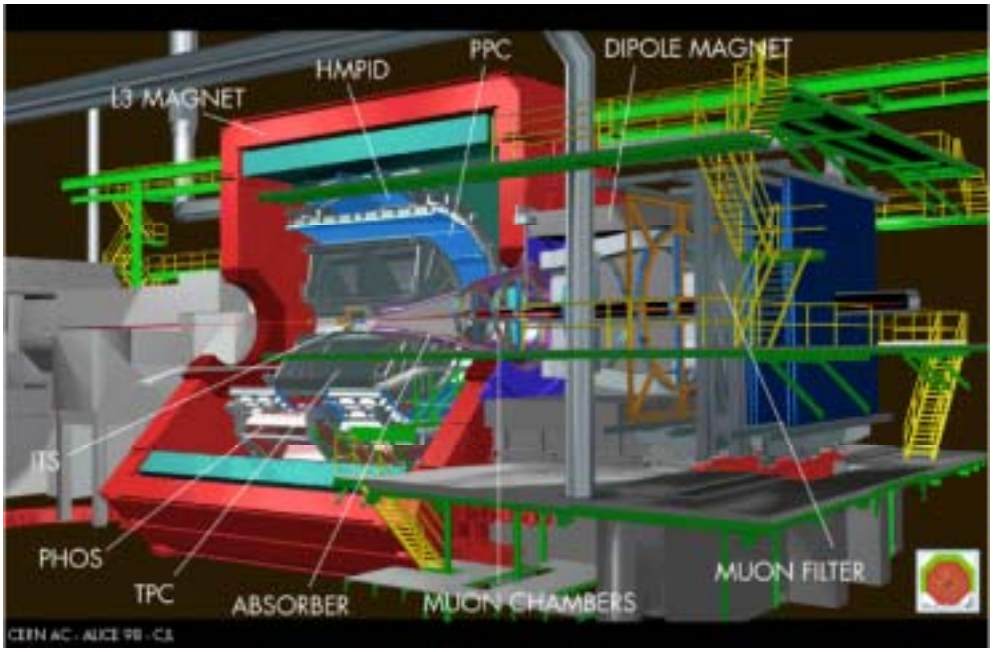

Figure 3-5 ALICE

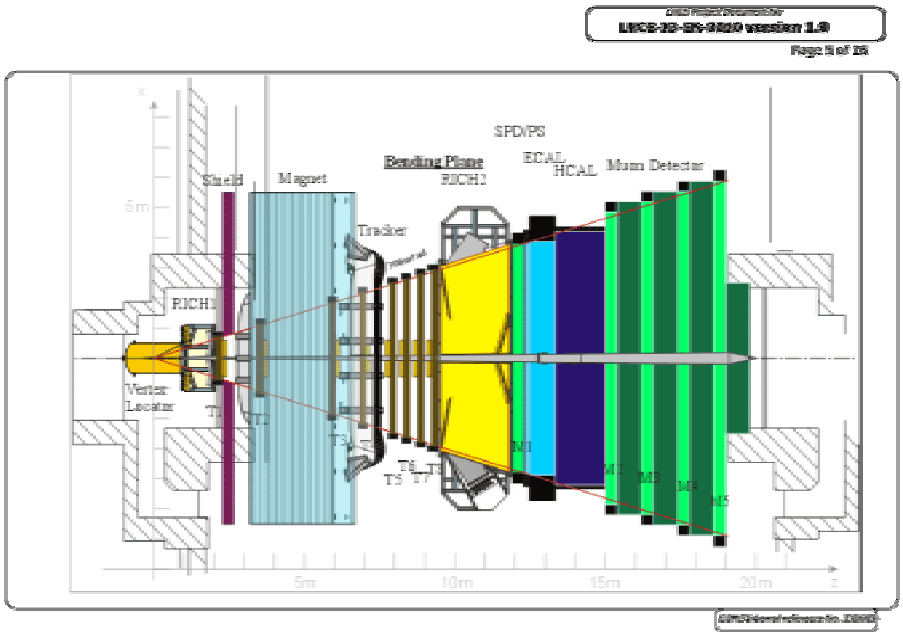

Figure 3-6 LHCB

3.2 ATLAS

The ATLAS experiment is one of the largest international projects, which consists of 34 countries, about 2000 scientists in 150 universities, and now has entered the construction phase for many of its detector components, with a strict schedule to meet the first collisions at LHC in 2006.

The Higgs is considered to the origin of mass introduced in the spontaneously symmetry-breaking mechanism and is the last elementary particle that should be discovered for the accomplishment of the Standard Model. It will be a great progress to find the Higgs and detailed study of its characteristics is desired. Another important goals are the search for heavy W- and Z-like object, for super symmetric particles, for compositeness of the fundamental fermions and detailed studies of the top quark.

The detector design criteria of the detector include as followings,

- good electromagnetic calorimetry for electron and photon identification and measurements, complemented by full-coverage hadronic calorimetry for accurate jet and

missing transverse energy (E_T^{miss}) measurements,

- high-precision muon momentum measurements, with the capability to guarantee accurate measurements at the highest luminosity using the external muon spectrometer alone,
- efficient tracking at high luminosity for high-pT lepton-momentum measurements, electron and photon identification, τ-lepton and heavy-flavor identification, and full event reconstruction capability at lower luminosity,
- large acceptance in pseudorapidity (η: $\eta = -\ln(\tan(\theta/2))$ with almost full azimuthal angle (ϕ) coverage everywhere. The azimuthal angle is measured around the beam axis, whereas pseudorapidity relates to the polar angle (θ) where θ is the angle from the *z* direction, and
- triggering and measurements of particles at low-pT thresholds, providing high efficiencies for most physics processes of interest at LHC.

The overall detector layout is shown in Fig. 3-3. This detector consists of four main components:

- Inner detector (measurement the momentum of each charged particles),
- Calorimeter (measurement the energies carried by the particles),
- Muon spectrometer (identify and detection muons), and
- Magnet system (bending charged particles for momentum measurement).

3.2.1 Inner detector

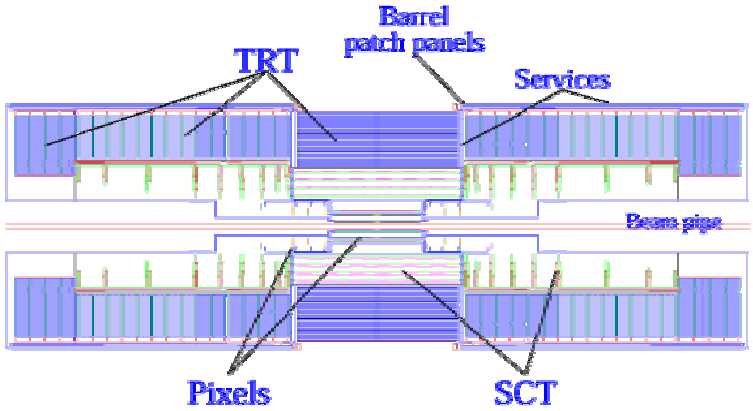

Figure 3-7 Inner detector

Figure 3-7 shows the cross-section of the Inner detector.

The Inner Detector consists of pixel, silicon, and TRT detector. This is contained within a cylinder of length 7 m and a radius of 1.15 m, in a solenoidal magnetic field of 2 T. Pattern recognition, momentum and vertex measurements, and electron identification are achieved with a combination of discrete high-resolution semiconductor pixel and strip detectors in the inner part of the tracking volume, and continuous straw-tube tracking detectors with transition radiation capability in its outer part.

3.2.2 Calorimeter

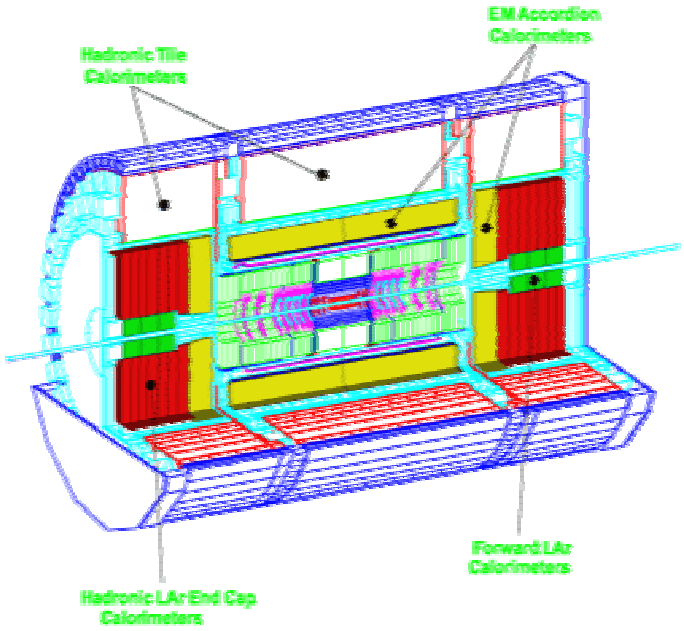

Figure 3-8 Calorimeter

Figure 3-8 shows the 3-D cross-section of Calorimeter.

The Calorimeter measures the energies of charged and neutral particles. This consists of an electromagnetic (EM) calorimeter, a hadronic barrel calorimeter, hadronic end-cap calorimeters, and forward calorimeters. And these calorimeters are constructed with metal plates (absorbers) and sensing elements. In the inner sections of the calorimeter, the sensing element is liquid argon (LAr). The showers in the argon liberate electrons that are collected and recorded. In the outer sections, the sensors are tiles of scintillating plastic. The showers cause the plastic to emit light that is detected and recorded.

3.2.3 Magnetic System

Figure 3-9 Solenoid coil

Magnet system consists of three kind of magnet (Solenoid, barrel Toroid, End-cap toroids) and bends charged particles for momentum measurement. The overall dimensions of the magnet system are 26m in length and 20m in diameter. The two end-cap toroids are inserted in the barrel toroid at each end. They have a length of 5m, an outer diameter of 10.7m and an inner bore of 1.65m. The central solenoid extends over a length of 5.3 m and has a bore of 2.4 m. The unusual configuration and large size make the magnet system a considerable challenge requiring careful engineering. Figure 3-9 shows Solenoid coil.

3.2.4 Muon Spectrometer

Muon spectrometer is based on the magnetic deflection of muon tracks in the large superconducting air-core toroid magnets, instrumented with separate trigger and high-precision tracking chambers. This consists of MDT (Monitored Drift Tube), CSC (Cathode Strip Chamber), RPC (Resistive Plate Chamber), and TGC (Thin Gap Chamber).

Figure 3-10 shows the layout of the muon spectrometer.

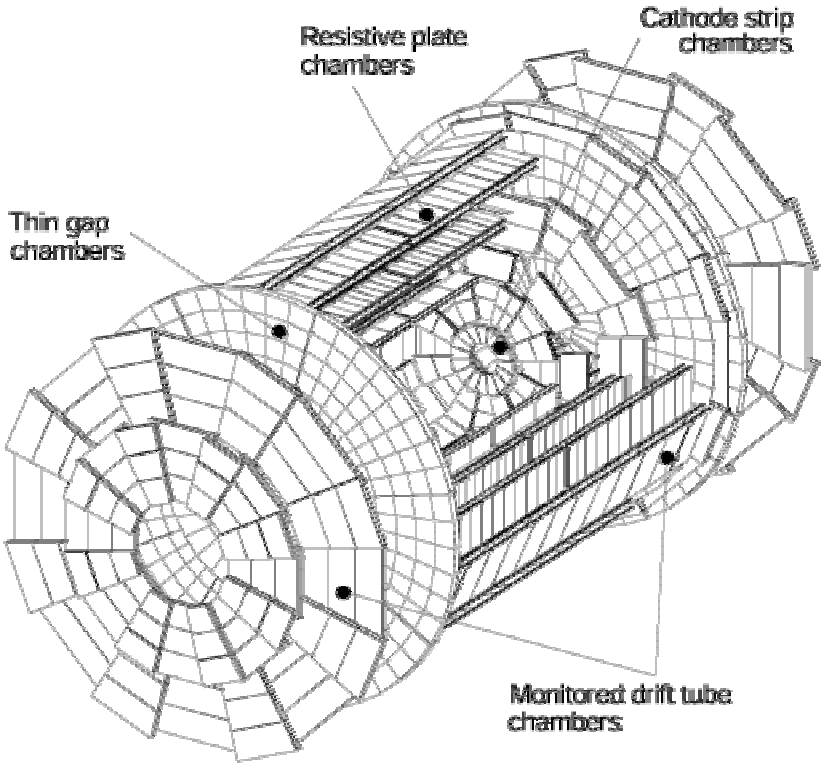

Figure 3-10 Muon Spectrometer

3.3 ATLAS trigger and Data Acquisition (DAQ) system

The ATLAS trigger and DAQ system is based on three levels of online event selection. Each trigger level refines the decisions made at the previous level and, where necessary, applies additional selection criteria. Starting from an initial bunch-crossing rate of 40.08 MHz, the rate of selected events must be reduced to ~100 Hz for permanent storage.

In this section, three levels of online event selection (Level-1, Level-2, Level-3 (Event Filter)) are discussed.

Figure 3-11 shows the block diagram of ATLAS trigger/DAQ system.

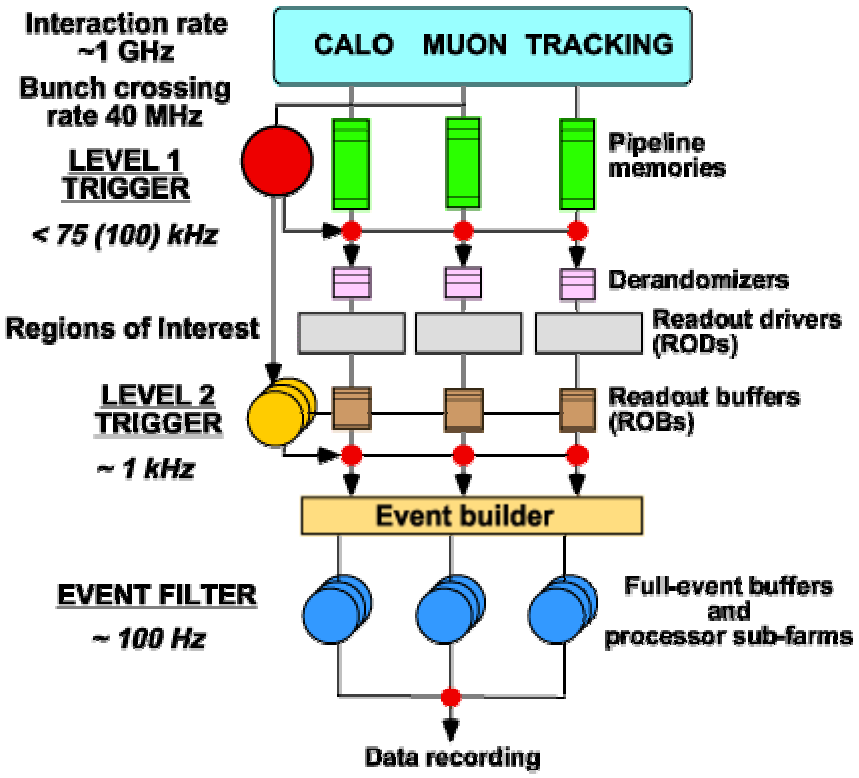

Figure 3-11 ATLAS trigger/DAQ system

3.3.1 Level-1 (LVL1) trigger system

3.3.1.1 Overview

In this section, the LVL1 trigger system to which the TGC trigger system belongs is explained. The LVL1 trigger system processes about calorimeter trigger and muon trigger based on the signals from calorimeters and muon trigger chambers. Final judgment for the LVL1 trigger is performed in CTP (Central Trigger Processor), this information signal (ROI: Regions of Interest) is sent to the LVL2 trigger system.

3.3.1.2 Level-1 muon trigger

The LVL1 muon trigger receives as input from TGC (Thin Gap Chamber) and RPC (Resistive Plate Chamber). TGC covers the end-cap, and RPC covers the barrel of ATLAS detector. Figure 3-12, 13,14 show these diagram.

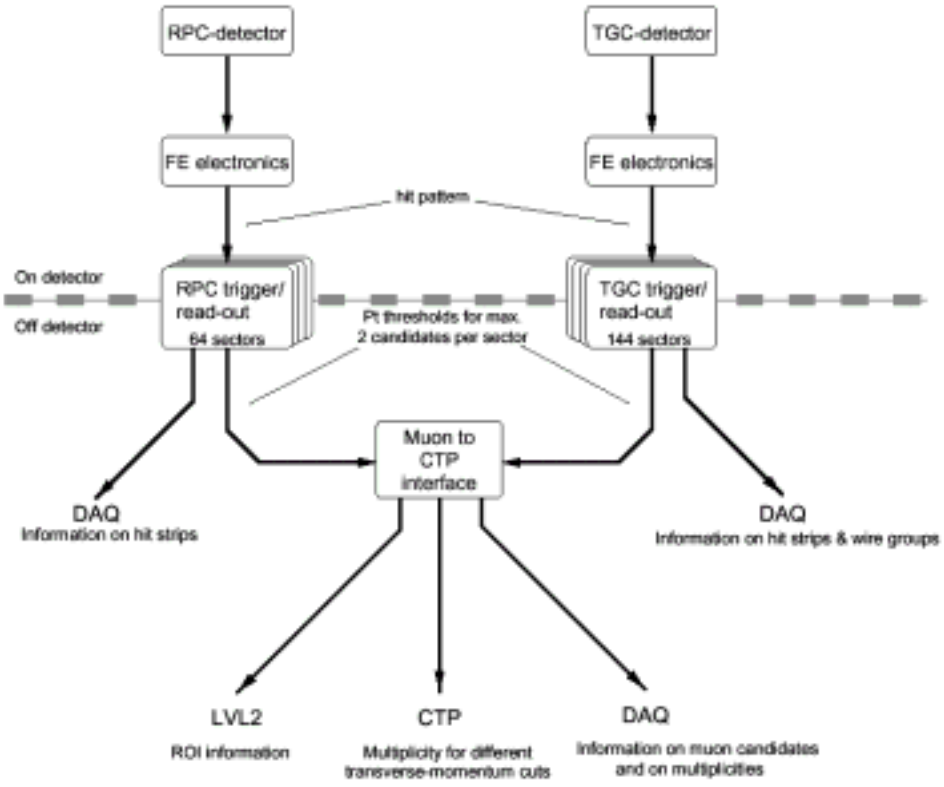

Figure 3-12 Block diagram of LVL1 trigger system of muon chambers

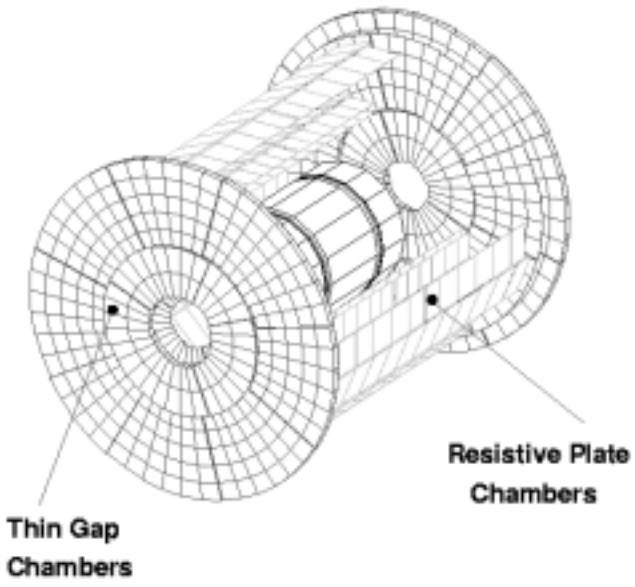

Figure 3-13 TGC and RPC

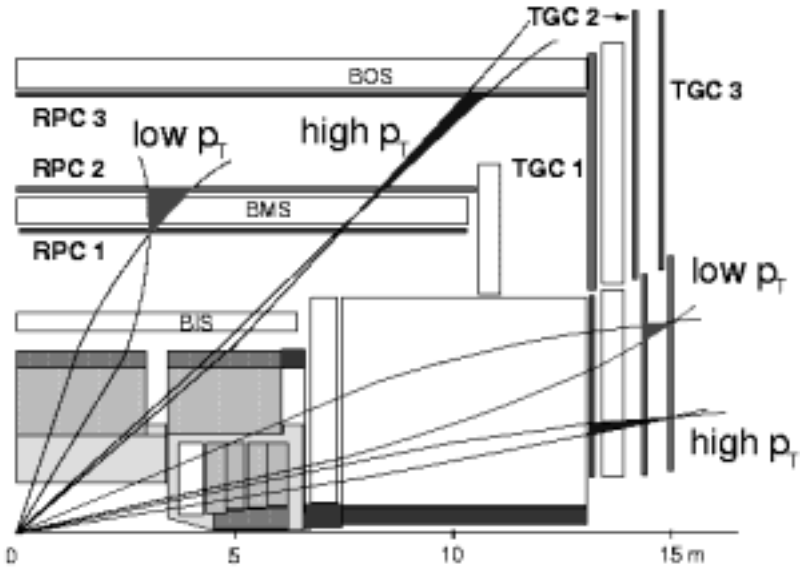

Figure 3-14 Layout of muon chamber

3.3.1.3 CTP

CTP stands for Central Trigger Processor, and the role of CTP is to combine the information for the different object types and to make the overall LVL1 trigger accept/reject decision. CTP receives muon information from muon chamber and other information (electron, photon, jet, and missing energy) from calorimeter, and CTP judges a trigger based on some degree of pT (transverse-momentum).

3.3.1.4 TTC

TTC stands for Timing, Trigger, and Control, and this system send TTC signals to the electronics system for all the ATLAS detector electronics. There are following signals handled by the TTC system;

- 40.08MHz LHC clock,
- LVL1 Accept signal for judgment of LVL1 trigger,
- Bunch-crossing identified number (BCID),
- Event identified number (EVID),
- Trigger-Type,
- Bunch-crossing identified number counter reset (BCR),
- Event identified number counter reset (ECR), and

- Control command and Data.

In chapter 4, TTC system is discussed again.

3.3.2 Level-2 (LVL2) trigger system

LVL2 trigger system processes the LVL1 trigger. Based on the space information accompanied with the LVL1, an ROI (Region Of Interest) in constructed around the hit points measured by the LVL1 detector components using all the detector position information. The LVL2 trigger refines the selection of candidate objects compared to LVL1, using full-granularity information from all detectors, including the inner tracker that is not used for LVL1. In this way, the rate can be reduced to 1kHz. Many events are analyzed concurrently by the LVL2 trigger system using processor farms, and an average latency of up to 100ms is considered reasonable.

3.3.3 Level-3 (LVL3) trigger system

LVL3 trigger system is also called Event Filter (EF). LVL3 trigger system processes the LVL2 trigger from Event builder and this trigger is fully built about event information using all acquired data. The maximum trigger rate is considered up to 100Hz. LVL3 trigger system is final section, therefore if a trigger data is passed LVL3 checking, this data is written down to storage medias and finally analyzed.

3.3.4 Data Acquisition (DAQ) system

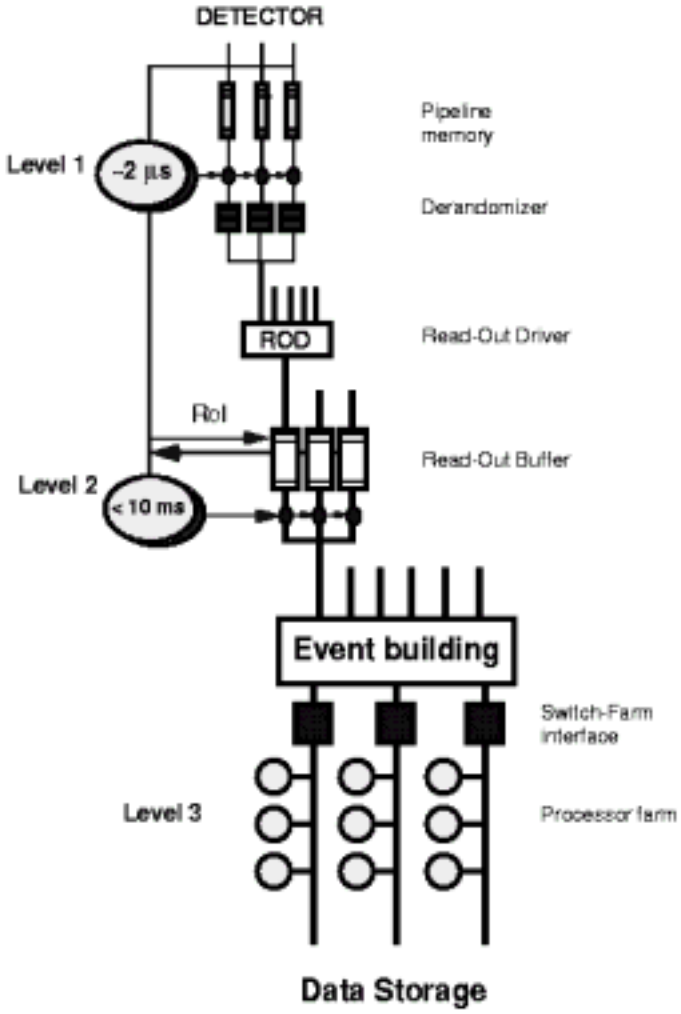

Figure 3-15 Data flow in DAQ system

The DAQ system is designed to take into account with each level trigger acceptance. In each level trigger processing, buffering memory are placed to keep the DAQ data for time long enough to accept the each trigger level latency. For the level-1 trigger buffer, for example, required buffering time are up to 2us and 10ms for the level-2 buffer.

Figure 3-15 shows the overview of ATLAS DAQ system.

3.4 TGC (Thin Gap Chamber) muon trigger system

3.4.1 Overview

TGC stands for Thin Gap Chamber, and is the muon tracking detector in the end-cap of the ATLAS detector. This chamber has very thin structure with the thickness of a few centimeters for lightness of the weight. Figure 3-16 shows a piece of Thin Gap Chamber.

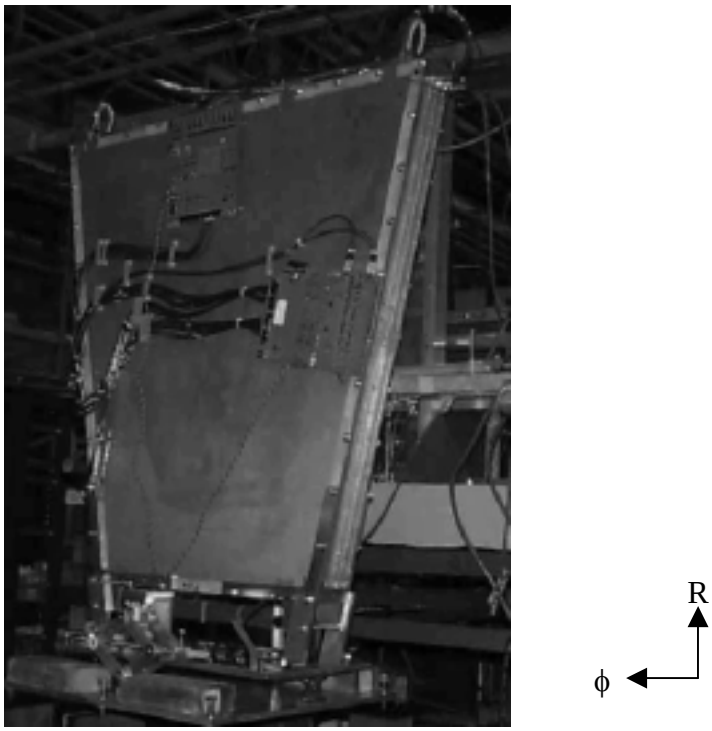

Figure 3-16 A piece of Thin Gap Chamber

As the thin structure gives good time response, this chamber is optimized for the LVL1 trigger decision detector. The size of TGC is about 1x2 meters and the thickness of about three centimeters. This chamber unit has about 200 wires along the transverse (R) direction and 30 pieces of copper strip on the one side of the surface along the longitudinal (ϕ) direction. Two-dimensional position information is obtained using both signals from wires and strips. Figure 3-17 shows the Layout of TGC.

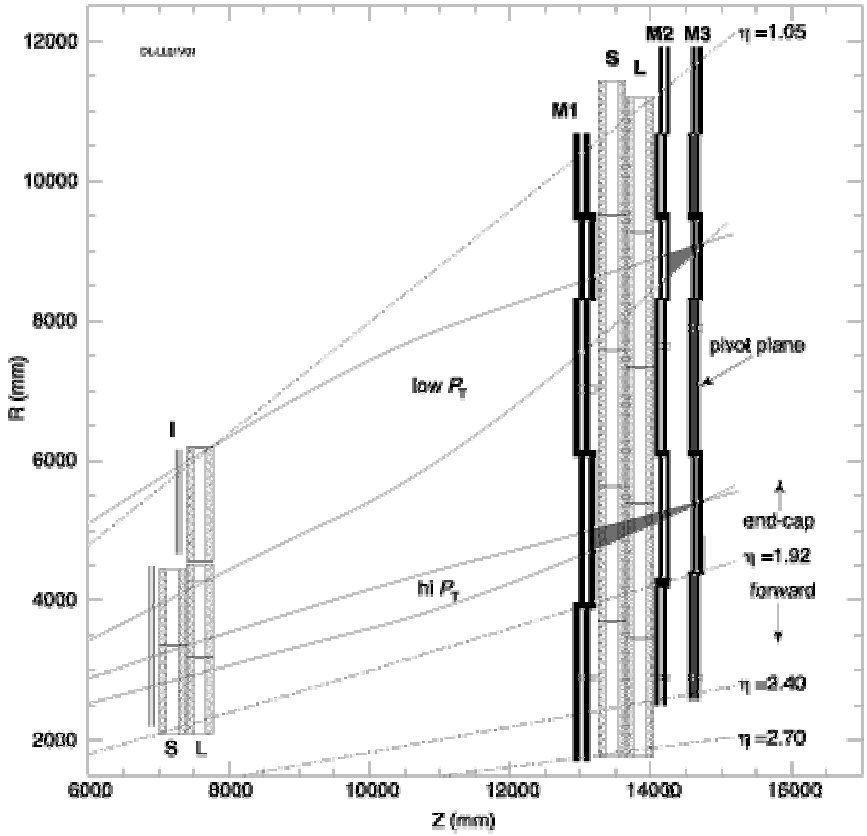

Figure 3-17 TGC layout (R-Z section)

3.4.2 Electronics system

The signals generated by TGC are amplified, discriminated and shaped in ASD (Amplifier Shaper Discriminator). ASD is an electronics component mounted on TGC directly, and the signals are sent to PP (Patch Panel). PP identifies the bunch-crossing and timing information of the ASD signals is sent to SLB (SLave Board). PP and SLB is mounted on PS board. SLB processes coincidences independently in R and ϕ roads. The coincidences provide R, dR and ϕ, dϕ, where R and ϕ are the track co-ordinates in the pivot plane and dR and dϕ are the track's deviation from the infinite momentum track. The signal from SLB is sent to High-pT, and the signal is checked pT (transverse momentum).

Electronics situated outside the ATLAS cavern, such as SL (Sector Logic) and ROD (Read-Out Driver), combines the measurements of R, dR and ϕ, dϕ to make a trigger decision which is then passed to the Muon Interface to the CTP, called MUCTPI. The

chamber hits and the intermediate R, dR and ϕ, dϕ values are read out by the on-detector electronics (Slave Board, Patch Panel, Star-SW, High-pT) and off-detector electronics (ROD, Sector Logic, Local DAQ Master). Figure 3-18 shows the diagram of TGC electronics location.

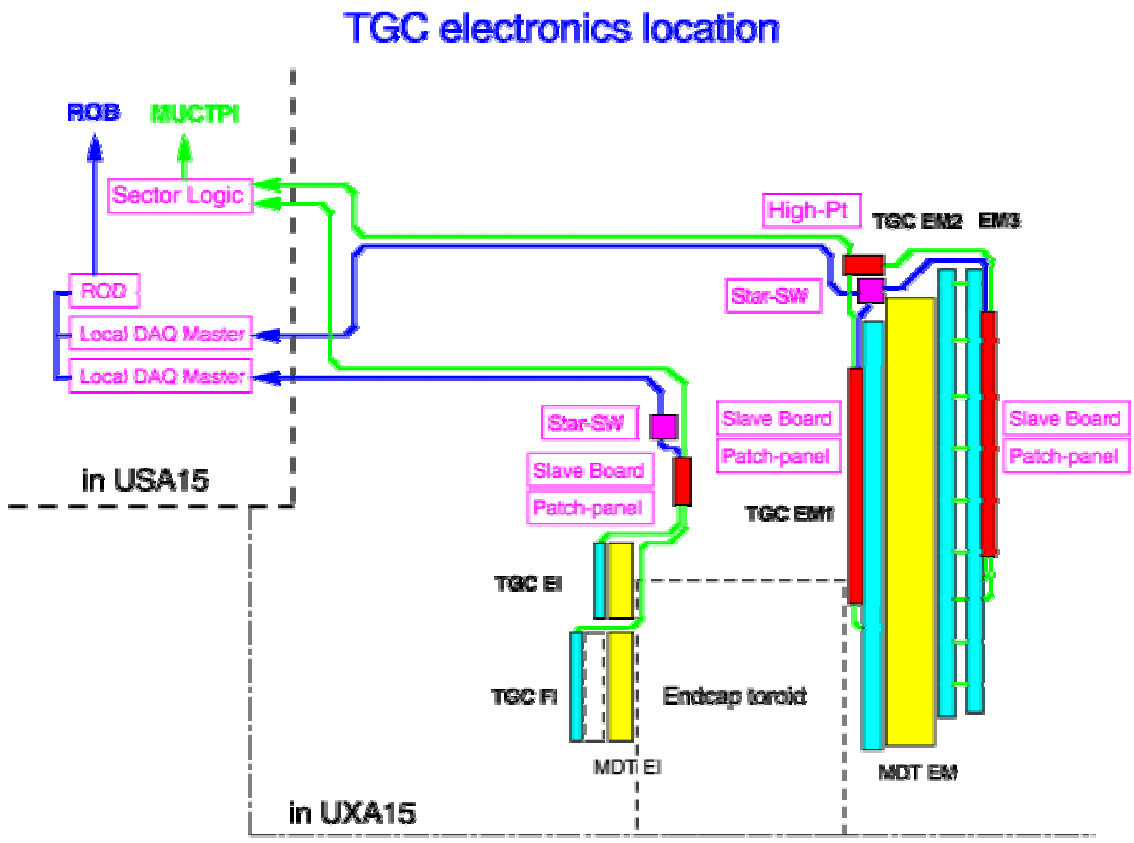

Figure 3-18 TGC electronics location

And the other components of TGC electronics system are Star switch and Read-Out Driver (ROD). Star switch is the data network system optimized for the TGC. It connects several front-end sources (SLBs) to one destination (ROD) with minimum dead time of switching. ROD is a functional element of the front-end system where one can reach a high level of data concentration and multiplexing by gathering information from several front-end data stream. Elementary digitized signals are formatted as raw data prior to be transferred to the ROB (Read-Out Buffer: raw data from ROD is buffered in ROB).

4, TTC (Timing, Trigger, and Control) System

4.1 TTC system overview

The targets of TTC system are synchronization trigger signals with the bunch crossings in the electronics and control the electronics. The overall TTC system architecture provides for the distribution of synchronous timing, Level-1 trigger, and broadcast and individually-addressed control signals, to detector related electronics controllers with an appropriate phase relative to the LHC bunch structure, taking account of the different delays due to particle time-of-flight and signal propagation.

Within each trigger distribution zone, the signals can be broadcast from a single laser source to several hundred destinations over a passive network composed of a hierarchy of optical tree couplers. The optical couplers have small size, low mass and unlimited bandwidth. For control room applications, 1x32 couplers can be mounted in 1U (Height: 1U = 44.4mm) rack trays or plug-in modules. They require no operating power and are potentially highly reliable.

TTC system development is a common project of LHC, SPS, and four LHC experimental groups. The collaboration has built a general purpose timing distribution system. An system designer for a detector electronics, then, must developed an own timing distribution sub-parts using the TTC system to get relevant central-timing signals.

Figure 4-1 shows TTC system overview in an LHC experiment. TTC signals are distributed to each experiment from LHC.

Figure 4-2 shows Bunch Disposition in the LHC, SPC, and PS. It has taken the space of 25ns per bunch.

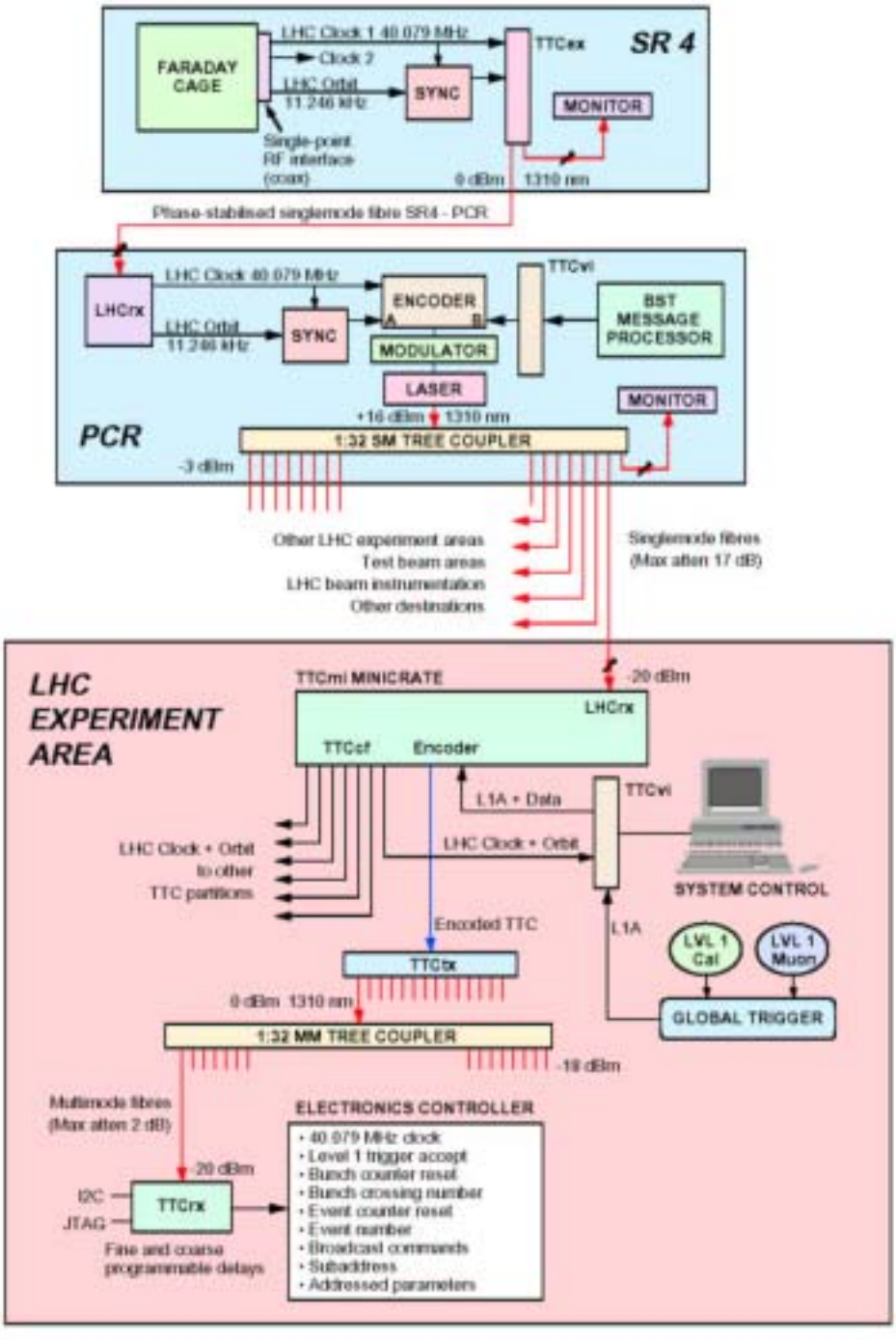

Figure 4-1 TTC system overview

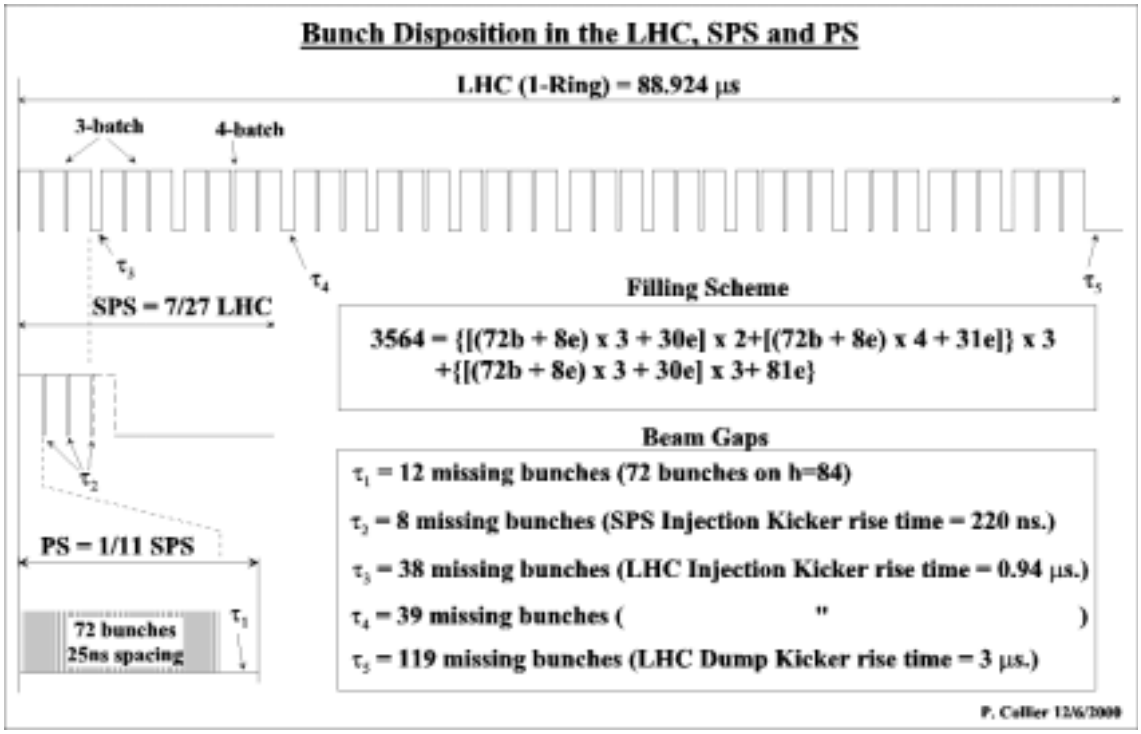

Figure 4-2 Bunch Disposition in the LHC, SPC, and PS

4.2 Interface

TTC system has interfaces to the following devices: LHC machine, CTP (Central trigger Processor), a sub-detector part, which comprises, calibration electronics, and Read-out electronics. These interfaces are described in this section.

4.2.1 The LHC machine

LHC provides a continuously running clock signal (BC[1] clock). As shown in Fig. 4-2, the BC clock structure has a cycle, which lasts 88.924μs. This time is one for 14TeV proton to run around the LHC ring once. The clock is thus generated when a proton pass at a fixed location in a ring. Regularly in one turn, no proton will be passed, and a

[1] Bunch-Crossing.

empty slot (no clock) is formed. Each time one cycle is finished, a signal called ORBIT is asserted. The BCR[2] signal is derived from this ORBIT signal.

Both BCR and ORBIT signals are fanned out electrically to the TTC partitions.

4.2.2 CTP (Central trigger processor)

CTP provides to the TTC system:

- CTP collects all the LVL1 candidate signals from the various LVL1 trigger generation systems, forms a trigger type from LVL1 combination, and transfer the signals to TTC system,
- the L1A (Level-1 Accept) signal which has to be broadcast to all of the readout elements,
- a pre-pulse (PPS) signal that can be issued a predefined number of clock cycles before a test trigger is generated, this signal can be used to initiate the transmission of a test pulse to the front-end electronics at the correct time with respect to the arrival time of the test L1A signal, and
- an 8-bit trigger-type word associated with each L1A signal, this word is transmitted to the readout elements and allows different types of events (e.g. physics events, test events, calibration events) to be distinguished.

All of these signals are electrically fanned out from the CTP crate to the TTC partitions.

4.2.3 Sub-detector part and calibration electronics

The TTC system receives timing (clock and BCID) and trigger (L1Accept, EVID, and Trigger-Type) signals which can be used during commissioning, test and calibration periods from the sub-detector electronics. These signals are transmitted to the front-end and readout electronics as TTC commands.

4.2.4 Read-out electronics

[2] Bunch Counter Reset.

The TTC system provides to the readout electronics the following signals or data;

- BC (Bunch Crossing) clock signal,
- L1A (Level-1 Accept) signal,
- BCR (Bunch Counter Reset) and ECR (Event Counter Reset) signals,
- BCID (Bunch Crossing ID) and EVID (Event ID) words with each L1A signal,
- Trigger-type word with each L1A signal, and
- Commands and Data, including test and calibration pulses.

The phase of the BC clock is adjustable in steps of 100ps within 25ns. L1A, BCR and commands can in addition be delayed by up to 15 BC clock cycles.

4.3 Details of TTC system

The ATLAS read-out elements, such as the front-end electronics, the read-out drivers (ROD) and possibly the read-out buffers (ROB), need the BC clocks and the L1A signals. Each read-out element has to produce an EVID and a BCID with each event. It is therefore necessary to make available some synchronization signals, in order to maintain coherence between these IDs across the experiment. These synchronization signals are BCR and ECR. During test and calibration periods, the read-out electronics also need to receive test and calibration signals.

TTC system allows the timing and trigger signals to be distributed to the read-out electronics. The timing signals comprise the LHC clock (BC clock) and the synchronization signals (BCR, ECR). The trigger signals include the L1A, test and calibration triggers. The TTC allows the timing of these signals to be adjusted.

4.3.1 Backbone components

TTC backbone components are:

- TTC crate and fiber network

- TTC VME[3] interface (TTCvi)
- TTC receiver chip (TTCrx)

TTC crate receives electrical signals from the TTCvi and the LHC machine, and performs the encoding and the electrical-to-optical conversion. An optical tree network with optical passive fan-outs distributes the encoded optical signals to up to 1024 destination nodes. These nodes consist of an optical-to-electrical conversion device followed by a receiver ASIC[4] (TTCrx) which decodes the incoming frame and makes available all of the timing, trigger and control signals.

TTCvi is a VME module which provides the trigger and control signals to the TTC crate in the form of two encoded signals (A-channel and B-channel). This module allows a user to select the trigger source and to generate commands at known times. A TTC partition consists of a TTCvi, a TTC crate, an optical network and as many receivers (TTCrxes) as necessary. An example is shown in Fig. 4-3.

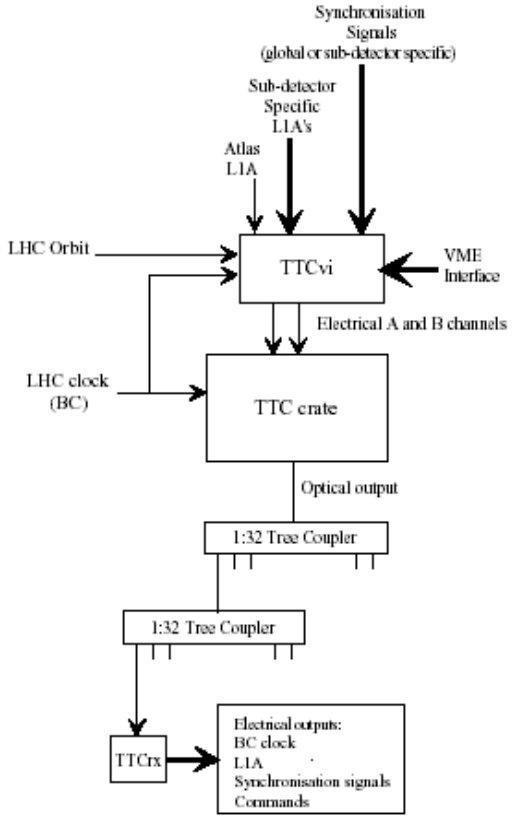

Figure 4-3 TTC partition

[3] Versa Module Europe. VME bus is IEEE 1014 standard, and Versa bus is standardized for 68k CPU by Motorola.
[4] Application Specific Integrated Circuit.

4.3.1.1 TTC crate

TTC crate receives two electrical signals from TTCvi and performs the final encoding and the electrical-to-optical conversion.

4.3.1.2 TTCvi (TTC VME Interface)

TTCvi[5] is developed by RD12[6] collaboration of LHC at CERN. TTCvi delivers the A-channel and B-channel signals to the TTC crate. These two signals carry timing, trigger and control information. TTC A-channel is used only to transmit L1A signal. TTC B-channel is used to transmit framed and formatted commands and data. These can be either.

Short-format synchronous or asynchronous broadcast command/data cycles

If synchronous, the timing of these cycles relative to the LHC orbit is controlled precisely. Such cycles are used for the broadcasting of the BCR signal and for the transmission of other fast synchronous broadcast controls and test commands. These can be decoded at the receiving end (after the TTCrx) and used to produce test pulses, calibration pulses, etc.

Long-format asynchronous individually-addressed or broadcast command/data cycles

The timing of these cycles with respect to the LHC orbit is indeterminate and they are not individually adjustable in the TTCrx ASICs. They are used for the transmission of parameters and non-time-critical commands. For instance, they are used to transmit the trigger type after each L1A signal.

TTCvi is the master of a TTC partition. It is fully controlled through a VME interface by the partition user. It is at this level that the user decides to include this partition in the global ATLAS readout system or to run the partition in independent test or calibration runs. In this last case the partition uses sub-detector-specific timing and trigger signals. When the partition is in the global ATLAS readout system the TTCvi is controlled by the DAQ run control. A simplified block diagram of this module is given in Fig. 4-4.

[5] Ref. “TTC-VME bus interface (TTCvi) Manual,” http://www.cern.ch/TTC/TTCviSpec.pdf
[6] One of the LHC Common project. Ref. http://ttc.web.cern.ch/TTC/intro.html.

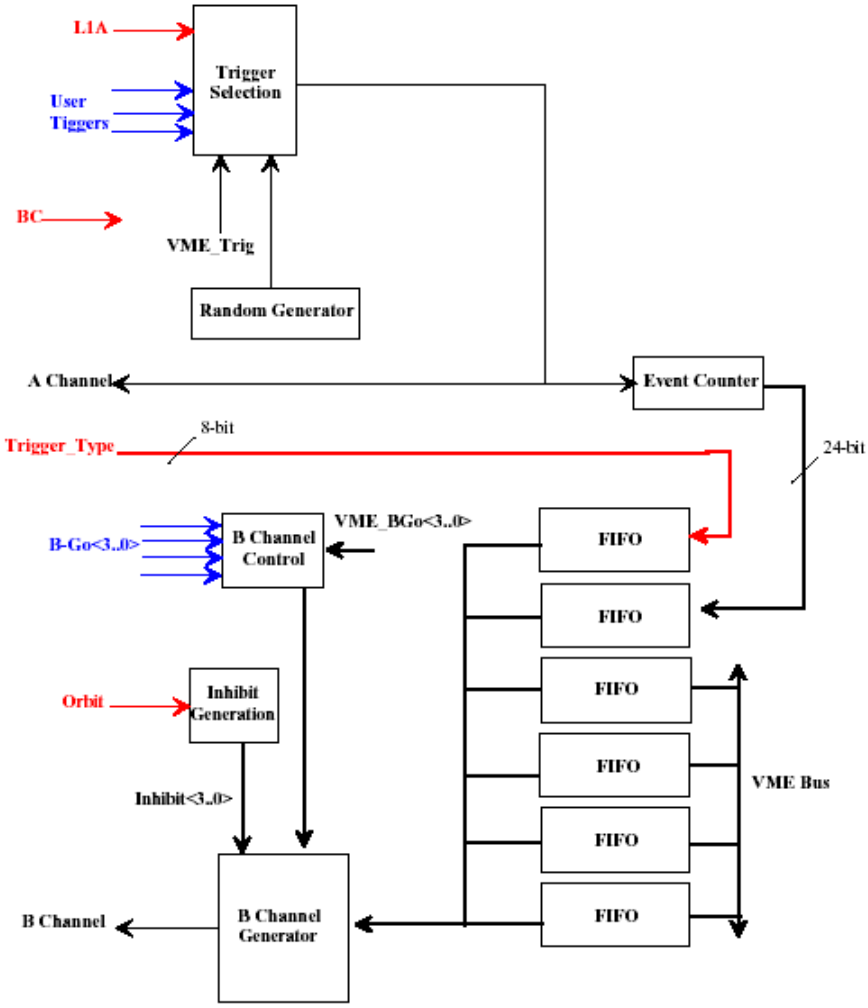

Figure 4-4 TTCvi simplified block diagram

4.3.1.3 TTCrx (TTC receiver chip)

TTCrx[7] is a custom ASIC that receives control and synchronization information from the central TTC system (after optical-to-electrical conversion) and makes it available to the readout electronics. TTCrx can be programmed to compensate for particle times of flight and for propagation delays associated with the detectors and their electronics.

One of the main functions of TTCrx is to recover and distribute the 40.08 MHz BC clock with minimal jitter. It also makes available to the readout electronics L1A signal and its associated BCID and EVID numbers. Each TTCrx IC is identified in the distribution network by a unique 14bits ID number. The ASIC control logic identifies the A- and B-channels, deserializes the data in the B-channel and continuously monitors it to

[7] Ref. “Timing receiver ASIC (TTCrx) Reference Manual,” http://www.cern.ch/TTC/TTCrx_manual3.4.pdf

look for the presence of its ID number. TTCrx diagram is given in Fig. 4-5.

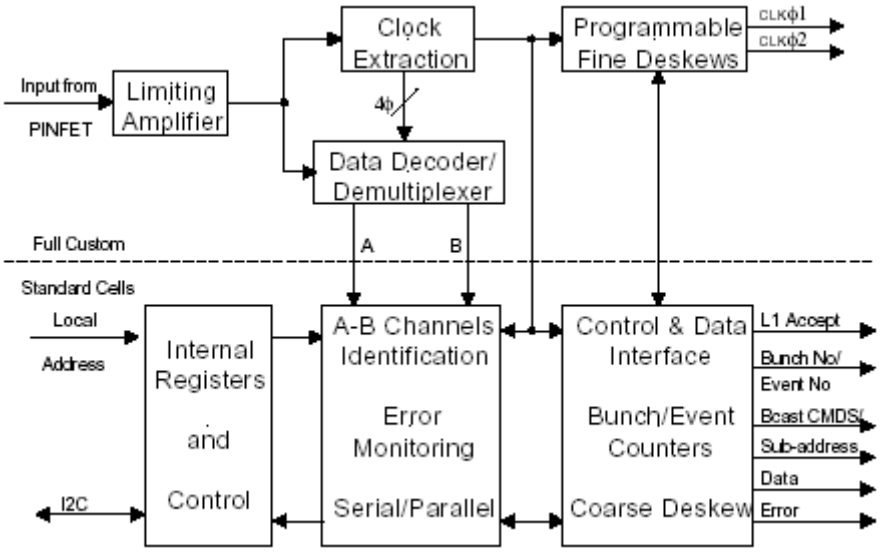

Figure 4-5 TTCrx diagram

4.3.1.4 TTCvx (TTC VME-size LED transmitter module)

A VME-size module, TTCvx[8], is developed by RD12 collaboration of LHC at CERN. TTCvx is foreseen to be an alternative of TTC crate and is used in TTC test and evaluation systems, where a compact and economical solution is desired.

In details, TTCvx module function is to multiplex and encode the A and B channels generated by the TTCvi. TTCvx has an internal clock, as well as an input for an external one. The switching between the two clock sources is automatic by the means of an external clock detection circuit. The, for the encoding, necessary clock multiplication is handled by a phase locked loop (PLL) frequency synthesizer circuit. The basic clock frequency from PLL is available on the module front panel in both LVDS and ECL levels and is used for synchronization with TTCvi. Up to four light emitting devices can be fitted to drive fiber optic cables. The encoded signal is also available on the front panel in both ECL and LVDS levels. TTCvx diagram is given in Fig. 4-6.

[8] Ref. "TTCvx Technical Description and Users Manual," http://www.cern.ch/TTC/TTCvxManual1a.pdf

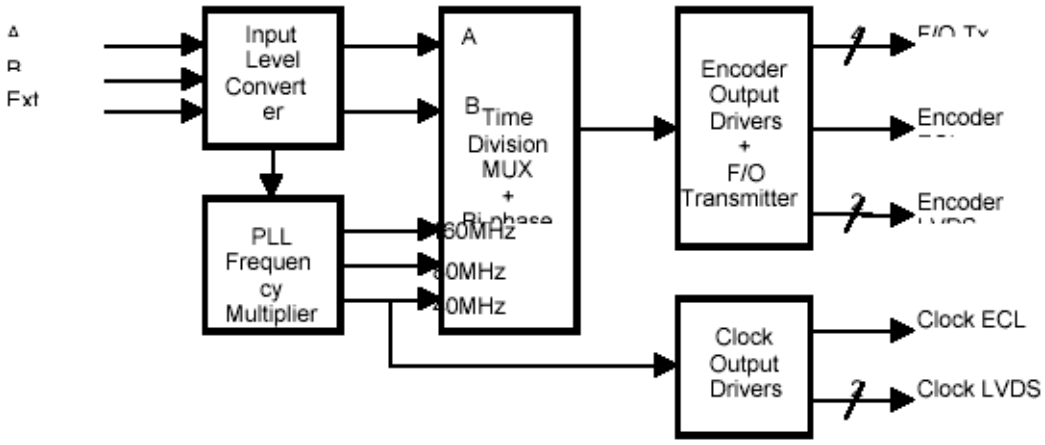

Figure 4-6 TTCvx diagram

4.3.2 Partitioning

A TTC partition consists of a TTCvi, a TTC crate, an optical network and as many TTCrx chips as necessary (up to 1024). Any signal, data or commands transmitted on a particular partition reach only the TTCrx chips belonging to that partition.
Partitioning the TTC system allows different sub-detectors to work concurrently in the following instances;

- during test or calibration periods with independent timing and trigger signals, and
- during the setting up of a physics run when the TTC network may be used to download parameters in the front-end and readout electronics.

Not only is it necessary to have independent partitions per sub-detector, but also to have further sub-partitions within each sub-detector. This is for the following reasons:

- During assembly and commissioning, a sub-detector is divided into independent parts,
- One could wish to run different parts of a sub-detector in different modes (e.g. test mode and calibration mode), and
- The fiber length from the TTC crate to the readout electronics may vary a lot from one part of the detector to the other and hence the delay compensation foreseen in

the TTCrx chip may not be sufficient.

4.3.3 Functionality

This section describes how the TTC system will be used, what functionality is available and how it is controlled.

4.3.3.1 Initialization

At the start of a run or a test or calibration period, one has to:

- define whether a particular TTC partition is to run independently or is to be part of the global ATLAS data-taking,
- select the signals to be used accordingly (clock, trigger source, etc.),
- configure necessary parameters in the TTCvi driving the TTC partition, and
- set all the programmable delays in the TTCrx chips.

The first three operations are done through the VME interface of TTCvi, while the fourth one can be done either through the TTC network or through the I^2C interface of the TTCrx chips. The TTCrx registers are loaded according to using asynchronous individually-addressed commands.

The initialization is performed within the framework of the DAQ/run-control system, as, from the DAQ viewpoint, there is a direct correlation between a TTC partition and a DAQ partition.

4.3.3.2 Synchronization

With regard to synchronization, one has to consider the following sentences.

Synchronization with respect to the LHC cycle

The LHC cycle is shown in Fig. 4-2. The LHC machine provides a synchronization signal (ORBIT) which exhibits a transition edge at a known time in the cycle. This signal is used by the TTCvi to build up to four internal synchronization signals (INHIBIT). These signals allow the generation of commands (including BCR) at known times within the LHC cycle.

Maintenance of a consistent BCID across the complete experiment

All the necessary tools to maintain a coherent BCID across the experiment are available. In the TTCvi, one of the INHIBIT signals is devoted to BCR command. The phase of this command with respect to the LHC cycle is properly adjusted in the TTCvi.

Maintenance of a consistent EVID across the complete experiment

ECR signal is necessary to reset the local event number counters if necessary (e.g. if a desynchronization has been detected). The system must guarantee that there is no L1A signal during the time this signal is broadcast to all the TTCrx's. This can be easily achieved by introducing dead-time at the CTP level.

4.3.3.3 Test and calibration signals transmission

During test and calibration periods, one has to be able to send pulses and triggers to the readout electronics. TTCvi allows this to be done in different ways, without requiring any hardware intervention. In addition to the ATLAS L1A signal coming from the CTP, three other trigger inputs are available. The test signals can be transmitted as synchronous commands on the TTC system and any one of the available B-Go[9] signals can be used (in this case the relative phase between the test pulse and the trigger is to be adjusted externally), or sequences of commands with timing defined by the internal INHIBIT signals can be used. In this latter case the user has to decode TTCrx command outputs to locally generate test and trigger signals. The INHIBIT signals are available as NIM[10] signals on the TTCvi front panel and can be used to fire external logic if needed. The command output of the TTCrx can be resynchronized with one of the two adjust-

[9] One of the B-channel data control signals.
[10] Nuclear Instrument Module.

able clocks available. This allows the readout electronics to have, for instance, a test signal with an adjustable timing with respect to the clock.

4.3.3.4 Trigger type transmission

It is necessary to have, with each L1A signal, some information on the type of the trigger (for example, calibration, physics). This information may be used in the RODs. TTCvi receives an 8bits trigger-type word from CTP and transmits it to the TTCrx. This transmission cannot be in phase with L1A signal, as there is not enough bandwidth available to transmit this word within five BC (the BC of the L1A followed by the four dead-time BCs). The trigger type is transmitted in an asynchronous way when the TTC system is available (i.e, when there is no transmission of synchronous commands such as BCR). The trigger type is available at the output of the TTCrx about 2us after the L1A signal has been issued, assuming there were no L1A signals in the previous 2us. If consecutive L1A signals occur within a short period of time, the trigger type transmission is queued and the trigger type of a given L1A signal will become available later at the output of the TTCrx. This is considered not to be a problem as the trigger type is used only at the ROD level where the event data are subject to similar fluctuations in arrival time.

4.3.4 Latency

The TTC system introduces latency (delays) on the L1A signal at different places:

- the L1A signal has to be fanned out and transported from CTP to TTCvi,
- the L1A signal has to be transformed in the TTCvi to provide the A-channel signal to TTC crate,
- the signal has to be transmitted from TTCvi to TTC crate and, in TTC crate, it has to be encoded and converted from electrical to optical,
- the light signal has to travel through the optical network, and
- at the receiving end, there is an optical-to-electrical conversion and TTCrx has to decode the incoming frame and make available the L1A signal.

The part of the latency due to the optical network depends on the fiber lengths. This corresponds to the maximum distance between any on-detector front-end electronics element and the furthest crate in the underground control room (USA[11]15). The final latency will have to be computed for each sub-system when the physical locations of the different elements are known. It should also include the latency introduced by a change of protocol on the line.

4.3.5 Test and Monitoring

There is a need for a global timing adjustment of the experiment which has to be done regularly and at least before each run. This timing adjustment sequence is a very good test of the TTC network itself as it requires the transmission to be fully efficient and all the timing characteristics of the delivered signals to be good. The monitoring of the system is done in the following ways:

- The information carried by the TTC is part of the event readout data (BCID number, EVID number, trigger-type word) and this information is checked at every stage of the readout chain. This allows the basic transmission on the TTC network to be monitored.
- The TTC system includes an error detection mechanism and each TTCrx maintains an error register. These registers will be read out regularly.
- The timing characteristics of the delivered signals (jitter on the BC clock, delay stability, etc.) will require a fine analysis of the readout data.

The test of the TTC system is done via VME for the TTCvi and via the I^2C interface for the TTCrx.

[11] Underground Service Area.

4.4 Adaptation of TTC for the ATLAS TGC Level-1 electronics system

Particular signals actually used among various kinds of TTC signals are differed with different sub detector system. This chapter describes the signals actually used in TGC Level-1 electronics system concretely.

In TGC, TTC system is used with three partitions. Then, in this section, it is discussed extensively how the TTC signal is passed to a Read-out electronics system with the setup of TTC system.

4.4.1 TTC system setup for the development of TGC electronics system

We use the following setup in order to adapt the TTC system into the TGC electronics as shown in Fig.4-7,8.

Figure 4-7 TTC system setup photo for the development of TGC electronics

In Fig. 4-7, from the right to left, TTCrx Fan-out board, TTCvx, and TTCvi are installed in a VME crate. The schematic diagram of the connection of the modules is shown in Fig. 4-8.

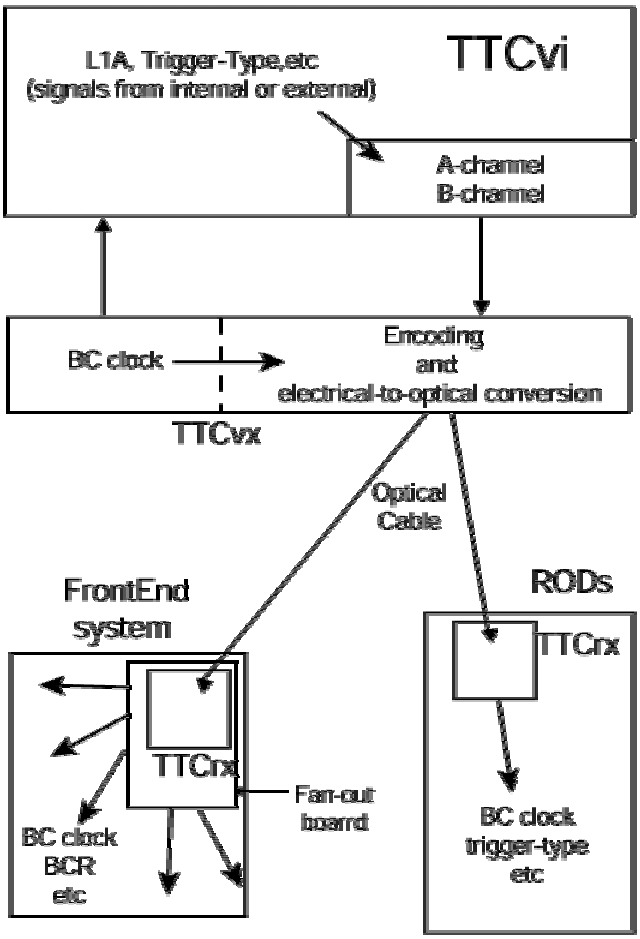

Figure 4-8 TTC system setup diagram for the development of TGC electronics

TTCvi packs signals, such as L1A and trigger-type, into A-channel and B-channel and sends them to TTCvx. We can choose whether to generate L1A within TTCvi, or to input into TTCvi from the external electronics module. In TTCvx, after encoding the signals sent from TTCvi, these signal are converted from electrical to optical, and they are sent to TTCrx. In TTCrx, these sent signals are decoded, and fan-out board distributes these decoded signals. The front-end modules in each partition will operate by taking in required signals from this fan-out board.

In the next section, how TTC signals are delivered to front-end modules from TTCrx and what fan-out module is used for TTCrx are discussed.

4.4.2 Used TTC signals and Partition

In TGC electronics, we use TTCrx test board for decoding signals from TTCvx to TTC signals. Figure 4-9 shows the overview of TTCrx test board. Encoded TTC signal is come from optical connector with optical fiber, this signal is decoded in center TTCrx chip, and the right and left 50-pin put these decoded signals.

Figure 4-9 TTCrx test board

The TTCrx test board[12] is developed by CERN Microelectronics group[13].

TTC signals are distributed to front-end electronics system by using this TTCrx test board as a mezzanine card on a fan-out board. Reasons why the TTCrx test board is used instead of the TTCrx chip itself are i) easiness to extract TTCrx signals from the test board rather than the pins of the chip, and ii) easiness to construct the TGC electronics because the board is easy to be adopted as mezzanine card.

4.4.2.1 SPP (Service Patch Panel board)

SPP is one of the TTCrx fan-out board, and SPP deliver TTC signals from TTCrx to PP and SLB board. SPP board photo is given in Fig. 4-10.

[12] Ref. “Timing receiver ASIC (TTCrx) Reference Manual,” http://www.cern.ch/TTC/TTCrx_manual3.4.pdf
[13] http://www.cern.ch/CERN/Divisions/ECP/MIC/WelcomeMIC.html

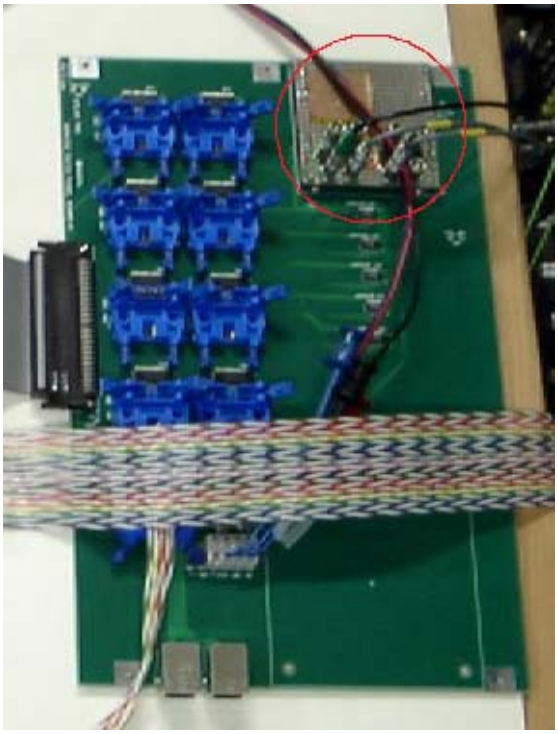

Figure 4-10 SPP board

Although a dummy board is mounted (for debugging SPP) on the SPP board in Fig. 4-10, originally a TTCrx test board should be mounted on SPP in this circle.

SPP is specially developed to be used on TGC End-cap muon detector. SPP board becomes the portion which connects TTC system and Front-end electronics, and supplies TTC signals to PS board (PP and SLB board) and HSC from TTCrx. SPP is developed wiring the signal line by equal length, in order to distribute all signals to the same timing. The TTC signals are distributed to eighteen (max.) by this SPP are as follows;

- BC clock (adjustable clock),
- L1A,
- BCR,
- ECR, and
- Test Pulse trigger.

Test Pulse trigger signal is distributed as Broadcast command signal.

4.4.2.2 LVDS Fan-out Board (for Sector Logic)

LVDS Fan-out board is one of the TTCrx fan-out board, as previously described SPP.

Figure 4-11 LVDS Fan-out board

Figure 4-11 shows TTC LVDS Fan-out board. This board is made based on VME standard. Although it was thought that this board is also used as SPP at first, there are some problems, such as the number of distributions of TTC signal, after that, and now we consider using this board for Sector Logic. The TTC signals distributed on this board are as follows, and Sector Logic uses three signals, BC clock, BCR and ECR, in these signals;

- BC clock (two adjustable clocks),
- L1A,
- BCR,
- ECR,
- Test Pulse trigger,
- TGC Reset, and
- DCS Reset.

This fan-out board is also developed wiring the signal line by equal length, in order to distribute all signals to the same timing. It is difficult to distribute a signal in order to have to arrange equal level voltage. Since the voltage of the TTCrx signal was set high (5V) at first, there is a difference of the voltage of distribution IC and LVDStx IC, and duty of BC clock has been out of order. However, since the voltage of the TTCrx signal falls into 3.3V and the voltage of two ICs become same value, this problem is solved.

Test Pulse trigger, TGC Reset, and DCS Reset are distributed as Broadcast command signal.

4.4.2.3 TTCrx on ROD (Read-Out Driver)

Figure 4-12 shows the overview of ROD board, and Fig.4-13 shows mounted TTCrx photo on ROD board. In ROD, in order to collect TGC readout data, more TTC signals are needed than the trigger system. The signals used are as follows;

Figure 4-12 ROD board

Figure 4-13 TTCrx on ROD board

- BC clock (adjustable clock),
- L1A,
- BCID (12bits),
- EVID (24bits),
- Trigger-type (8bits),
- BCR,
- ECR,
- Test Pulse trigger,

- TGC Reset, and
- DCS Reset.

However, you see so far and know, and many modules of TTC system are required for development of the read-out electronics system, and in order to control these modules, you also have to write control software. What should TTC signals be made for using more easily? This answer is described in the following section.

4.5 TTC Emulator for ATLAS TGC Electronics

4.5.1 Overview

Why we have developed TTC Emulator? Because there are two main reasons:

Easy handling

For using TTC Signals, we have to use some modules (i.e. TTCvi, TTCvx, TTCrx, etc) and make some programs for their modules. By developing the TTC Emulator, the fundamental function of TTC system can be obtained easily with only one board, without making any program and setting up the whole system. This board is designed by the completely same pin assignment and size so that TTCrx can be replaced.

Cost reduction

Since the total cost of TTC system is high, to use the whole TTC system for the development of read-out electronics is inefficient. We cannot purchase a lot of sets freely. In order to reduce this cost, we make the TTC Emulator with limiting the function to generate only required TTC signals for TGC electronics.

The TTC Emulator presently constructed fulfils above two purposes. But, in the future, the other signals will be required in the TGC electronics development, or there may be change of TTC or LHC signal specification. Since this TTC Emulator is con-

structed on FPGA, dealing with specification change is possible. Specifically, the following measures are taken:

- In addition to configuration that uses PROM, configuration that uses JTAG is prepared.
- Since all the pins (except VCC) currently used by TTCrx are connected to FPGA, it can respond to change of specification or the addition of signals flexibly without circuit redesign.

Flexible correspondence is possible for TTC emulator.

Figure 4-14 TTC Emulator board

Figure 4-14 shows the overview of TTC Emulator board.

Then, it is described which functions and signals are emulated on the TTC Emulator in the following chapter.

4.5.2 Emulated signals and functions

TTC Emulator implements functionalities of generation of signals which are normally produced in the chain of TTCvi, TTCvx, and TTCrx. Therefore, a test system environment of read-out modules using TTC system can be simplified dramatically. TTC Emulator is compatible (size and footprint) with TTCrx test board (see Fig. 4-9 and 4-14). TTC Emulator block diagram is given in Fig. 4-15.

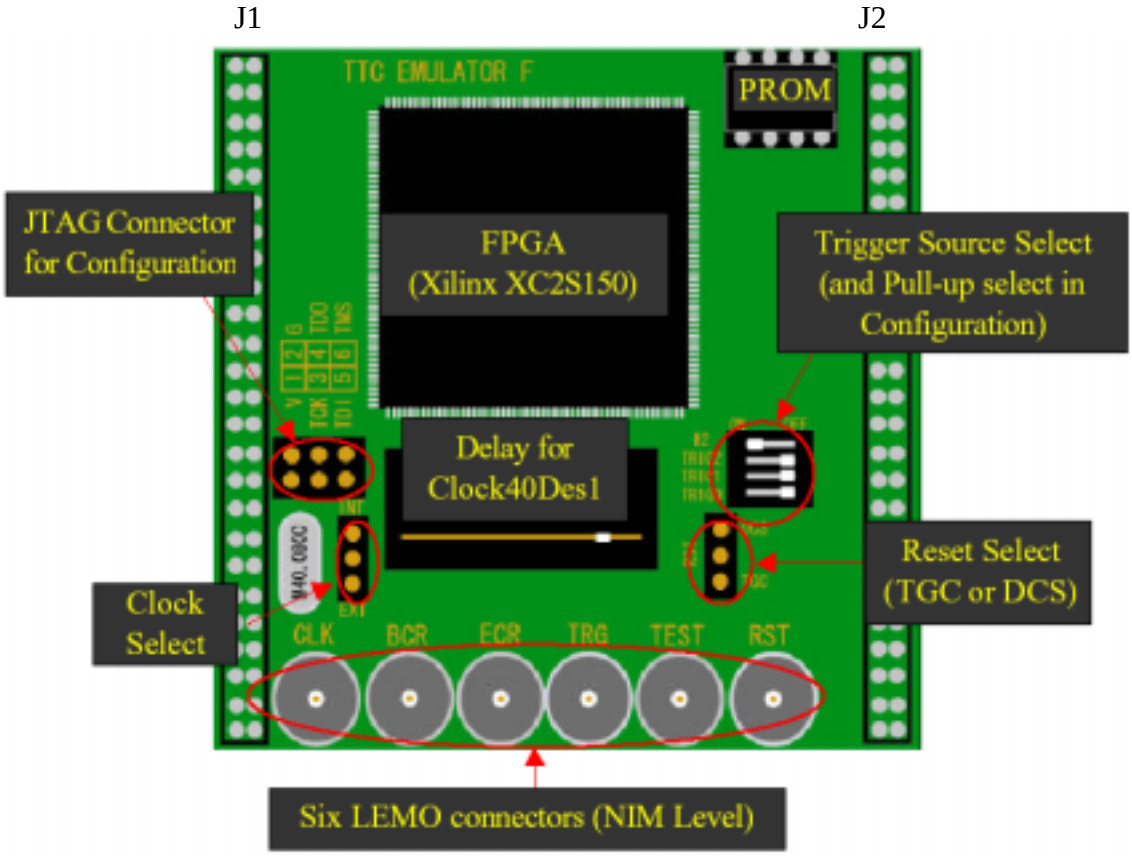

Figure 4-15 TTC Emulator block diagram

Emulated TTC signals are described in table 4-1. In table 4-1, J1 is 50-pin located on left and J2 is 50-pin located on right in Fig. 4-15.
TTC Emulator is pin compatible with TTCrx test board.

J1	Contents
Clock40Des1	Clock signals. This signal can be delayed by using Elmec VDS2120
Brcst<5>	Reset signal for DCS.
BrcstStr1	Strobe signal. This signal outputted with Brcst<5>.
SubAddr<1:0>	In case TriggerType<7:0> and EVID<23:0> are divided and taken out to 4 steps, these signals indicate what signal pattern are outputted.
SubAddr<7:2>	0(Low)
DQ<3:0>	0(Low)
DoutStr	Strobe signal. This signal outputted with Dout<7:0>.
Dout<7:0>	It is used in case TriggerType<7:0> and EVID<23:0> are outputted in 4 steps.
Reset_b	Whole reset. There is an effect equivalent to the case where BCR and ECR are inputted simultaneously.
TTCready	1(High) except when Reset_b is 1(High).
J2	Contents
BrcstStr2	Strobe signal. This signal outputted with Brcst<7:6>.
Brcst<6>	Test pulse trigger signal for TGC.
Brcst<7>	Reset signal for TGC.
EvCntRes	Event Counter Reset. EVID is reset at High. Being set to High is restricted when ECR signal is inputted from Lemo and when EVID fills (all 24bits are 1).
L1Accept	Level 1 Accept Trigger. It is outputted when trigger is generated inside and trigger is inputted from Lemo.
EvCntLStr	Strobe signal. This signal outputted with BCnt<11:0> as EVID<11:0>.
EvCntHStr	Strobe signal. This signal outputted with BCnt<11:0> as EVID<23:12>.
BcntRes	Bunch Counter Reset. BCID is reset at High. Being set to High is restricted when BCR signal is inputted from Lemo and when BCID is3563.
BCnt<11:0>	It is used in case BCID<11:0> and EVID<23:0> are outputted in 3 steps.
BCntStr	Strobe signal. This signal outputted with BCnt<11:0>.
TTCrx_VDD	3.3V Power Supply

Table 4-1 Emulated TTC signals

TTC emulator can make TTC signals from only this board. For this reason, by this emulator, the L1A signal had to be generated inside FPGA. In order to bring close to an actual experiment state, the random trigger generation function was incorporated.
Thanks to the random trigger generation (originally this function is included in TTCvi), TTC Emulator can give us a realistic experimental environment for TGC electronics system. This random trigger generation function can choose the average frequency of a trigger, and is as follows:

- Internal random rate (Poisson Random distribution) (100kHz, 10kHz, 1kHz, 100Hz, 1Hz)
- Internal regular rate (75kHz, 1Hz)
- External input trigger

As mentioned above, quite realistic TTC signals can be taken out with only one board. However, for example, when you want the BC clock of quicker frequency, signals with the more sufficient convenience to the development of electronics cannot be made. Therefore, it is possible to input some important signals from the outside. There are six Lemo connectors prepared for input signals.

Then some emulated TTC signals are actually seen, and analyzed in the next section.

4.5.3 Test results

- L1A signal

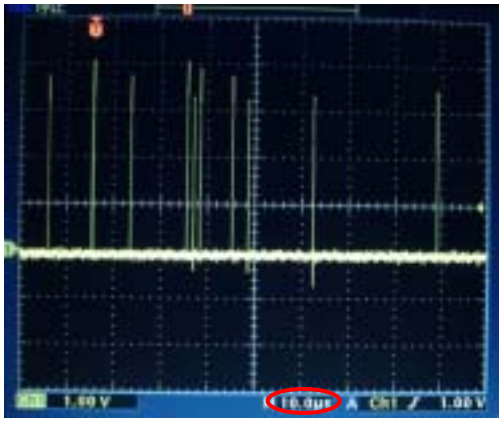

Figure 4-16 100kHz random-rate trigger

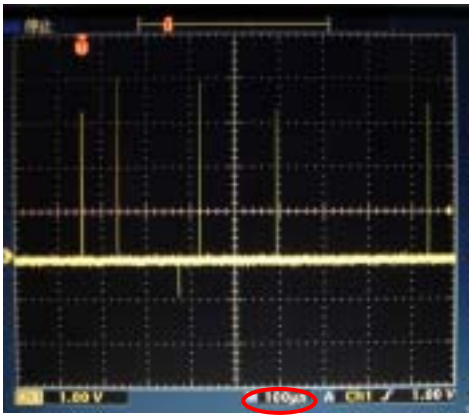

Figure 4-17 10kHz random-rate trigger

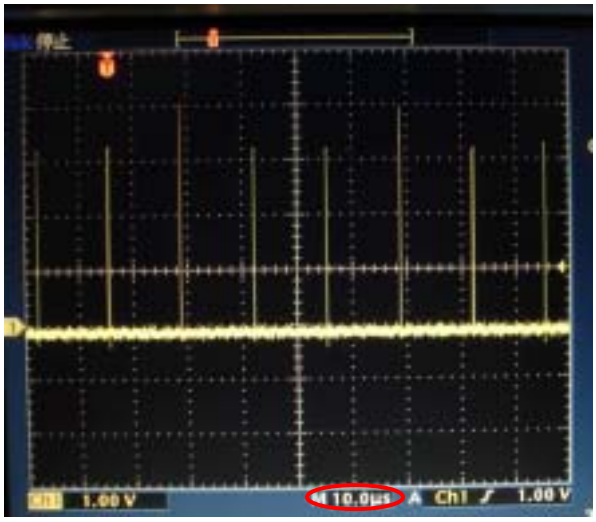

Figure 4-18 75kHz regular-rate trigger

Figure 4-16, 17,18 are actual emulated L1A signals. Trigger frequencies are random-100kHz, random-10kHz, and regular-75kHz, respectively. The scale of this oscilloscope shows that the L1A signals are generated correctly.

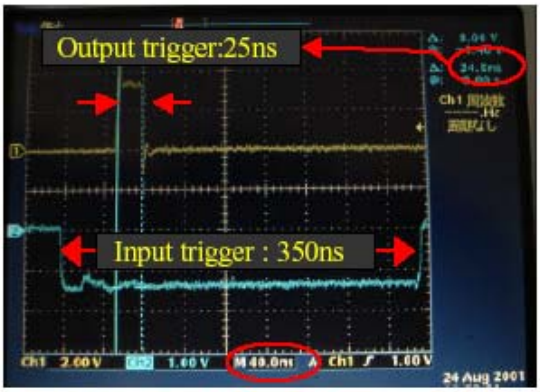

Figure 4-19 input trigger and output trigger

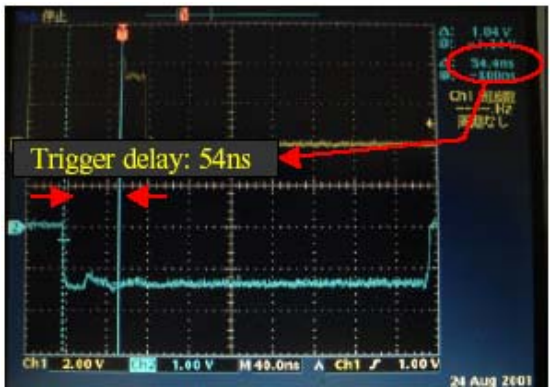

Figure 4-20 trigger delay

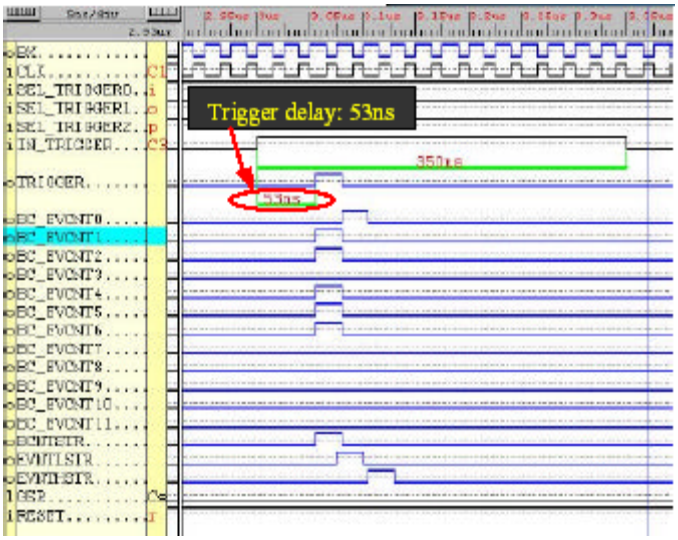

Figure 4-21 software simulation

Figure 4-19 shows if input trigger is longer than 1 BC clock, output trigger is modified. Figure 4-20 shows internal delay in FPGA from input trigger to output trigger. This delay timing can be simulated because of software simulator is prepared. This result is given in Fig. 4-21. If these two results are compared, FPGA is correctly programmed about L1A signal.

- L1A trigger information signal

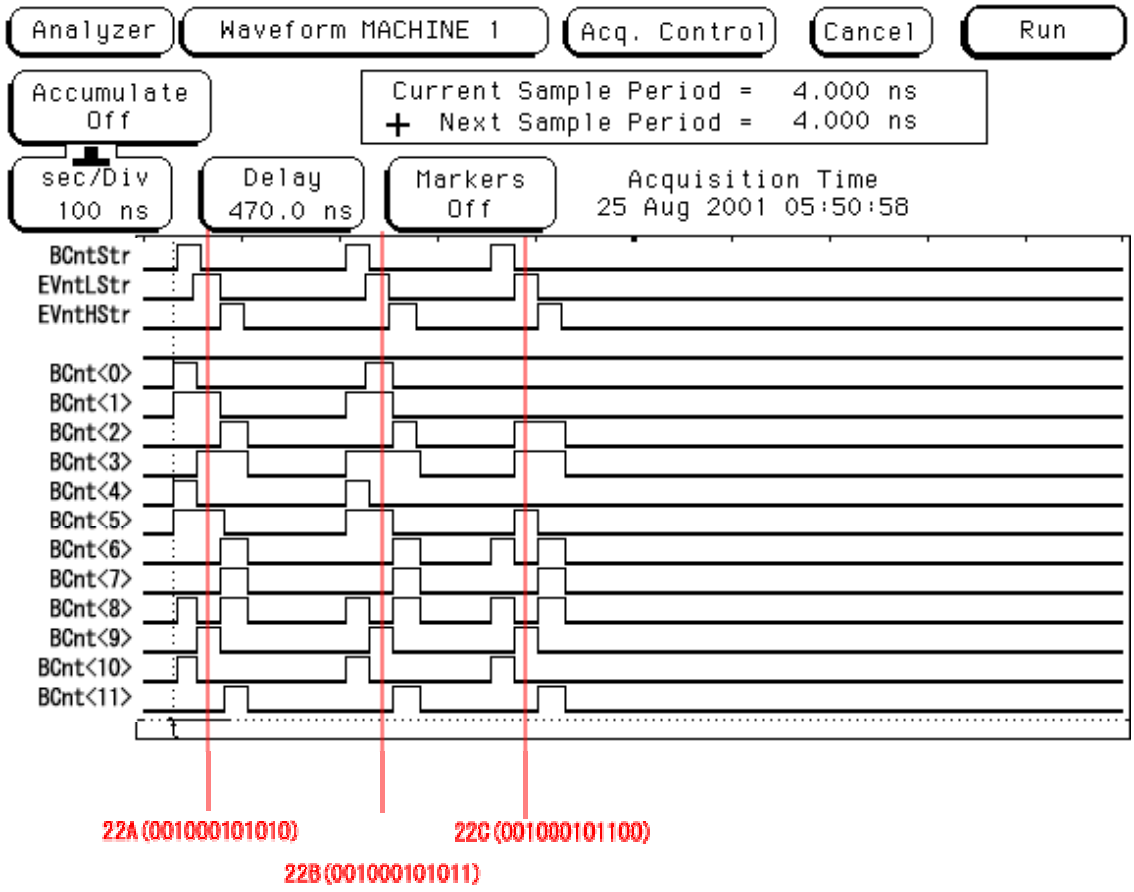

Figure 4-22 BCID and EVID

TTC Emulator can make L1A trigger information signals:

- BCID
- EVID
- Trigger-type

Figure 4-22 shows BCnt bus line (include BCID and EVID):

- BCID<11:0> (12-bit BCID) outputted with BCntStr
- EVID<11:0> (Lower bits in 24-bit EVID) outputted with EvntLStr
- EVID<23:12> (Higher bits in 24-bit EVID) outputted with EvntHStr

This figure shows EVID is increasing in number for every trigger correctly.

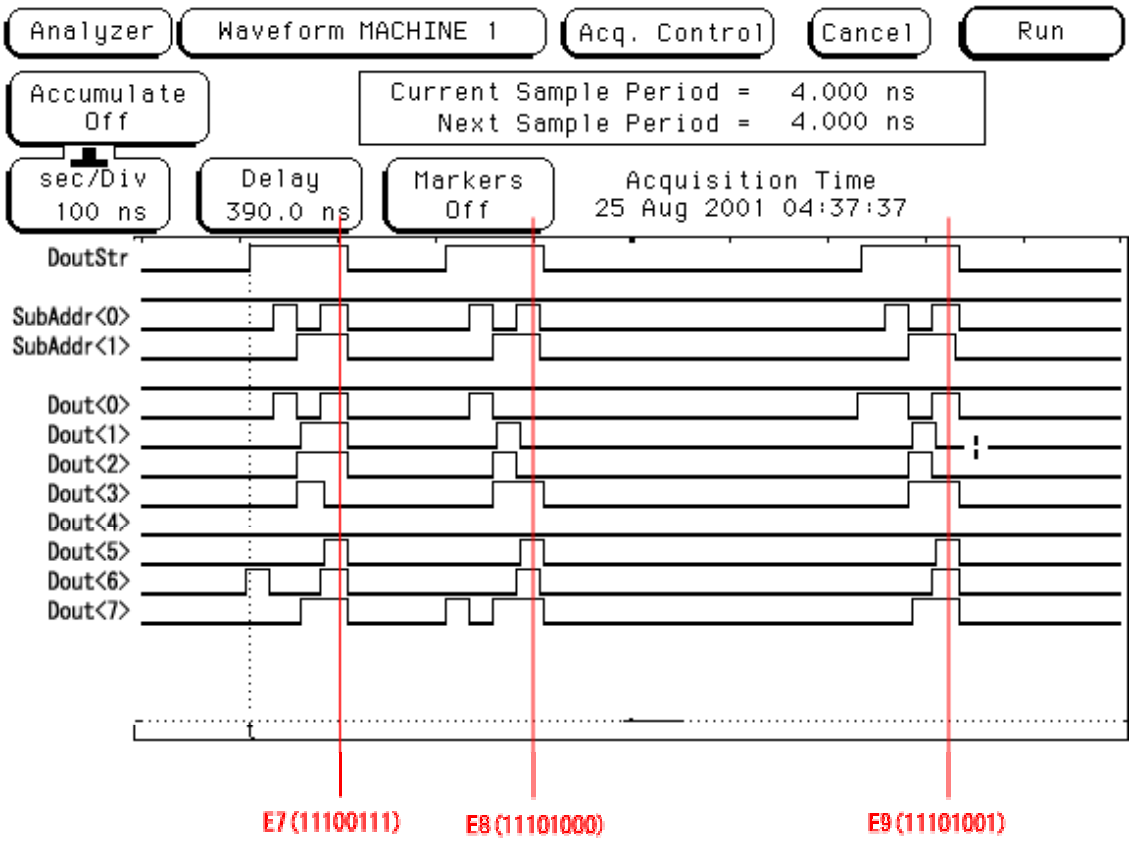

Figure 4-23 Trigger-type and EVID

Figure 4-23 shows Dout bus line (include Trigger-type and EVID):

- Trigger Type<7:0> (8-bit Trigger-type) outputted with DoutStr and SA1(0)SA0(0)
- EVID<23:16> (Highest bits in 24-bit EVID) outputted with DoutStr and SA1(0)SA0(1)
- EVID<15:8> (middle bits in 24-bit EVID) outputted with DoutStr and SA1(1)SA0(0)
- EVID<7:0> (Lowest bits in 24-bit EVID) outputted with DoutStr and SA1(1)SA0(1)

(SubAddr<1:0> = SA1(*)SA0(*); Lowest 2 Sub Address bits)

This figure shows EVID is increasing in number for every trigger correctly.

Moreover, in addition to these results, signals, such as BC clock, BCR, and ECR, are also outputted correctly. Furthermore, BC clock has checked that deskewing BC clock over one BC clock was also possible by using delay line. Thus, We already have checked TTC Emulator taking out the TTC signal exactly and TTC Emulator has played a substitute of the TTC system sufficiently. Probably, it will be important to introduce so that TTC Emulator may actually be used in TGC electronics and can profit the development of TGC electronics.

5, Radiation Tolerance

5.1 Introduction

In ATLAS, as described even in Chapter 3, many particles pass through the detector. There are leptons like muon, hadrons like neutron. These particles contain the radiation activity, and make many by-products, such as γ-ray and electrons, simultaneously. Owing to this radiation effect, many electronics currently being attached to the ATLAS detector may carry out incorrect operations, or the electronics themselves will be destroyed. These phenomena are called radiation damage and in order to check how our electronics will be tolerant for long time radiation in the actual ATLAS experiment, radiation tolerant check for our electronics parts is needed.

ATLAS has agreed a Quality Assurance plan[1] dedicated to the radiation tolerance of its electronics components, of which the aims are summarized in two items followingly.

1. The effects of radiation on electronics should have no consequences on the safety of the persons and of the global experiment. In other words, they should not induce any risks for the people working on irradiated electronics, and no fire risks.

2. The electronic systems should be built in such a way that they remain in conformity with their specifications during 10 years of operation in their specific radiation environment. This can be obtained either by designing radiation tolerant systems, or by designing less robust systems but foreseeing their replacement after a certain period of time.

In this chapter, our two experiment results, the γ-ray irradiation experiment made in RCNST (Research Center for Nuclear Science and Technology), the University of Tokyo, and the proton irradiation experiment made in CYRIC (CYclotron Radio Isotope Center), Tohoku University, are discussed.

[1] http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm

5.2 Construction of Radiation tolerant electronics system

5.2.1 ASIC (Rohm[2] 0.35um process)

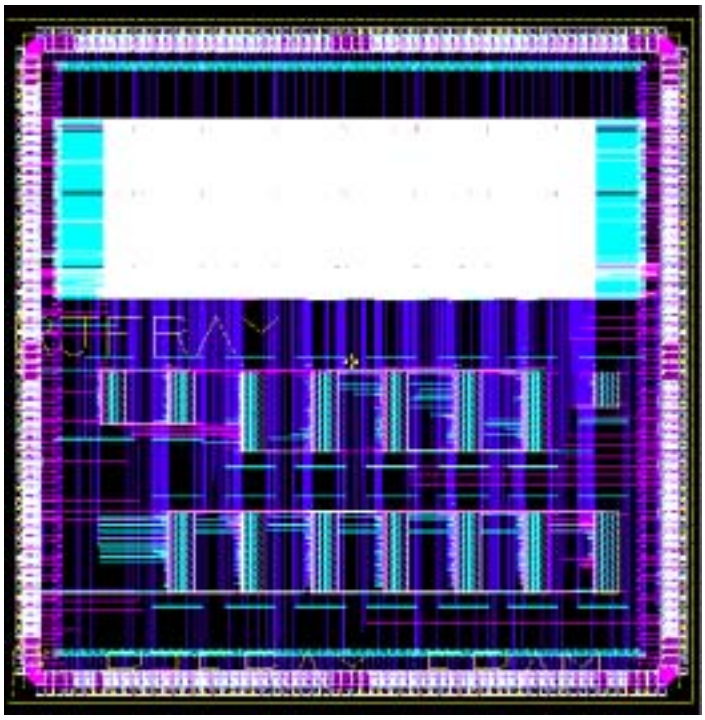

Figure 5-1 SLB ASIC Mask Layout

ASIC stands for Application Specific Integrated Circuit, and ASIC used for this test was made by Rohm (Kyoto), and this ASIC was made from the rule of the gate width of 0.35μm. Two ASICs created by Rohm among all ASICs used in the TGC electronics system, SLB (SLave Board) ASIC and PP (Patch Panel) ASIC, and SLB ASIC were used for the radiation tolerant test. Since PP ASIC is also made with 0.35μm gate width, characteristics for the radiation tolerance will be regarded well as identical as SLB ASIC.

SLB ASIC was tested for γ-ray irradiation experiment at RCNST, and this test result is described in subsection 5.3.

[2] Kyoto, Japan. http://www.rohm.co.jp/

5.2.2 CPLD (Xilinx[3] and Altera[4])

Figure 5-2 CPLD Chip (Xilinx XC95288XL)

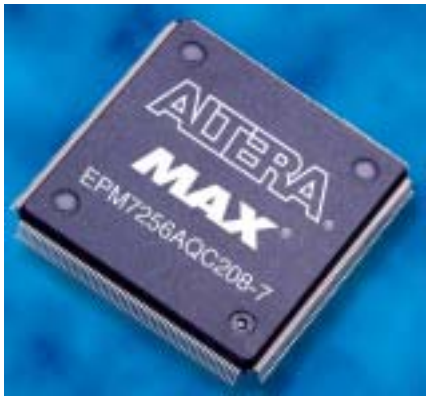

Figure 5-3 CPLD Chip (Altera EPM7256A)

CPLD stands for Complex Programmable Logic Device, and CPLD used for this test was made by Xilinx (U.S.) and Altera (U.S.). In TGC electronics group, we plan to use Xilinx CPLD (XC95288XL) for High-pT Board and Altera CPLD (EPM7512AE) for HSC Board.

CPLD was tested for proton beam irradiation experiment at CYRIC, and this test result is described in subsection 5.4.

5.2.3 G-Link

Figure 5-4 G-Link TX Chip (Agilent HDMP-1032)

Figure 5-5 G-Link RX Chip (Agilent HDMP-1034)

[3] San Jose, CA, U.S.A. http://www.xilinx.com/
[4] San Jose, CA, U.S.A. http://www.altera.com/

Figure 5-6 G-Link OE/EO Converter (Infineon V23818-K305-L57)

G-Link is the general term of the link system that can transmit data with gigabit transfer rate. In TGC electronics, since data must flow at very high bandwidth for the LVL1 trigger decision, and it must be synchronized, we have to build a system that can perform high-speed data transmission. Therefore, IC, which can respond to gigabit data transmission, is required, and OE/EO converter is also needed in order to use optical fiber because optical signal is hardly decayed and delayed for the distance over 50m. We have tested G-Link chips of especially Agilent[5] HDMP-1032/1034 and OE/EO converter of Infineon[6] V23818-K305-L57as we currently think these devices as the most profitable for our system.

G-Link was tested for γ-ray irradiation experiment at RCNST and for proton beam irradiation experiment at CYRIC, and both test results are described in Chapter 5.3 and 5.4.

5.2.4 LVDS

Figure 5-7 LVDS TX Chip (NS DS92LV1023)

Figure 5-8 LVDS RX Chip (NS DS92LV1224)

[5] Palo Alto, CA, U.S.A. http://www.agilent.com/
[6] Munich, Germany, http://www.infineon.com/

LVDS stands for Low Voltage Differential Signaling[7], and by taking two difference signals as the name shows, the influence by fluctuation of GND and the decay of signal can be smaller than a single ended signal protocol as TTL. LVDS allows the ICs to transfer data with high data rate ranging from 100's Mbps up to 1 Gbps. Additionally, the low voltage swing minimizes power dissipation while providing the benefits of differential transmission. We have used LVDS chips (NS[8] DS92LV1023/1224) for this test.

LVDS was tested for γ-ray irradiation experiment at RCNST and for proton beam irradiation experiment at CYRIC, and both test results are described in section 5.3 and 5.4.

5.2.5 Remote control System

In the irradiation environment, we cannot access to the experimental area so often and are shut out where activity is high. Therefore, we have built a remote control system so that all the experimental apparatuses under irradiation test could be controlled from the other place away from the irradiation area.

This remote control system is roughly divided into two systems. One is the control system of experiment equipment and the other is the real-time data acquisition (DAQ) system.

The control system of experiment equipments is a system which operates the position of the target device (Device Under Test (DUT) like ASICs or CPLDs in the present case) which is irradiated. An X-Y stage called super FA KL-type[9] made by THK[10] was used for this position adjustment. The X-Y stage requires one dedicated PC to be controlled. We have installed our own developed stage-control system into that. The software was run under the Windows environment. We have to, however, operate this software remotely from the radiation-safe control area.

[7] http://www-s.ti.com/sc/psheets/slla038a/slla038a.pdf
[8] National semiconductor. Santa Clara, CA, U.S.A. http://www.national.com/
[9] http://www.thk.co.jp/pro/20300050.htm
[10] Tokyo, Japan. http://www.thk.co.jp/

Figure 5-9 X-Y stage (THK)

Figure 5-10 X-Y stage complete image

We have been able to use VNC (Virtual Network Computing) system. It is, in essence, a remote display system which allows you to view a computing 'desktop' environment not only on the machine where it is running, but from anywhere on the Internet and from a wide variety of machine architectures. VNC system was developed by AT&T Laboratories Cambridge.

Figure 5-11 VNC system screen shot

Therefore we could control the X-Y stage under irradiation environment by operating PC with VNC system, and the actual software ran in the PC placed in the radiation environment.

The real-time data acquisition (DAQ) system is the system for continuing taking log of experiment on-line data. In this experiment, DAQ software can be running on Linux, so X11 forwarding with ssh was used for online monitoring, and data logs were written to files.

5.3 γ-ray irradiation experiment at RCNST (Univ. of Tokyo)

In December 2001, we have made γ-ray irradiation test at RCNST, Univ. of Tokyo. We have irradiated following devices;

- Agilent 3.3V G-link serializer (1032)/deserializer (1034),
- Infineon EO/OE converter (V23818-K305-L57),
- NS 3.3V LVDS serializer (DS92LV1023)/deserializer (DS92LV1224), and
- Rohm 0.35u ASIC (SLB ASICs).

Results of the experiment are discussed in this section, together with the experiment system setup we have made for the test.

5.3.1 Experimental Setup

The γ-ray irradiation has been performed with the ^{60}Co facility of RCNST, Univ. of Tokyo. The facility is well calibrated with Fricke dosimetry and the half-life of ^{60}Co. The total dose is about 20 krad(Si) which is slightly larger than the RTC[11] required. The dose rate is about 50 krad/hr.

Figure 5-12 is a setup image of γ-day irradiation for G-link/LVDS chip sets. Data & DAQ lines are removed in the case of ASIC test because of offline data taking check.

Figure 5-13 is LVDS test board setup photo.

Figure 5-14 is SLB ASIC test board setup image. Right photo shows overview of online current monitoring setup, and left photo shows ASIC test board setup.

[11] Radiation Tolerance Criteria. http://tgce.icepp.s.u-tokyo.ac.jp/technology/radtol/index.html. The ATLAS radiation-assurance team has made calculation and simulation of Total dose for various parts of the detector assuming the high luminosity Proton-Proton 14TeV collision with LHC for ten years operation. The team published the total dose for places where sub-detector electronics would be installed. The TGC electronics were estimated to be suffered as about 20krad according to this estimation. Numerical detail will be found in section 5.3.2.

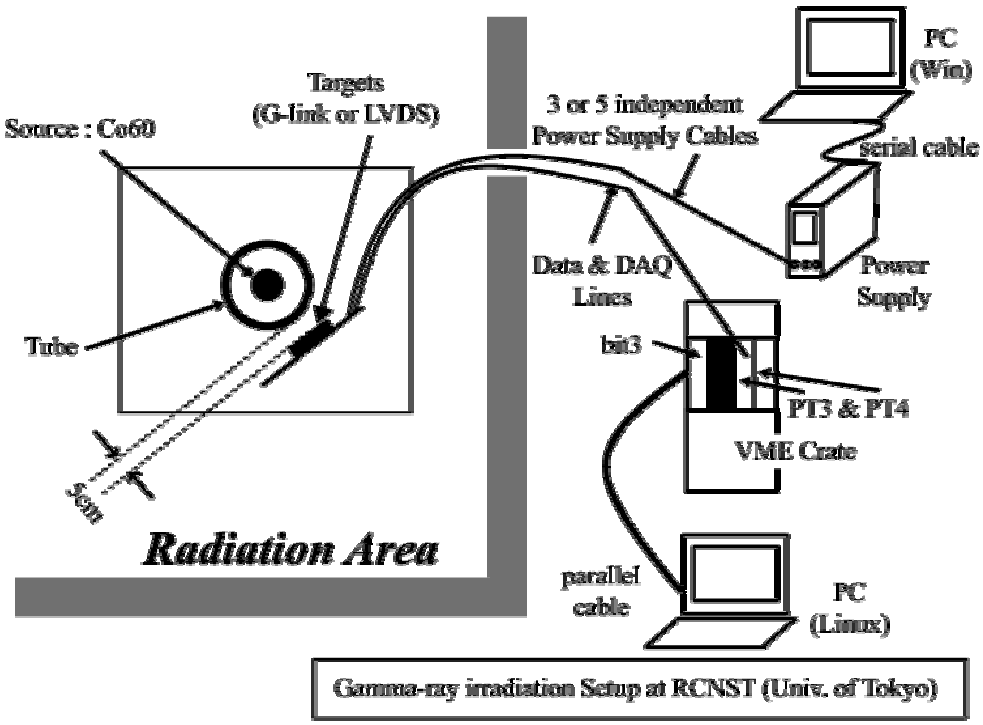

Figure 5-12 γ-ray irradiation setup for G-link/LVDS chip set

Figure 5-13 LVDS test board setup

Figure 5-14 SLB ASIC test board setup

5.3.2 Data acquisition and Calibration

Although three sets of ICs were tested in this radiation test, every DAQ system has slightly different parts rather than most common ones. These DAQ methods are discussed in this section.

G-link

G-link chip set consists of a set of EO/OE converter, G-link RX and G-link TX. During the irradiation, the board was biased 3.3V (normal operating voltage). Total Vcc current of the set was monitored and logged by a digital multi meter (DMM) with a PC (Win). A local control/monitor (LCM) system has been built for the test. The LCM is based on VME and uses general-purpose modules, PT3[12] and PT4[13], which Kyoto University group of our collaboration has developed. The LCM sends two 16-bit test

[12] Proto Type 3 module, http://www.hep.scphys.kyoto-u.ac.jp/~nishida/atlas/pt3/
[13] Proto Type 4 module, http://kuhes3.hepnet.scphys.kyoto-u.ac.jp/~sakamoto/research/atlas/tgcelex/development/prototyping/pt4/

patterns (checker patterns: 0x5555 and 0xaaaa) alternatively in 40.08 MHz to the G-link RX via OE conversion; received data are transferred directly to the G-link TX on the same board and are sent back again to the LCM after EO conversion. The consistency of the data was checked there. All the link error signals were also monitored and logged by the LCM. The data sent and data received are compared in a FPGA chip mounted on PT3/PT4.

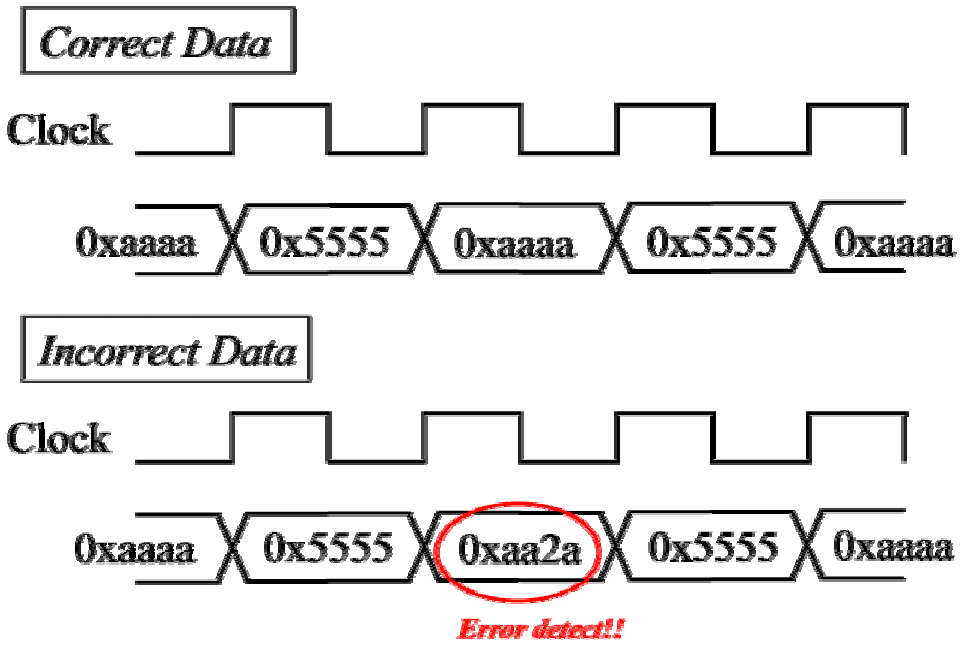

Figure 5-15 data checking image

LVDS

LVDS chip set consists of a set of LVDS RX and LVDS TX. During the irradiation, the board was biased 3.3V (normal operating voltage). Total Vcc current of the set was also monitored and logged by a DMM with a PC (Win). Similar manners of validity check for the data transfer as ones done in the G-Link irradiation were applied. The same 10-bit checker patterns (checker patterns: 0x155 and 0x2aa) were used.

SLB ASIC (Rohm 0.35um)

Two SLB ASICs were irradiated. First we checked the basic functionality of the ASIC and measured the Vcc current in various conditions (non-clocked, clocked, data-in) as the pre-irradiation measurements. During the irradiation, ASICs were biased;

the one fed a 50-MHz clock; the other fed no clock. Each current was monitored and logged by DMMs.

After the irradiation up to RTC, post-irradiation measurements (same as pre-irradiation) had been performed.
(RTC = 0.249 x 3.5 x 5 x 4 = 17.43 krad for 10-year LHC operation)

5.3.3 Results

The results of the γ-ray radiation experiment are summarized for each set of ICs here.

G-link and LVDS

We had no error for both G-link and LVDS during the irradiation. No data inconsistency was observed; no link errors occurred. The total current is stable and no significant increase was observed. Following graphs are shown the measurement of total current and lowest voltage that operates correctly. Idle mode is the state that no data is flowing. Dataflow mode is the state that valid data is flowing. Dataerr mode is the state that invalid data is flowing. Figure 5-16,17,18 are the measurement of total current and lowest voltage that operates correctly for both G-link and LVDS. Target ICs were irradiated with 25krad after pre-irradiation check. Other checks with annealing are done without irradiation.;

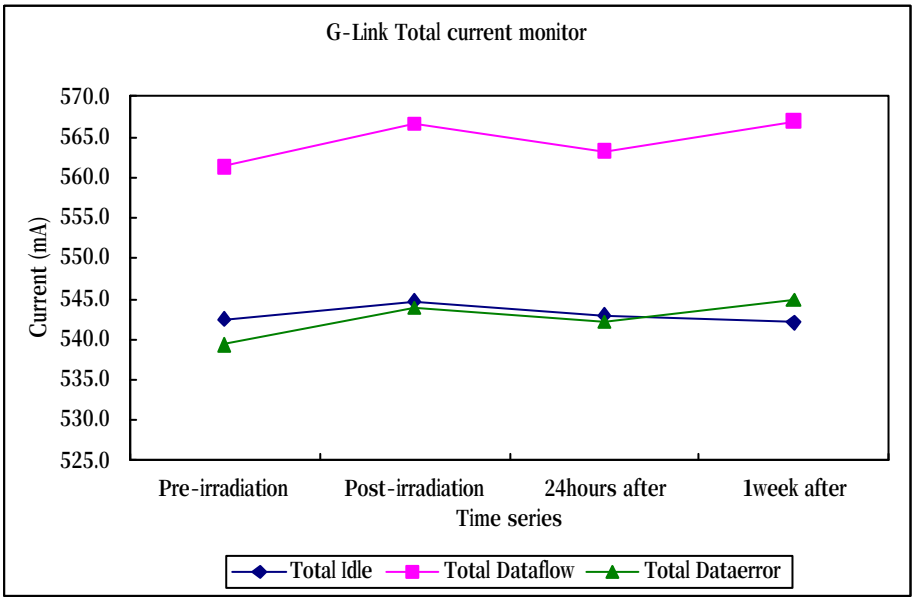

Figure 5-16 Total current of G-link test board

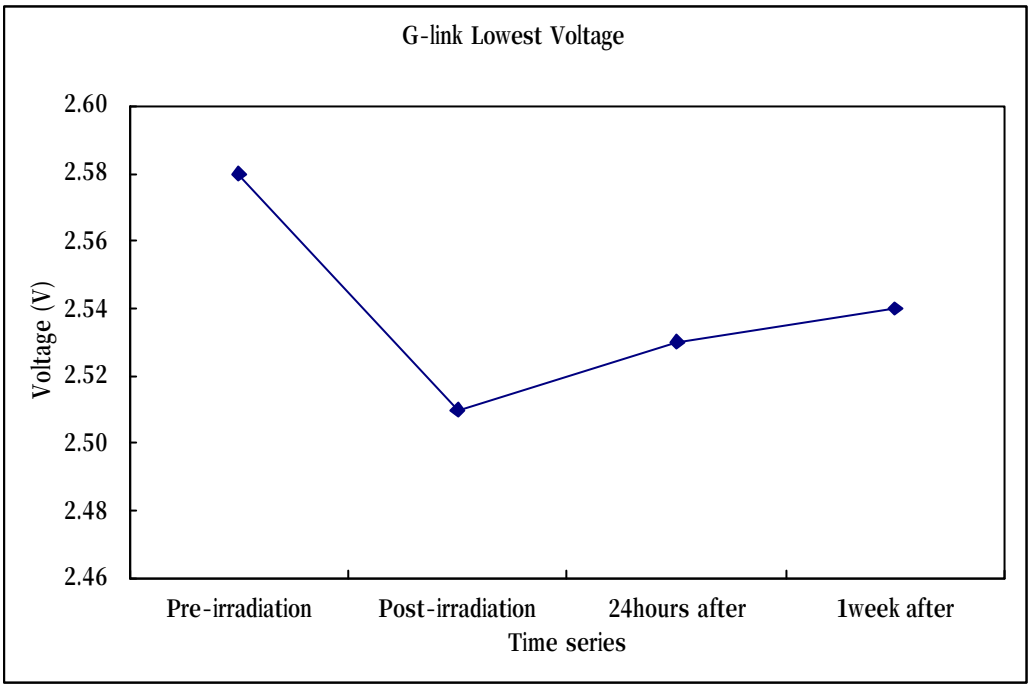

Figure 5-17 Lowest Voltage of G-link test board

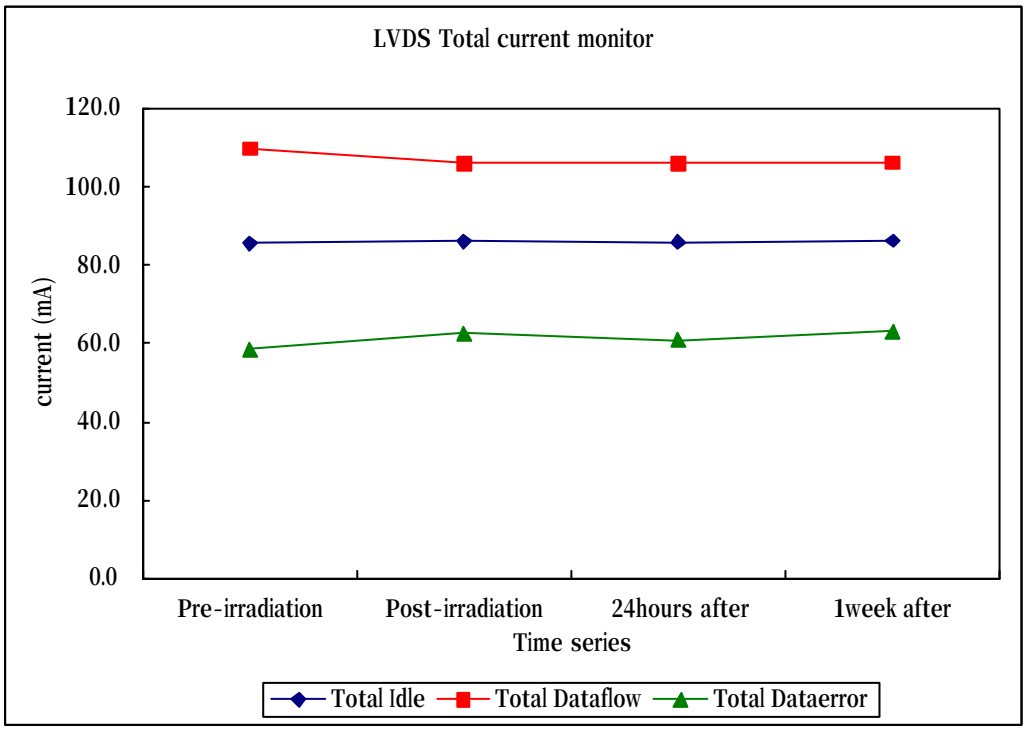

Figure 5-18 Total current of LVDS test board

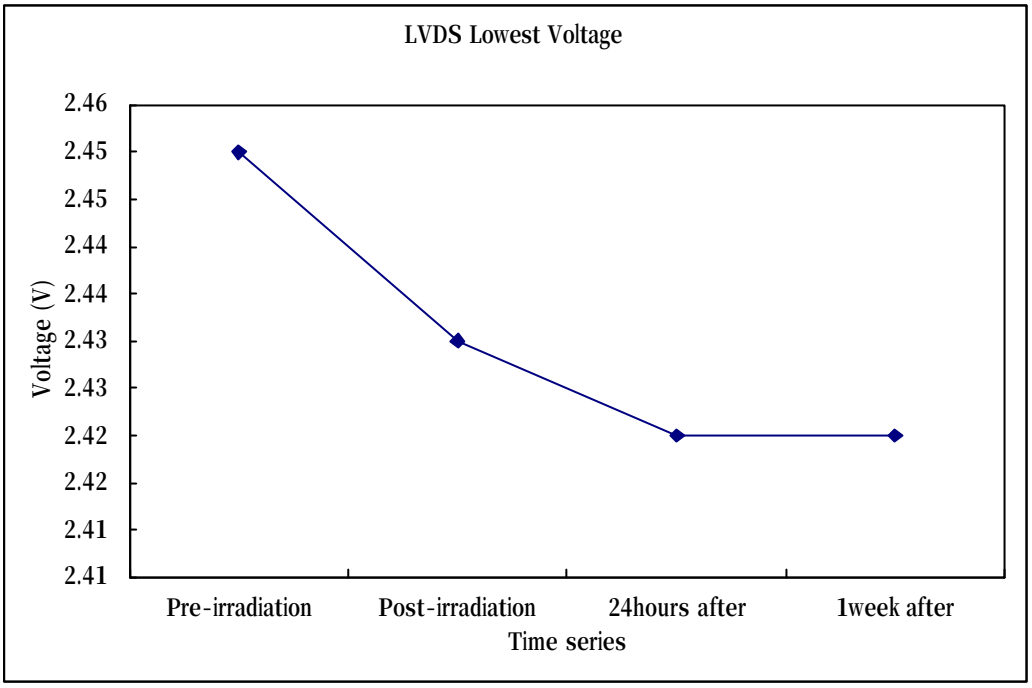

Figure 5-19 Lowest Voltage of LVDS test board

As these graphs show, since the big rise of current values over 10% is not seen and the minimum voltage is almost stable, we find that there is no damage by irradiation of γ-ray for G-link and LVDS. From these results, we guess G-link and LVDS have sufficient tolerance over the γ-ray in the 10 years of ATLAS experiment.

ASIC (Rohm 0.35um)

We had observed no functional errors in the post-irradiation measurements. The currents were stable during the irradiation and no significant increase was observed.
Figure 5-20,21,22 are the measurement of total current and lowest voltage, which show the ASICs were operated correctly;

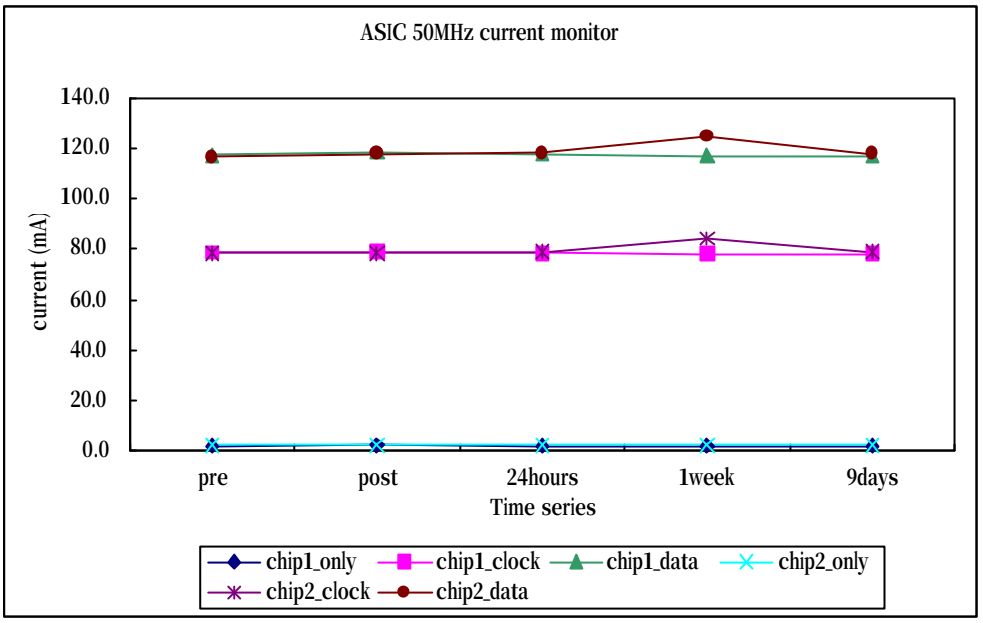

Figure 5-20 Total current of ASIC test board @ 50MHz

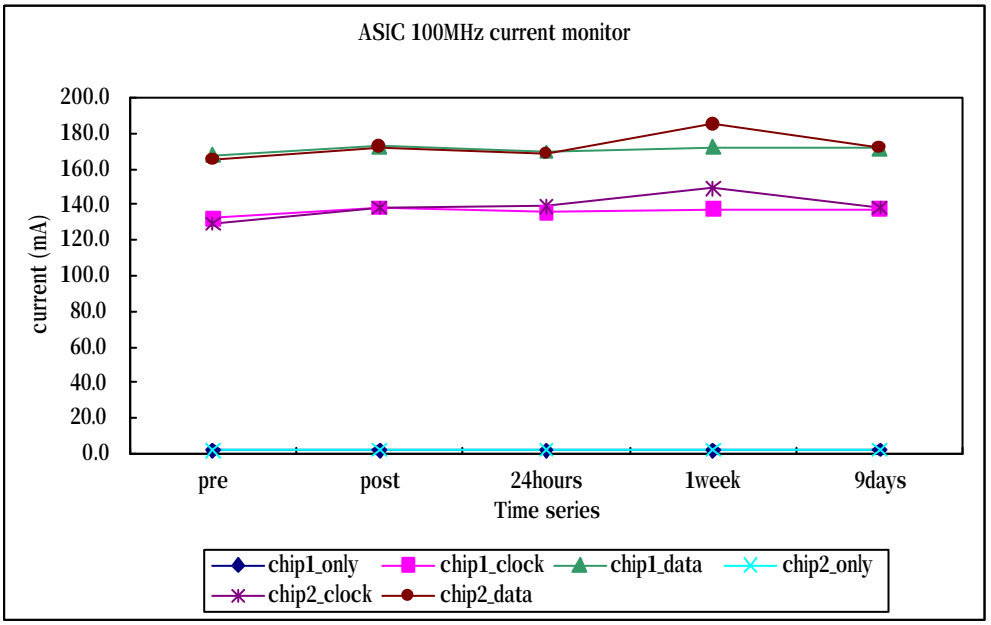

Figure 5-21 Total current of ASIC test board @ 100MHz

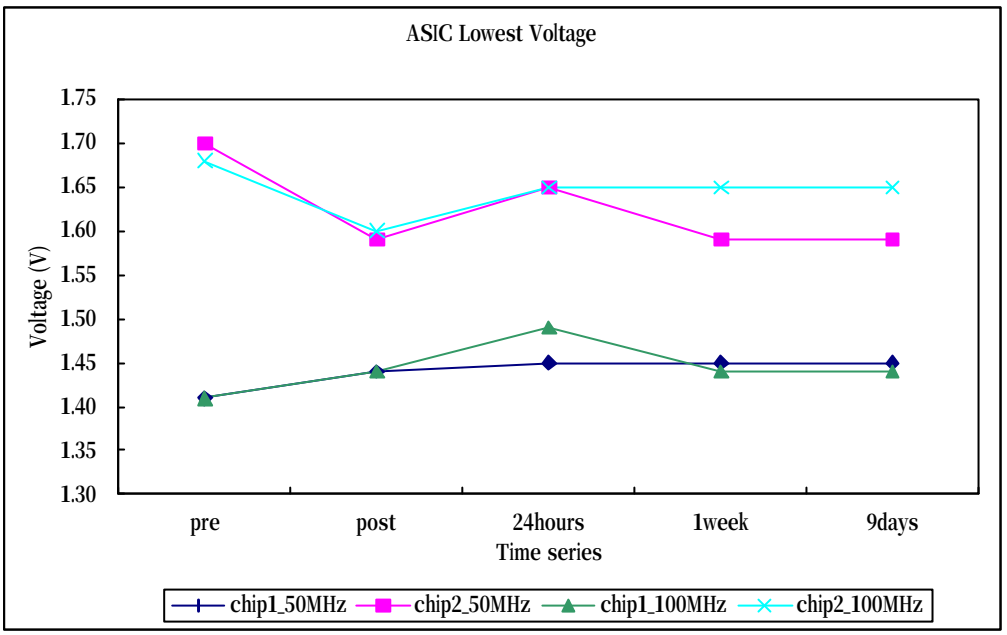

Figure 5-22 Lowest voltage of ASIC test board

As these graphs show, since the rise of current values was hardly seen and the minimum voltage values were slightly changing, we found that there is no damage by irradiation of γ-ray for Rohm ASICs. From these results, we conclude Rohm ASICs have sufficient tolerance against γ-ray over the 10 years of ATLAS experiment.

5.4 Proton irradiation experiment at CYRIC (Tohoku Univ.)

In December 2001, we have experimented proton irradiation test at CYRIC, Tohoku Univ. We have irradiated to the following devices:

- Agilent 3.3V G-link serializer (1032)/deserializer (1034),
- Infineon EO/OE converter (V23818-K305-L57),
- NS 3.3V LVDS serializer (DS92LV1023)/deserializer (DS92LV1224),
- Xilinx CPLD (XC95288XL), and
- Altera CPLD (EPM512AE).

Both results and the setup of the experiment are discussed in this section.

5.4.1 Experimental Setup

The proton irradiation has been performed with proton beam energy 50MeV and beam current 1nA to 4nA in this setup at CYRIC, Tohoku Univ., although both parameters were adjustable.

Figure 5-23 is a setup image of proton irradiation for G-link/LVDS chip sets.

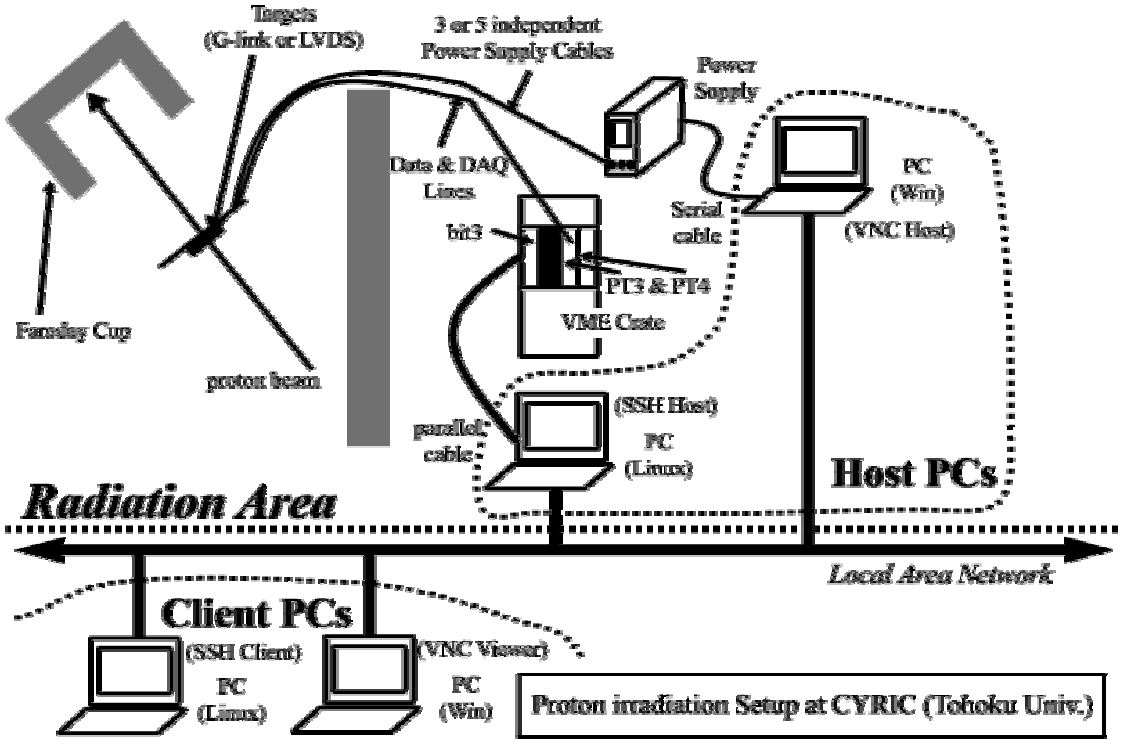

Figure 5-23 Proton irradiation setup for G-link/LVDS chip set

Figure 5-24 is a setup image of proton irradiation for CPLD chip.

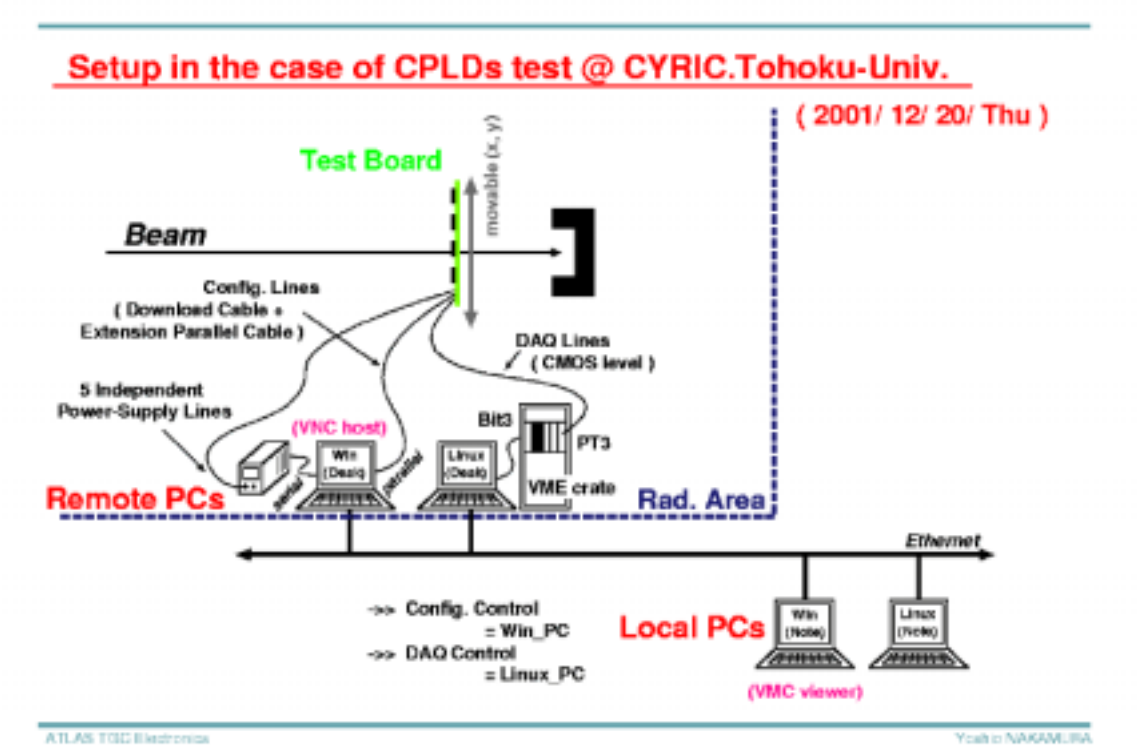

Figure 5-24 proton irradiation setup for CPLD chip

5.4.2 Data acquisition and Calibration

Although three sets of ICs were tested in this radiation test, three DAQ methods have difference. These DAQ methods are discussed in this section.

G-link

The same setup as the γ-ray irradiation experiment has been used. Refer to the section 5.3.2. In addition, the remote control system for the X-Y stage is used because we could not enter the radiation area.

LVDS

The same setup as the γ-ray irradiation experiment has been used. Refer to the section 5.3.2. In addition, the remote control system for the X-Y stage is used because we could not enter the radiation area.

CPLD

Figure 5-25 is DAQ flow chart for CPLD test. Since CPLD is programmable logic device, it is judged whether the design of test circuit is downloaded to CPLDs correctly and whether CPLDs operate correctly during irradiation.

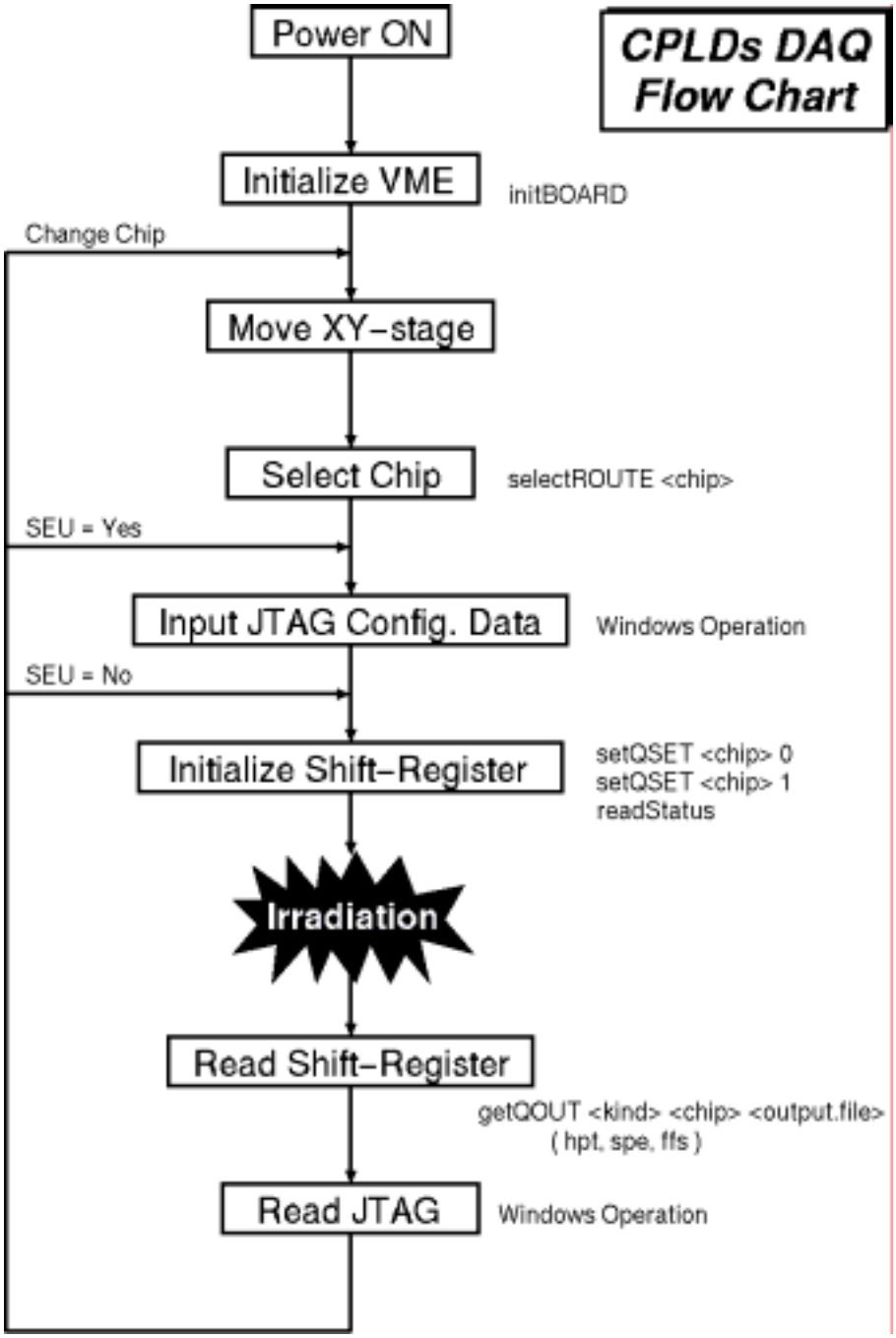

Figure5-25 DAQ flow chart for CPLD

5.4.3 Results

Results of the proton radiation experiment are summarized for each set of ICs in this section.

- G-link and LVDS

We had some errors for LVDS but many errors for G-Link during the irradiation. In LVDS, data inconsistency was observed mainly; one link error occurred. However in G-Link, a lot of data inconsistency was observed and IC status signals are almost inconsistency; 29 link errors occurred. In both of ICs, the total current is stable and no significant increase was observed. Table 5-1 shows total error rate at TGC area.

	Radiation time	Total dose (proton)	Total error	Link error	Error rate at TGC area
G-link	660sec	6.6×10^{10} p/cm^2	336	**29**	**0.007errors/link/hour**
LVDS	1860sec	1.86×10^{11} p/cm^2	197	**1**	**0.0013errors/link/hour**

Table5-1 Total Error Rate

Reaction cross sections per device are;

$$\text{Cross section} : \sigma = 1.7 \times 10^{-9}\ \text{cm}^2/\text{device}\ \text{(G-link)}$$
$$\sigma = 5.5 \times 10^{-10}\ \text{cm}^2/\text{device}\ \text{(LVDS)}$$

All errors are but temporary error (soft error) not hardware break (hard error).

From this result, LVDS may be operated correctly under hadron shower. But G-Link may not be operated correctly.

However we have tested only one set of each ICs, so we should test many set of ICs.

Figure 5-26,27,28,29,30 are the beam profile in the radiation test of LVDS and G-Link.

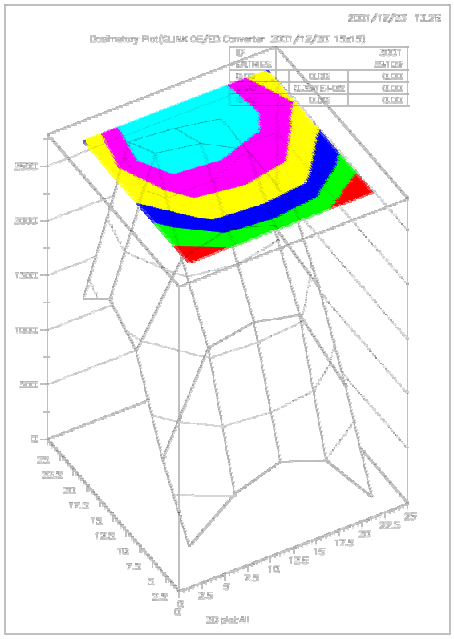

Figure 5-26 beam profile of G-Link OE/EO

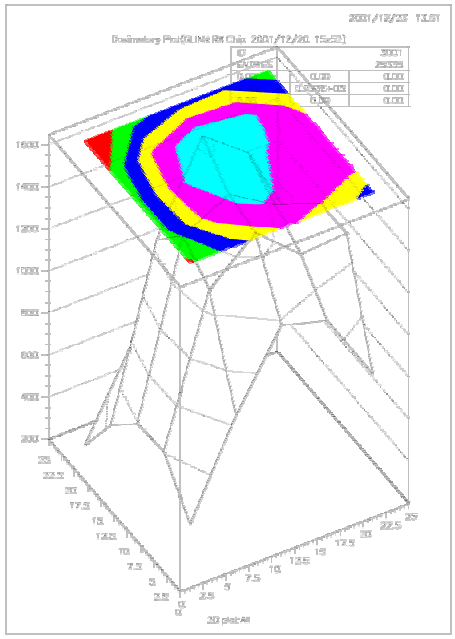

Figure 5-27 beam profile of G-Link RX

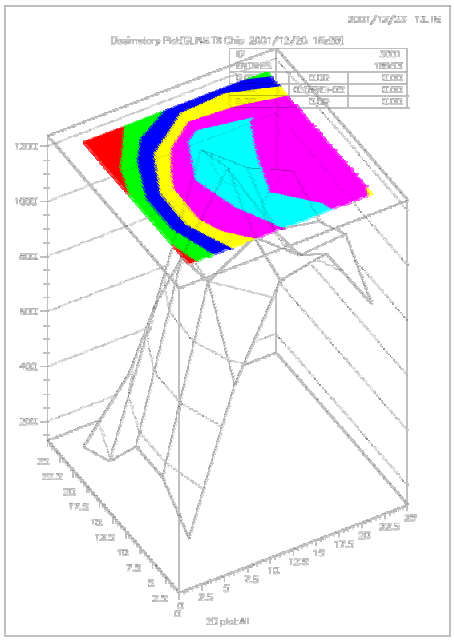

Figure 5-28 beam profile of G-Link TX

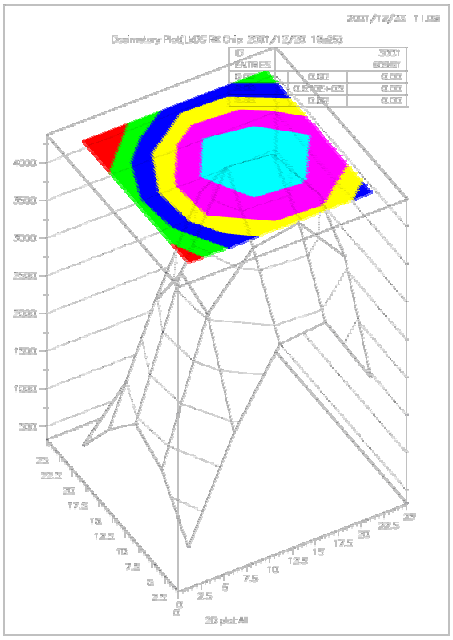

Figure 5-29 beam profile of LVDS RX

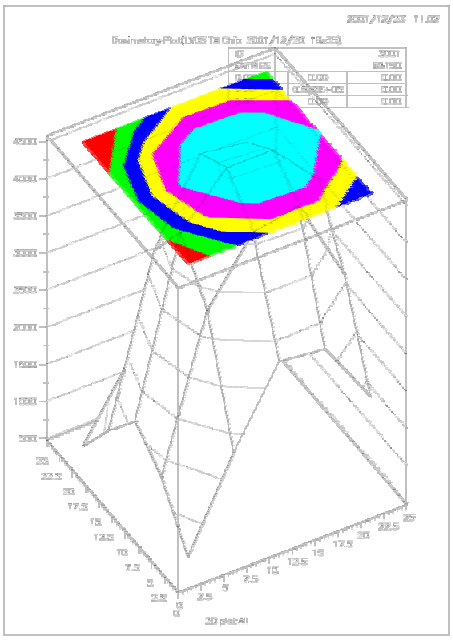

Figure 5-30 beam profile of LVDS TX

- CPLD

Chip ID	Radiation Time	Total dose (proton)	SEU Error	Diagnostic Error
Xilinx 00	540 sec	$3.0x10^{11}p/cm^2$	**3**	0
Xilinx 01	450 sec	$2.8x10^{11}p/cm^2$	**0**	0
Xilinx 03	900 sec	$1.6x10^{11}p/cm^2$	**4**	1
Altera 02	600 sec	$1.1x10^{11}p/cm^2$	**0**	0
Altera 02	420 sec	$1.0x10^{11}p/cm^2$	**0**	0

Table5-2 Radiation test data of CPLD

Three Xilinx CPLDs and two Altera CPLDs are irradiated. SEU (Single Event Upset) Error occurred about two Xilinx CPLDs; one has 3 errors and another has 4 errors. reaction cross section is calculated from these result;

Cross section : $\sigma = 1.0x10^{-11}\ cm^2$ (Xilinx 00)

$\sigma = 3.1x10^{-11}\ cm^2$ (Xilinx 03)

Two CPLDs (Xilinx 00, 01) were destroyed with the rapid rise of current, while another CPLDs were destroyed with no change of current. It was not able to control CPLDs

from the outside of ICs and configure CPLDs. Since there were the rapid rise of current about Xilinx 00 and 01, the influence of total dose by the gamma ray can be considered. In the future, it is necessary to check CPLDs by gamma ray radiation test for considering the cause of destruction of all CPLDs.

When it is compared with Xilinx and Altera, Xilinx CPLDs have larger reaction cross section than Altera CPLDs. Now there are many devices using Xilinx CPLDs, but we have to consider changing from Xilinx to Altera.

6, Conclusion

The TTC system is developed as a common system for all the experiments with LHC including ATLAS experiment, and is used to distribute the common signals about time-axis to read-out systems. The time-axis must be unified. We should identify an event observed with two or more detectors as the same event. Since the TTC system is general-purpose one, signals without necessity for the individual experiment or sub-detectors in an experiment are included. Therefore it needs to consider a system customized for each experiment and electronics system.

Throughout the graduate course, the author has developed and tested the various modules for the application of the TTC system (TTC modules), which specialized for the TGC electronics. Moreover, not only these modules but in order to mount on directly, the author has made the design of TTC system in the ROD module. These will be used for the actual experiment that will start from 2006, and will be useful to the analysis of the muon.

SPP actually is connected with the PS board, and is used for debugging of PP and SLB. Although test of SPP is done in one channel since there is only one PS board now, test of all the functionality will be done in the next years. However, since the same signal is distributed to PS boards, it is hard to occur a problem. This can also apply to the LVDS Fan-out board.

ROD uses more TTC signals than the TGC trigger part, the author has checked that ROD accepts correctly many TTC signals as we intended.

TTC emulator, which we have developed, will be useful since this generates simply TTC signals by just being installed instead of TTCrx test board on SPP, Fan-out board or ROD. It may be obliged to changing the TTC modules for upgrade and specification change of TTC signals etc. It is thought that there is no big change in the basic specifications, and that big influence does not give development of modules of TGC electronics. Even when there is a big change for TTC specifications, we can respond to this change immediately by reprogramming the FPGA installed on TTC emulator. It is expected that time lag until the modules of new TTC standard is completed is

compensated.

The radiation tolerant test is also conducted. This test is important since actual environment is under radiation-active region, when ICs do not wear correctly, we must reconsider to apply the same technology of ICs in the TGC electronics. We have to in this case develop radiation tolerant or even rad-hard ICs rather than ones built with the rad-soft technology. It was successful in the γ-ray irradiation experiment for all the components we have tested, but some problems were revealed in CPLD and G-Link test in the proton irradiation experiment. It is an important problem, because it is related especially with G-Link from the viewpoint of high-speed data transmission and G-Link is used not only in TGC electronics also in the electronics system of other sub-detectors in ATLAS. It has been tested only one set in this test. We need more statistics to make final conclusion for G-link chip. We keep also proceeding the radiation test experiments with increasing the number of individual chips. This makes the results more reliable.

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