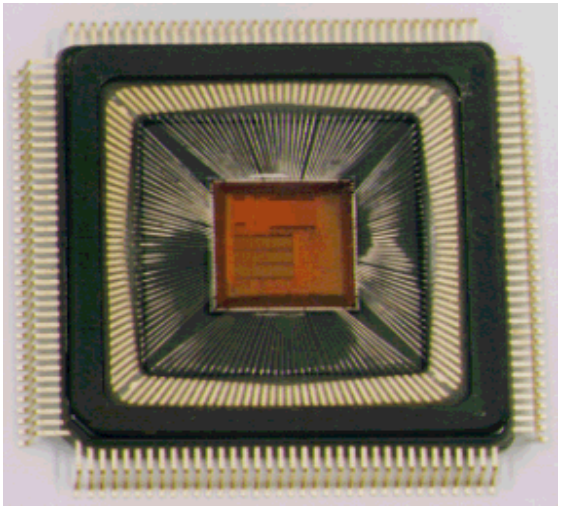
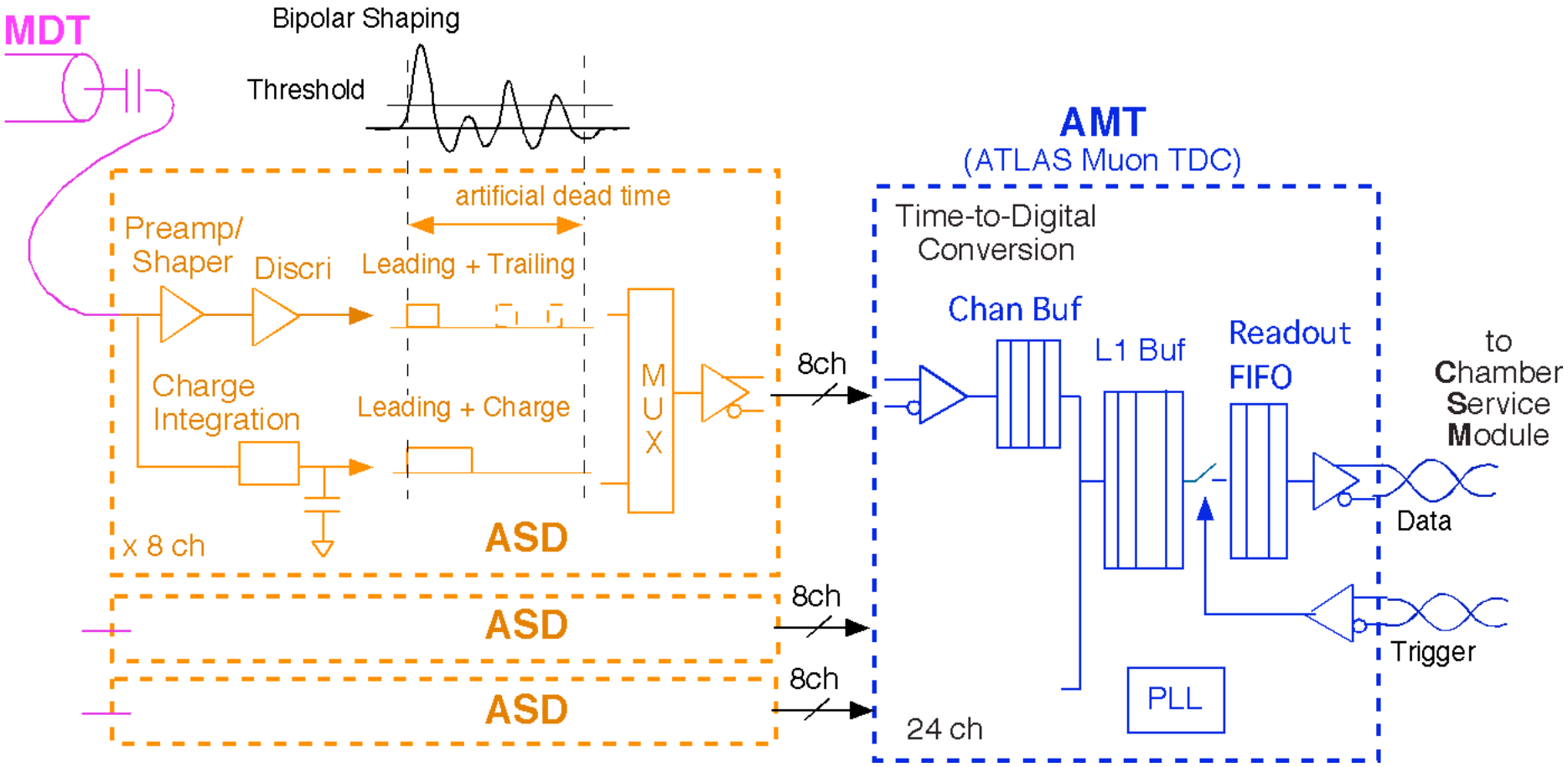
# AMT-3: Pair mode issue & New Simulation Results

24 Feb 2004@CERN
Yasuo Arai (KEK)
*yasuo.arai@kek.jp*
http://atlas.kek.jp/tdc/

- Introduction
- Short Pulse effects in Pair mode
- Simulation at New Conditions
- Summary

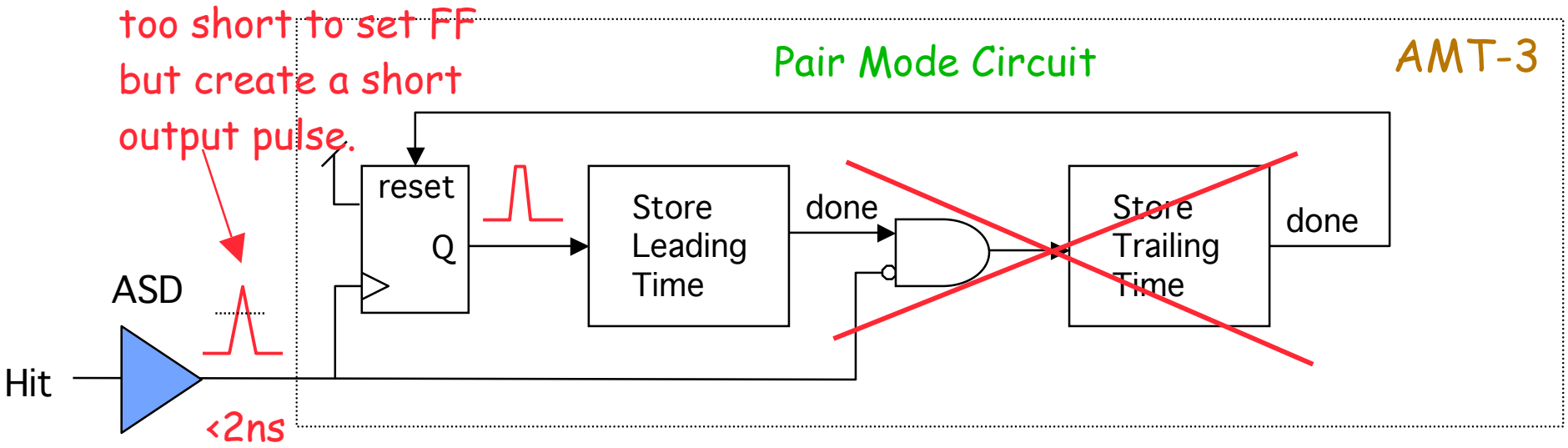


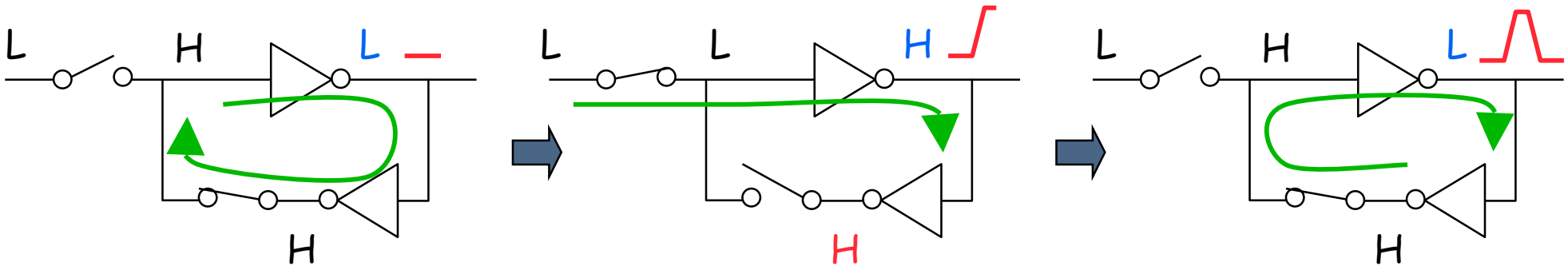
# ATLAS MDT Front-end Electronics



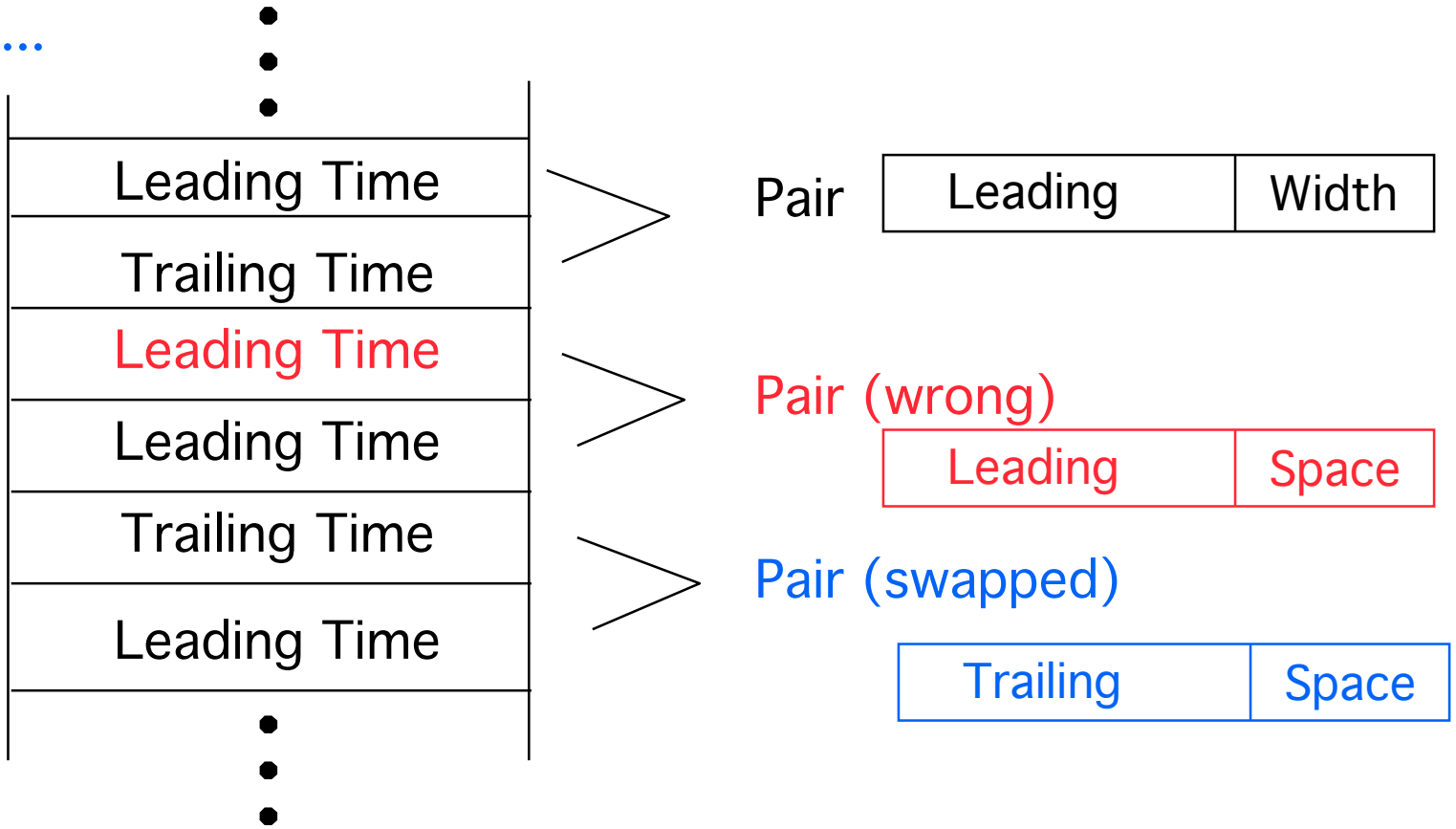
# Short Pulse Effects in Pair (Leading + Width) Mode

A phenomenon is found in that most of hits are lost for some period in pair mode. This is explained by a very short pulse from the ASD.



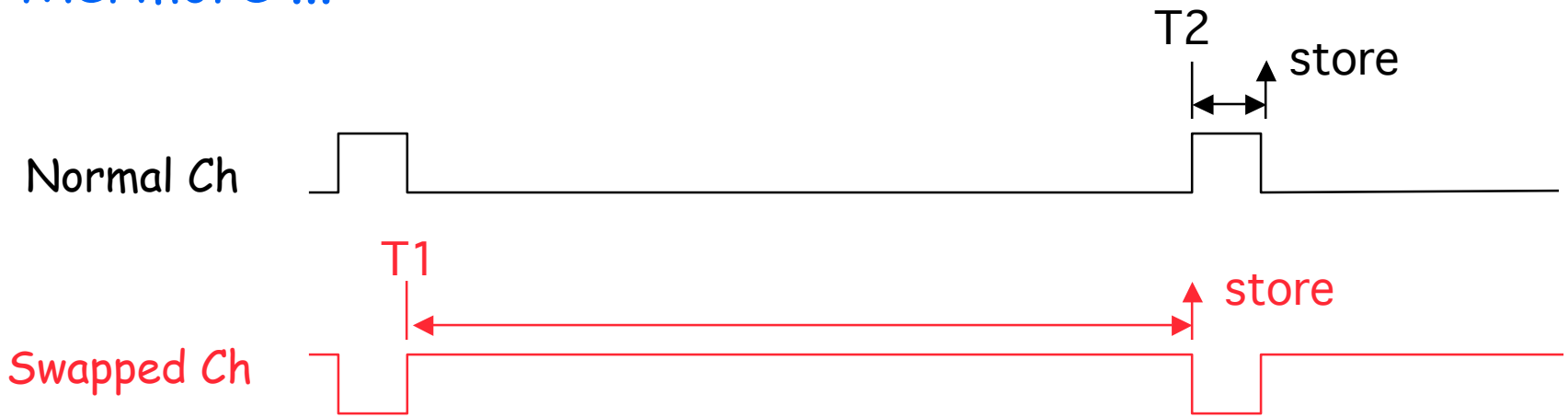



Then ...

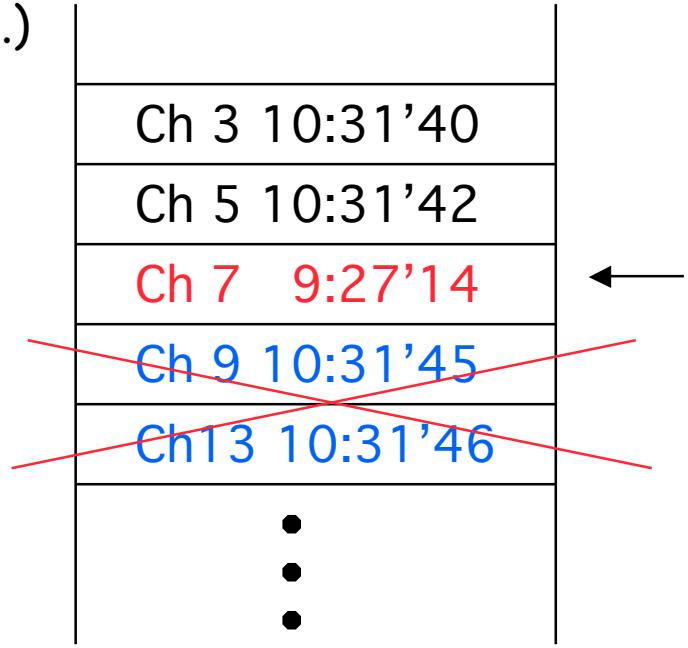



Leading edge time and Trailing edge time are swapped. Then pair data has wrong leading edge time. Thus it becomes outside of matching window.

# Furthermore ...



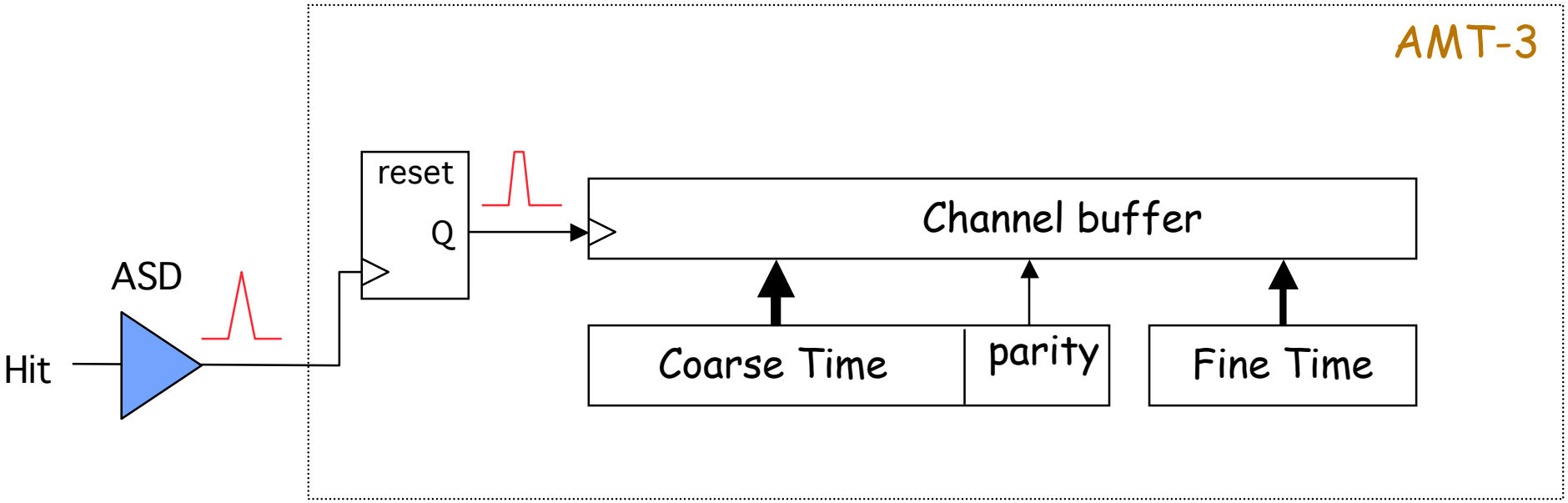

Ex.)




This is actually early data but regarded as late data since large difference of time, so following data of other channels are also regarded as late data.

Swapped Ch data also blocks normal Ch data! Therefore all ch in a mezzanine card are affected.

# and may also cause ...




Unstable load of Coarse/Fine Time --> coarse counter parity error.

# Summary for short pulse input

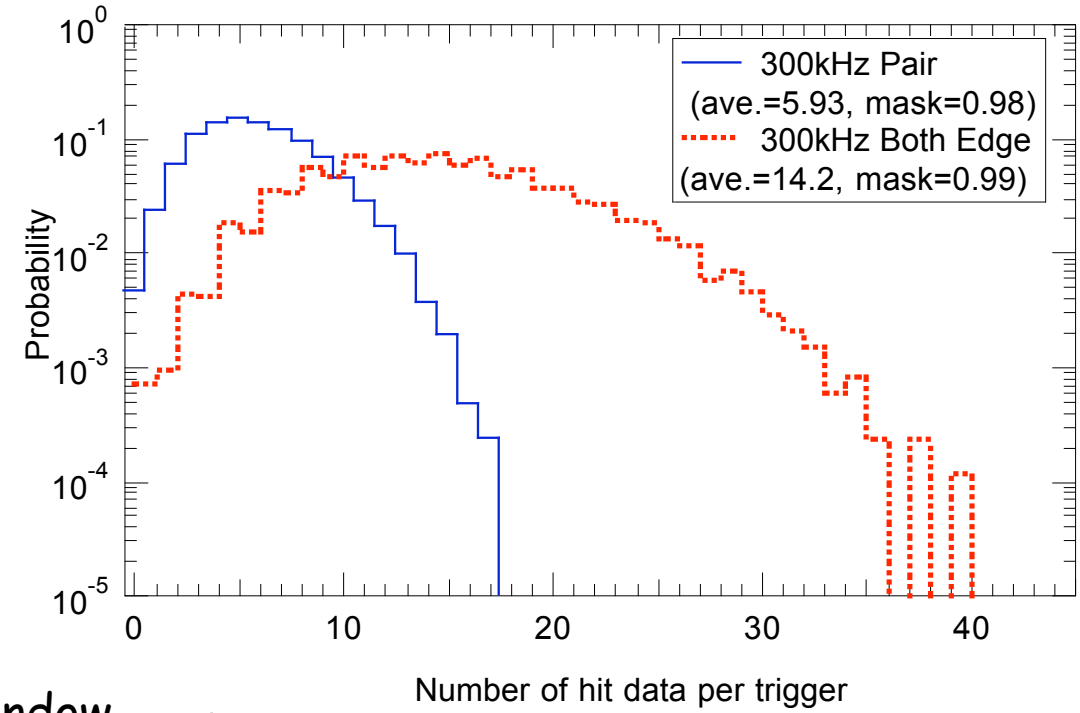
- A short pulse input of less than 2 ns width can not set 1st flip-flop, but generate a short output pulse. Thus only a leading edge is stored in pair mode.
- Then leading and trailing edge are mistaken afterward. This mistake will last until next short pulse.
- Due to the data driven architecture of the AMT, the mistaken data may also block other normal channel data.
- The short pulse also cause unstable latch of the coarse and fine time (coarse counter parity error).
- The same phenomena can be happen also in edge mode, but it is only temporally.
- The effects can be minimized by re-designing pair matching logic, but it is difficult to eliminate such short pulse effects perfectly in digital LSI.

# Data Flow Simulation of AMT

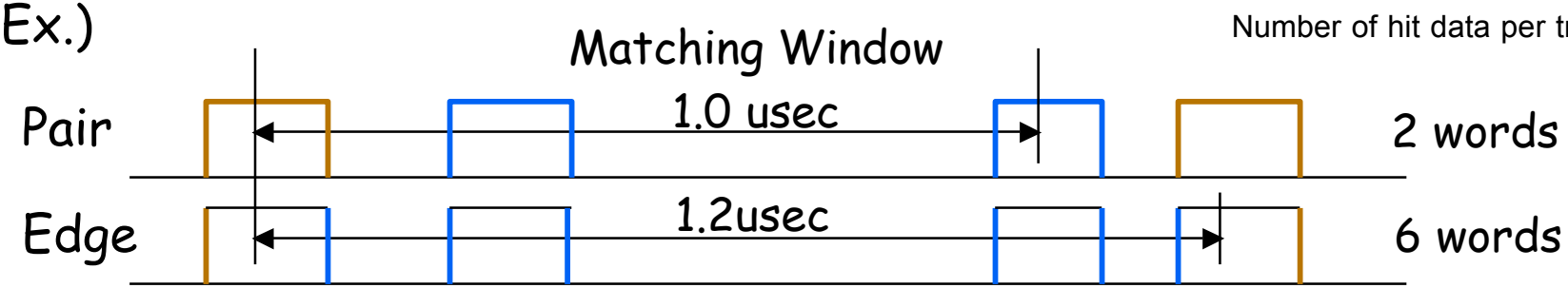
Data flow simulation have been done by using AMT-3 Verilog codes.
Assumed conditions are follows;

- Trigger rate : 100kHz
- Hit Rate : ~ 300kHz x 24ch
- Trigger latency : 2.5 μs
- Drift time : 0 ~ 800 ns
- Pulse width : 10 ~ 200 ns
- Dead time : 800 ns
- Mode : Pair (Leading edge + Width) or Leading & Trailing Edge
  (Pair mode and Leading edge only mode are almost same)
- Matching window = 1000 ns (@Pair) or 1200 ns (@Edge)
- Header, Mask, and Trailer words are read out
- Serial readout : 40Mbps (80Mbps)
- Buffer control :
  enable rofull reiect=enable l1full reiect=enable trfull reiect=1.

# Average Data Size



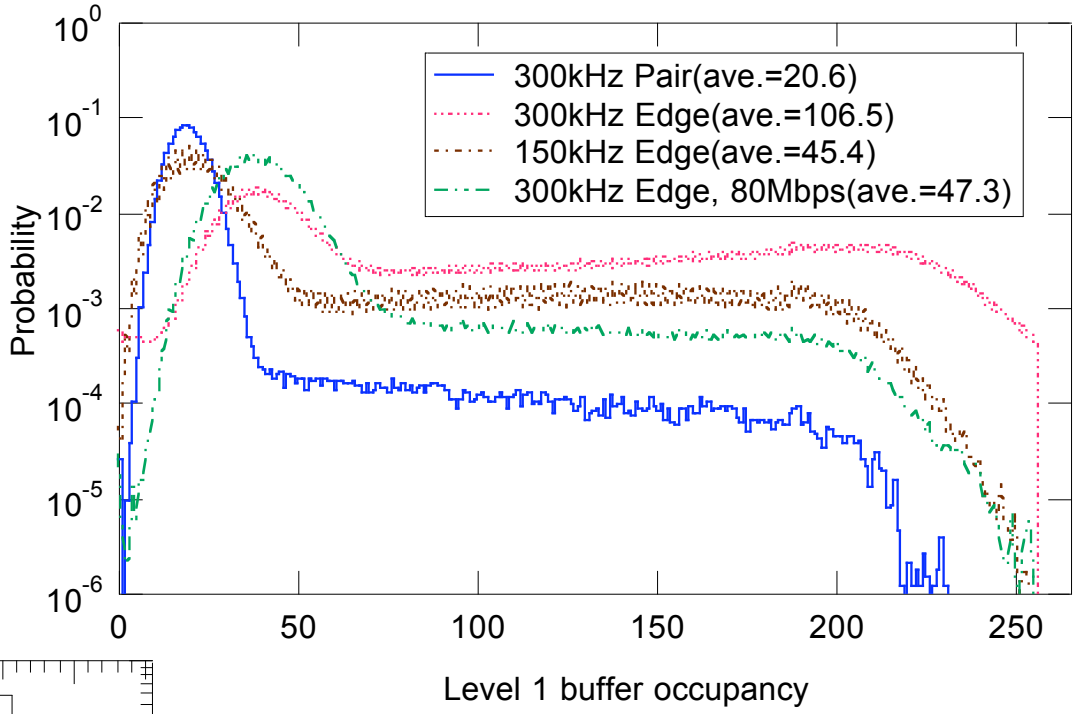

Ex.)

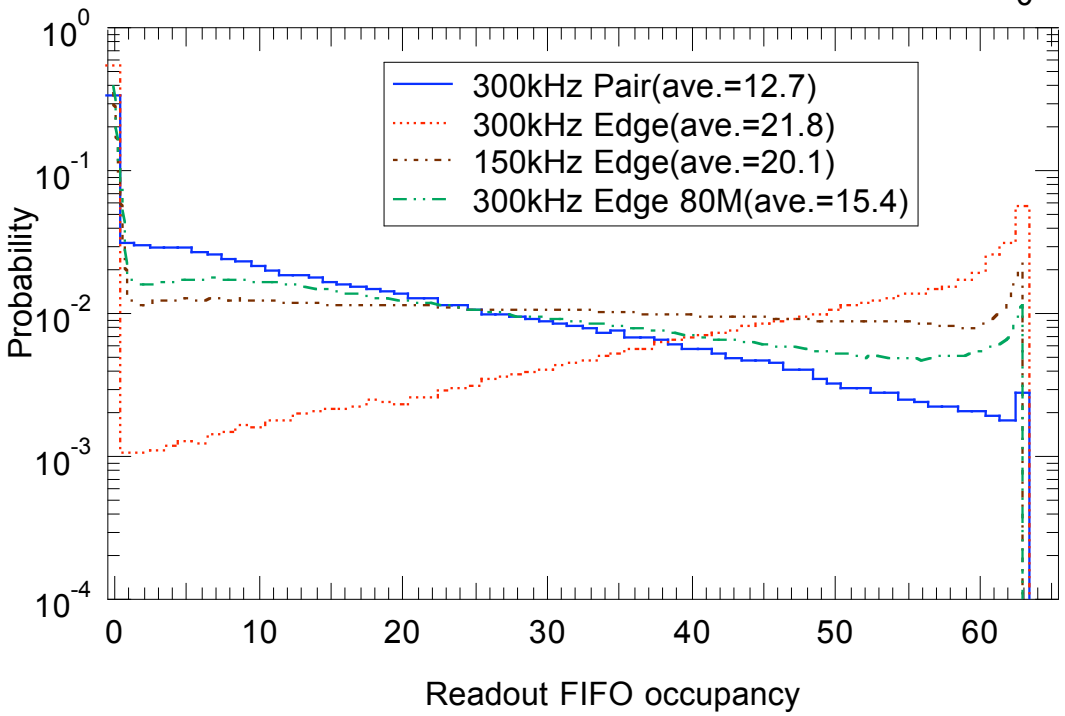



| Hit Rate | Mode | No. of Hits | No. of Mask Word | Total No. of Words (incl. head and trailer) |
|---|---|---|---|---|
| 300 kHz | Pair | 5.93 | 0.98 | 8.91 |
| 300 kHz | Edge | 14.2 | 0.99 | 17.1 |

x2.4 x1.9

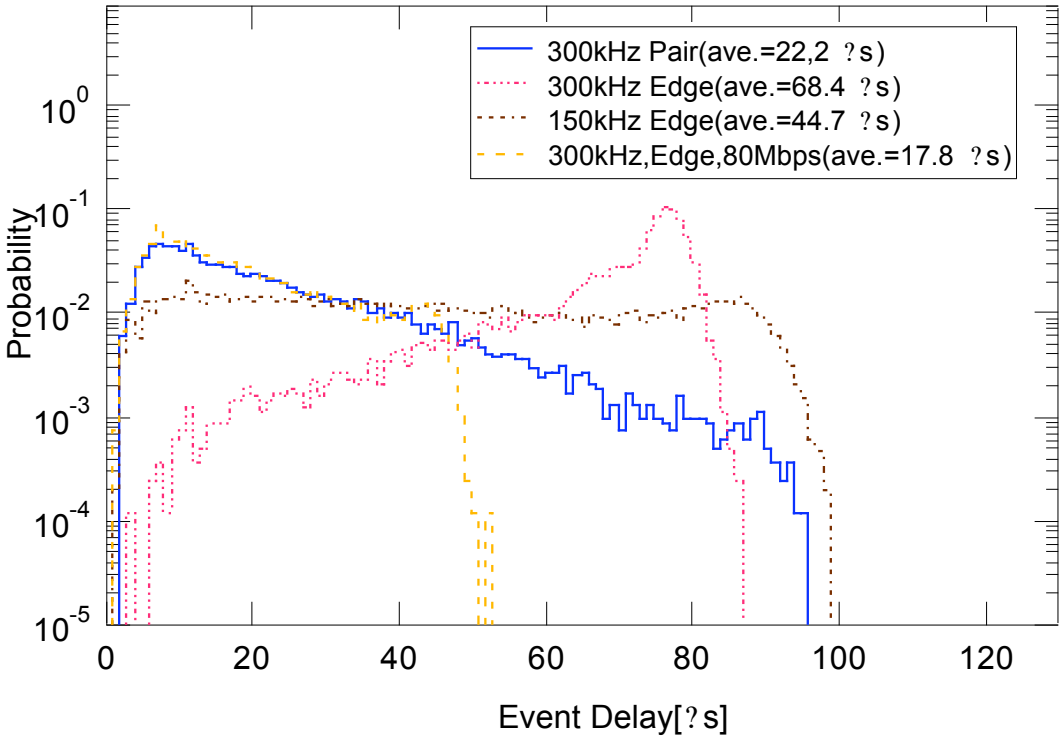
# L1 Buffer Occupancy




# Readout FIFO Occupancy

## Event Delay



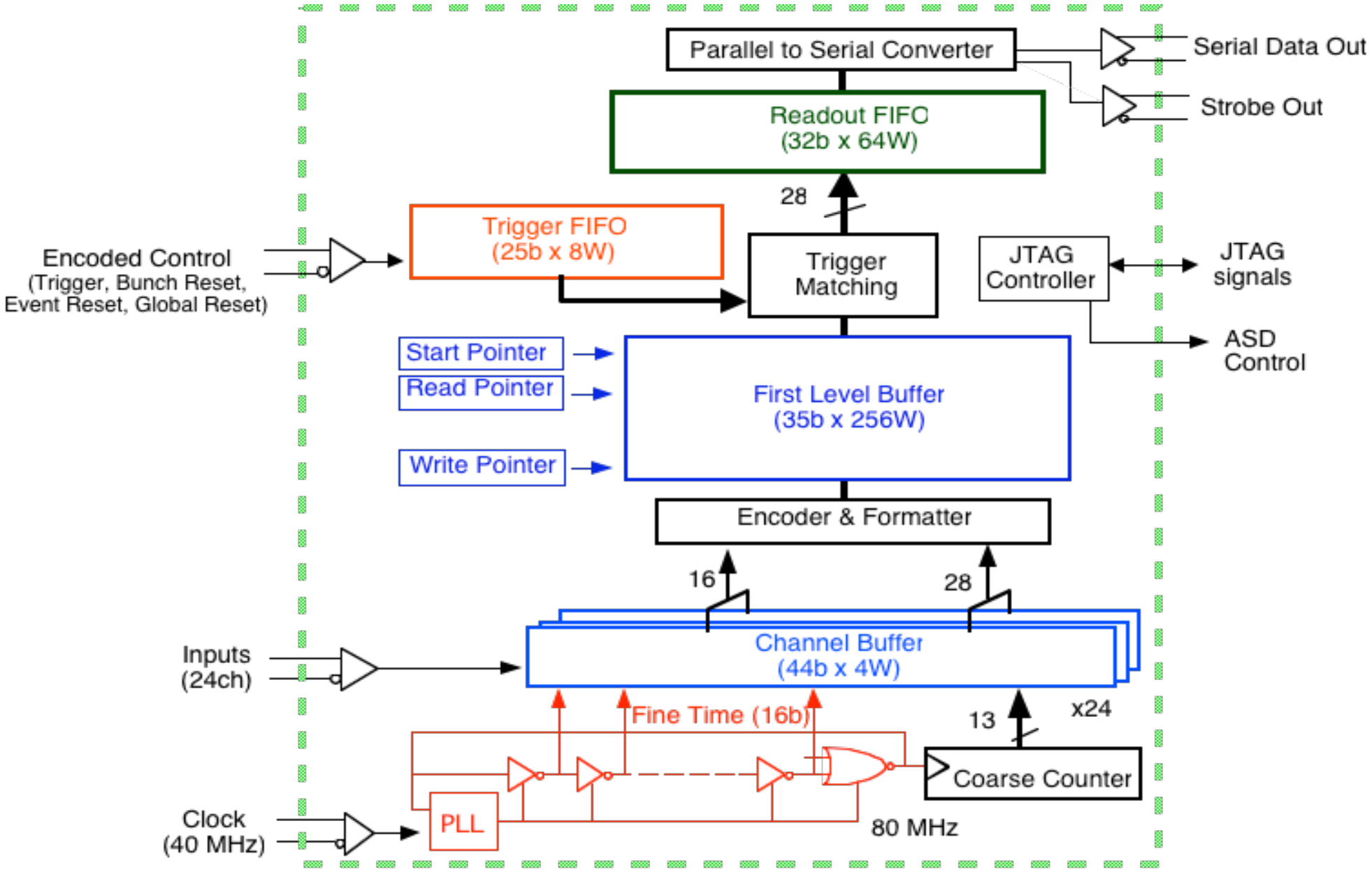

## Summary

| Hit Rate | Mode | Serial Speed | Data Loss | Max. Event Delay |
|---|---|---|---|---|
| 300 kHz | Pair(Leading+Width) | 40 Mbps | 0.36% | 95 μsec |
| 300 kHz | Edge(Leading & Trailing) | 40 Mbps | 41.9% | 87 μsec |
| 150 kHz | Edge(Leading & Trailing) | 40 Mbps | 6.4% | 98 μsec |
| 100 kHz | Edge(Leading & Trailing) | 40 Mbps | 0.19% | 108 μsec |
| 300 kHz | Edge(Leading & Trailing) | 80 Mbps | 2.3% | 53 μsec |

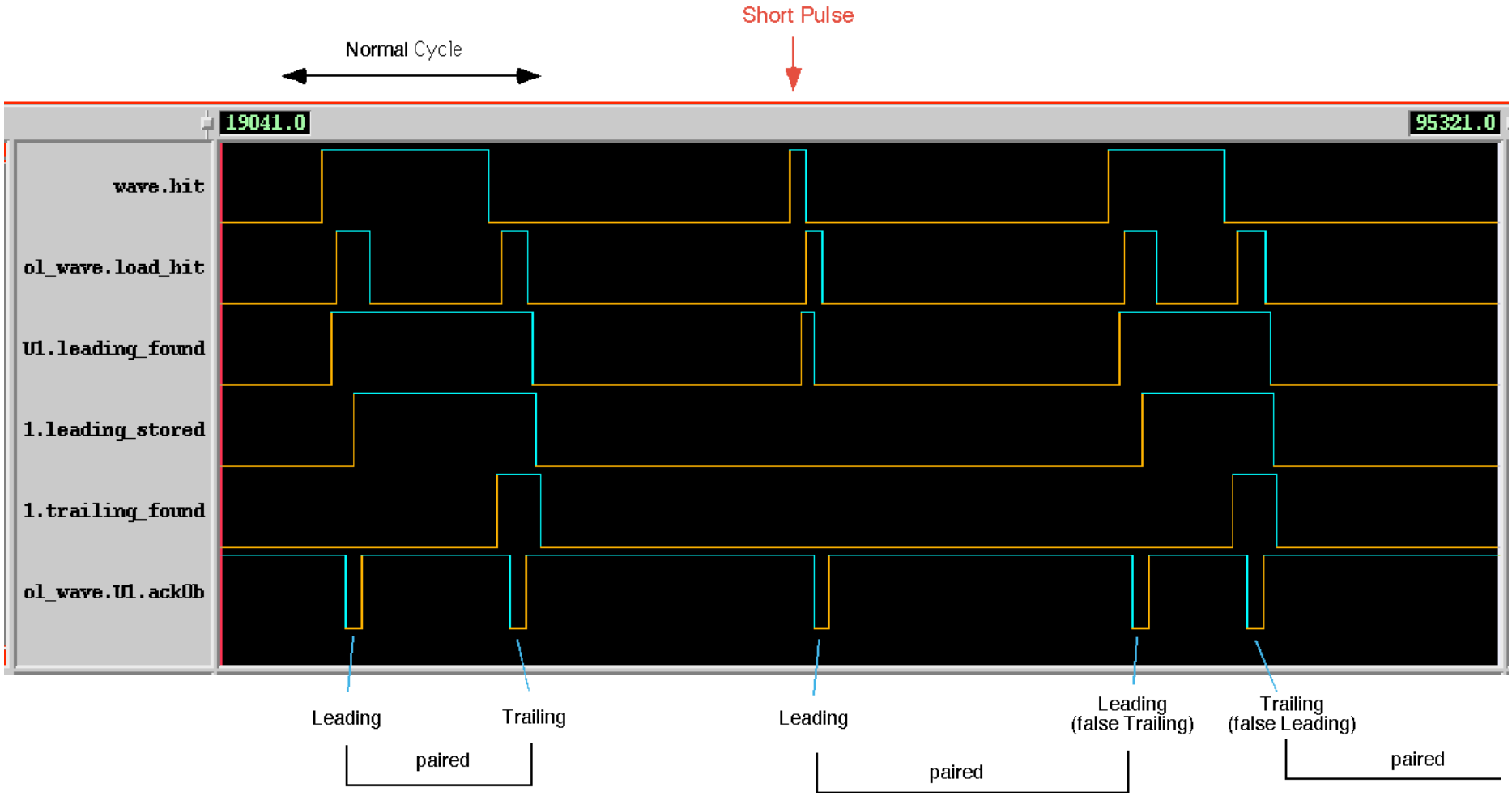
# Summary of Simulation

- Data loss is around 0.4% in Pair mode and Leading edge only mode at 300 kHz.
- Hit data size in Edge mode becomes 2.4 times larger than that in the Pair mode due to different matching window size.
- In Leading and Trailing edge mode, maximum hit rate should be less than 150 kHz to keep data loss in reasonable level.
- By increasing the serial readout speed to 80Mbps, maximum hit rate resumes near 300 kHz.
- Event delay is reduced to half in 80Mbps serial readout.
- Dropping mask word will reduce data size by 6% at 300 kHz hit rate.
- Reducing dead time to 300ns will increase data size by 14% at 300kHz hit rate.

End




Block Diagram of the AMT

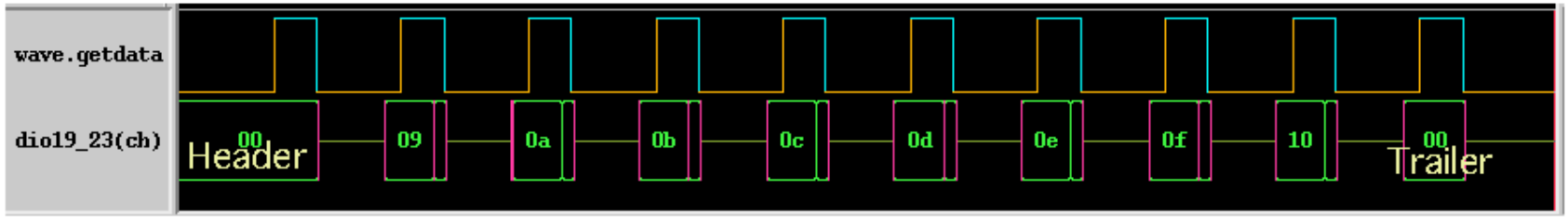

Short Pulse
Normal Cycle
19041.0
95321.0
wave.hit
ol_wave.load_hit
U1.leading_found
1.leading_stored
1.trailing_found
ol_wave.U1.ack0b
Leading
Trailing
paired
Leading
Leading
(false Trailing)
Trailing
(false Leading)
paired
paired

Emulated short pulse(ch0).
(leading and trailing edges are swapped, and has 82usec pulse width.)

Input signals

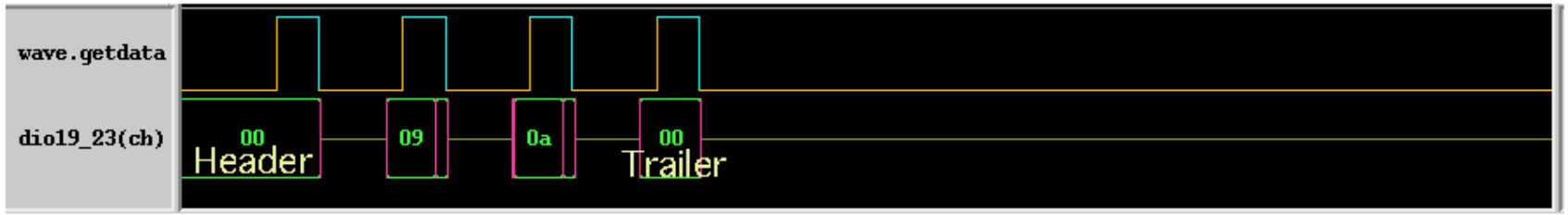
(actual ch0 signal)

Output when the short pulse does not exist.



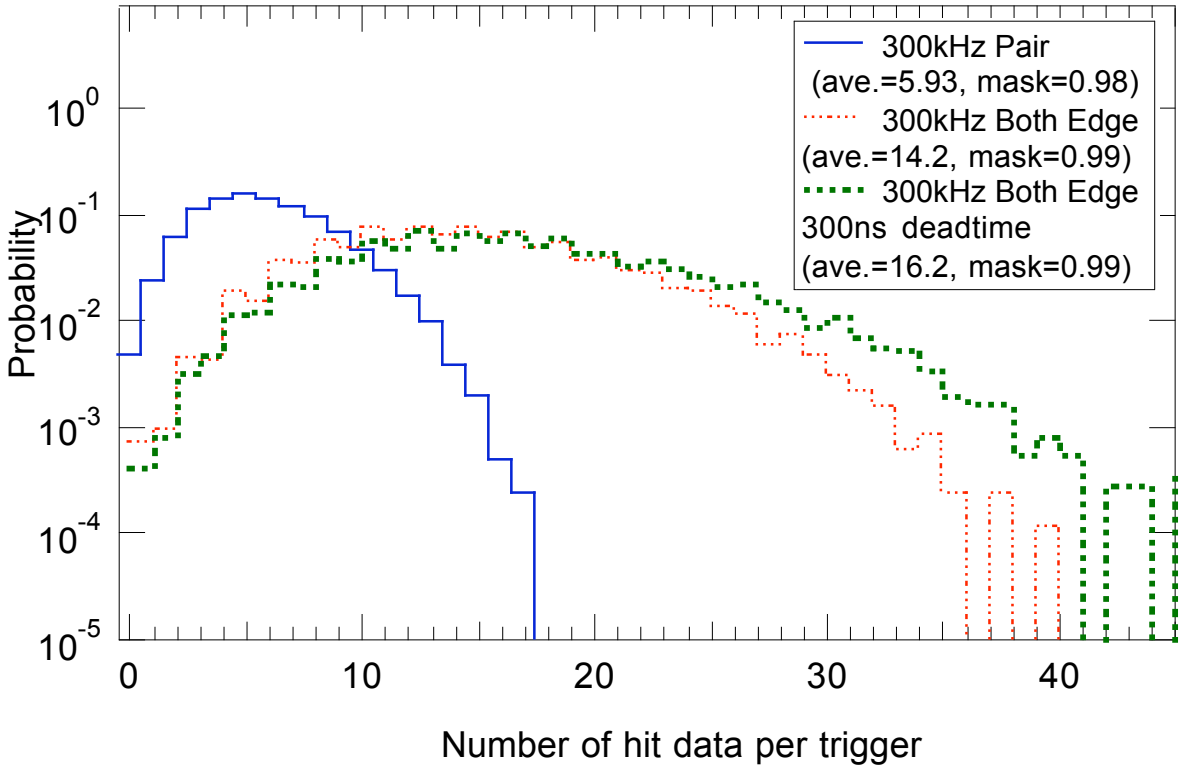

ch9 ~ ch16 data are selected and read out.

Output when the short pulse exists




ch9 and ch10 data are selected but ch11 ~ ch16 data are dropped since ch0 data stop processing of trigger matching circuit.
Thus we can reproduce the phenomena of mezzanine card dropout by a short pulse.

# 300ns Dead Time




15% (300kHz x 500ns) larger data size.