AMT Status

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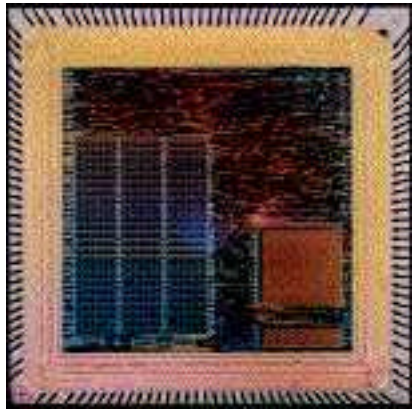
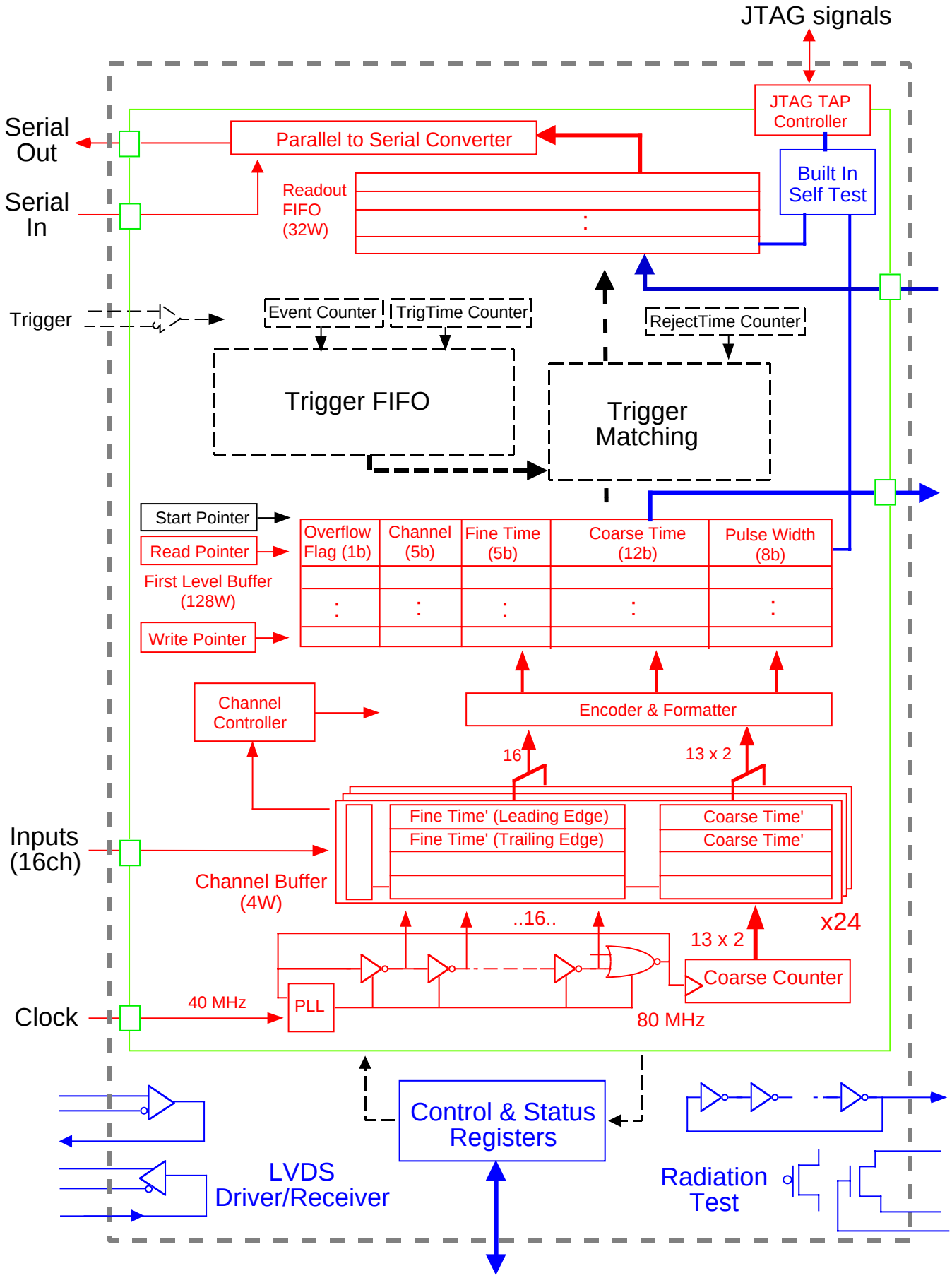
June 6, 1999
PC Elec@CERN

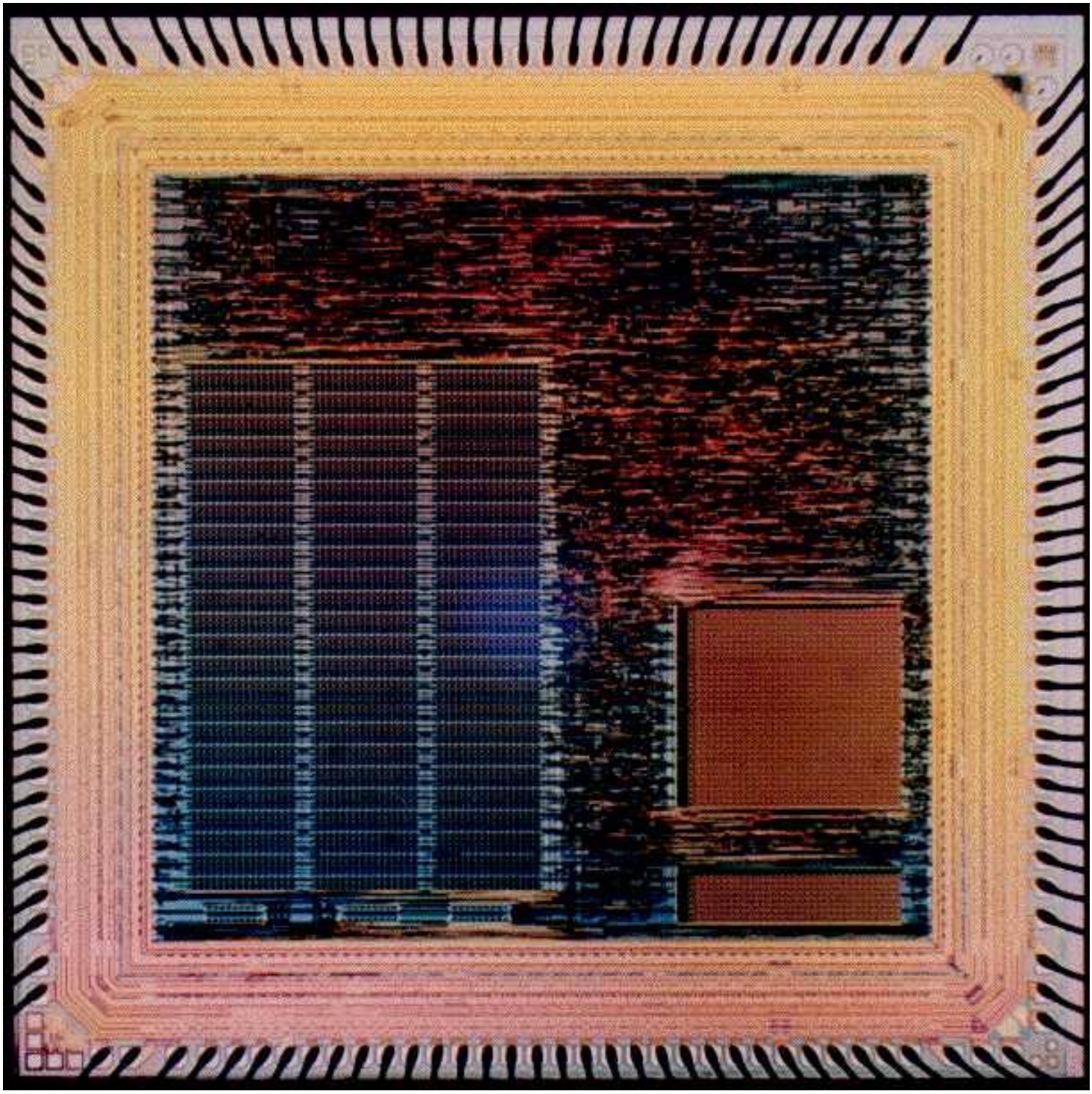
- AMT-TEG1 test
  - Previous measurements
  - New measurements
- AMT-1 schedule
- Summary





AMT-TEG1 Block Diagram

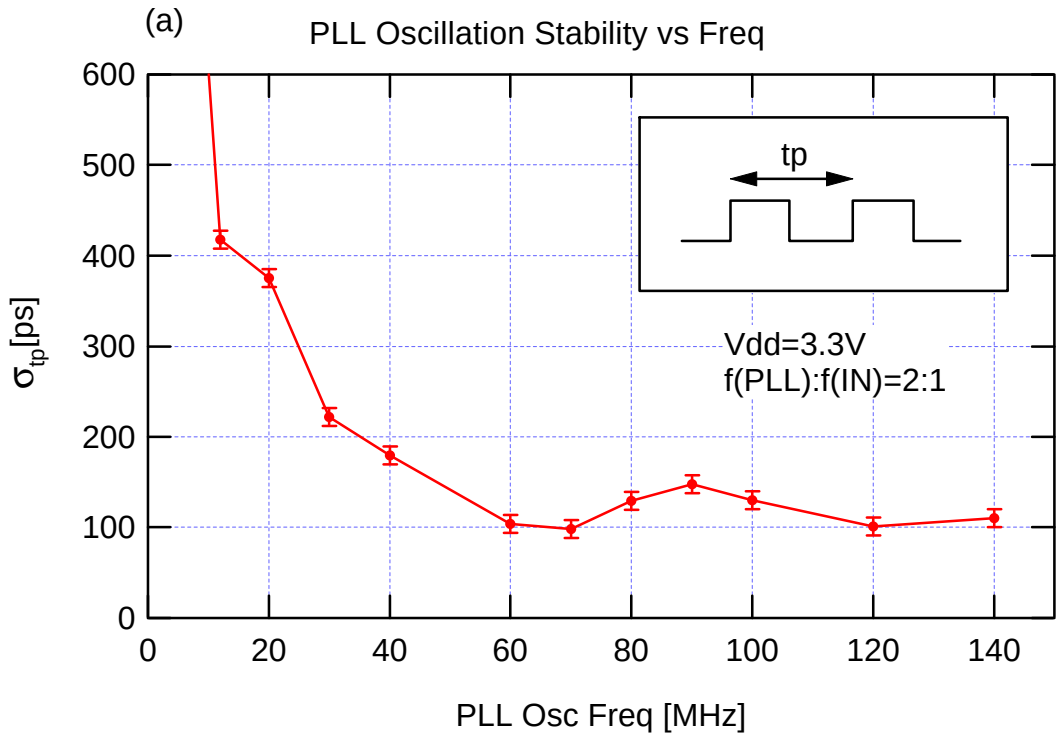
June 7, 1998, Y.Arai

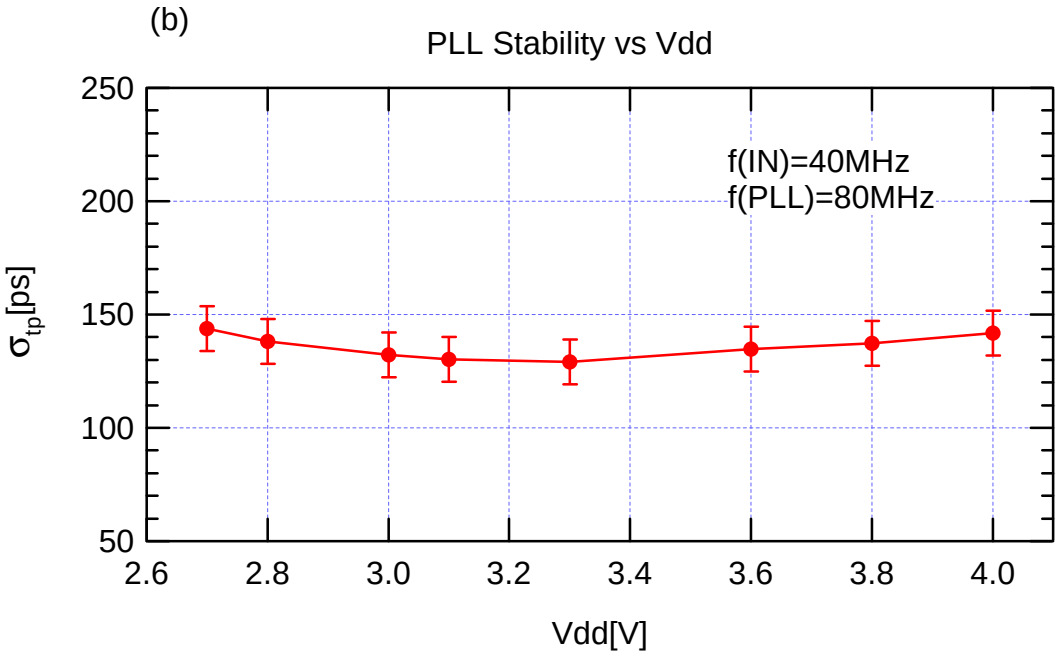


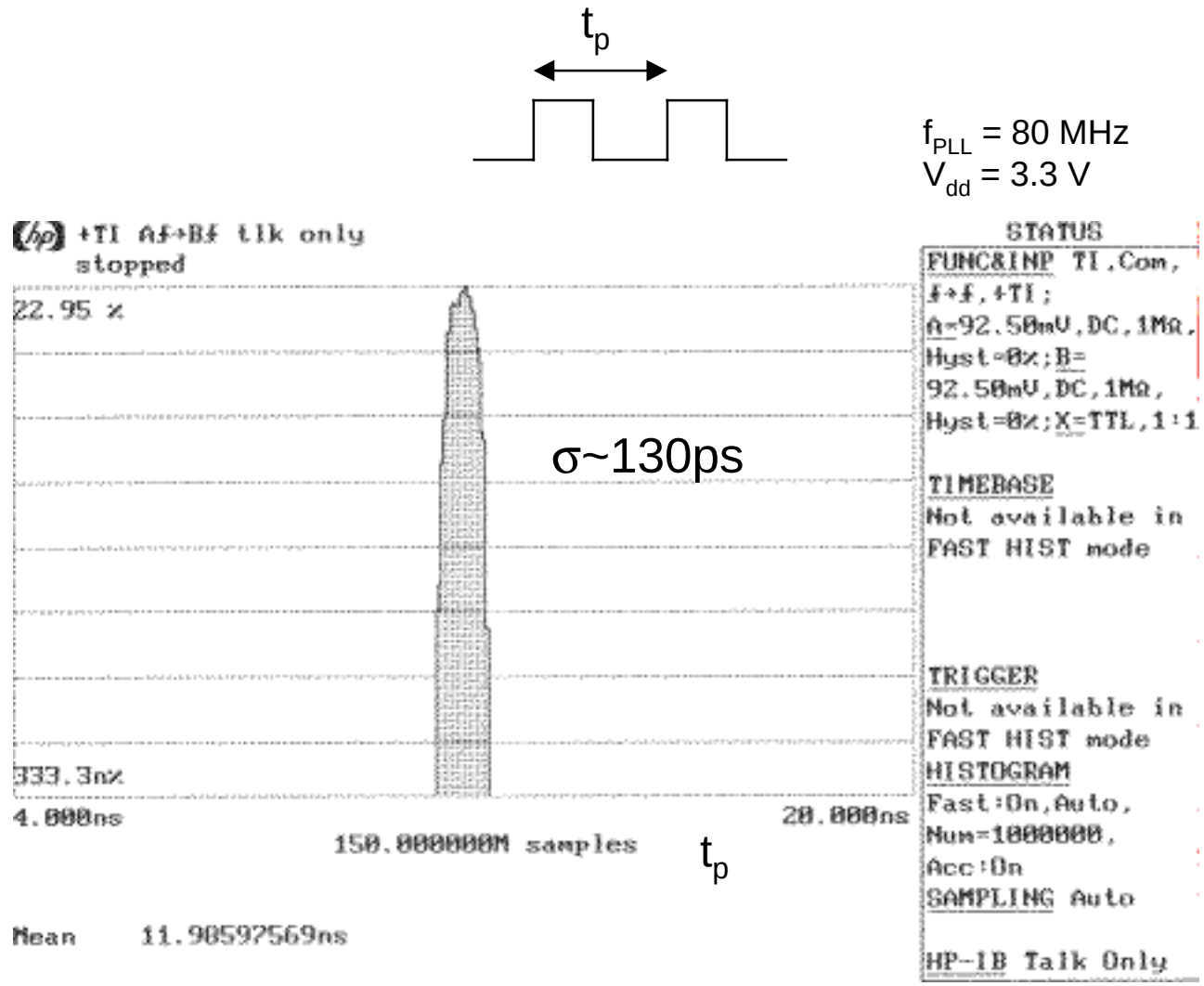
AMT-TEG1 test

- AMT-TEG1 is successfully designed in a 0.3 μm CMOS process.
- Reported measurements in previous meetings.

	measured value	operating point (target value)
PLL Operation	Freq = 40 ~ 120 MHz Vdd = 2.8 ~ 3.8V	80 MHz 3.3V
PLL Jitter	σ ~ 130 ps	< 200 ps
Coarse Time Counter	120 MHz	80 MHz
Radiation hardness for γ	50 krad	11 krad
Radiation hardness for n	to be measured (irradiated at April)	1.2×10^{13} n/cm^2

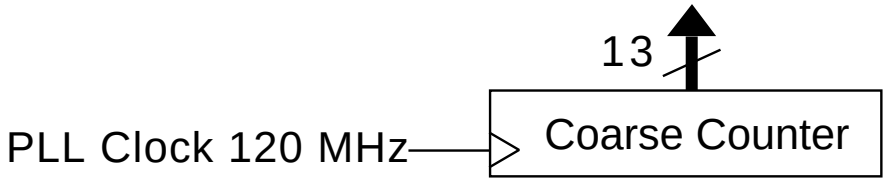

(a)
PLL Oscillation Stability vs Freq
600
500
400
300
200
100
0
0
20
40
60
80
100
120
140
σtpd[ps]
PLL Osc Freq [MHz]
tp
Vdd=3.3V
f(PLL):f(IN)=2:1

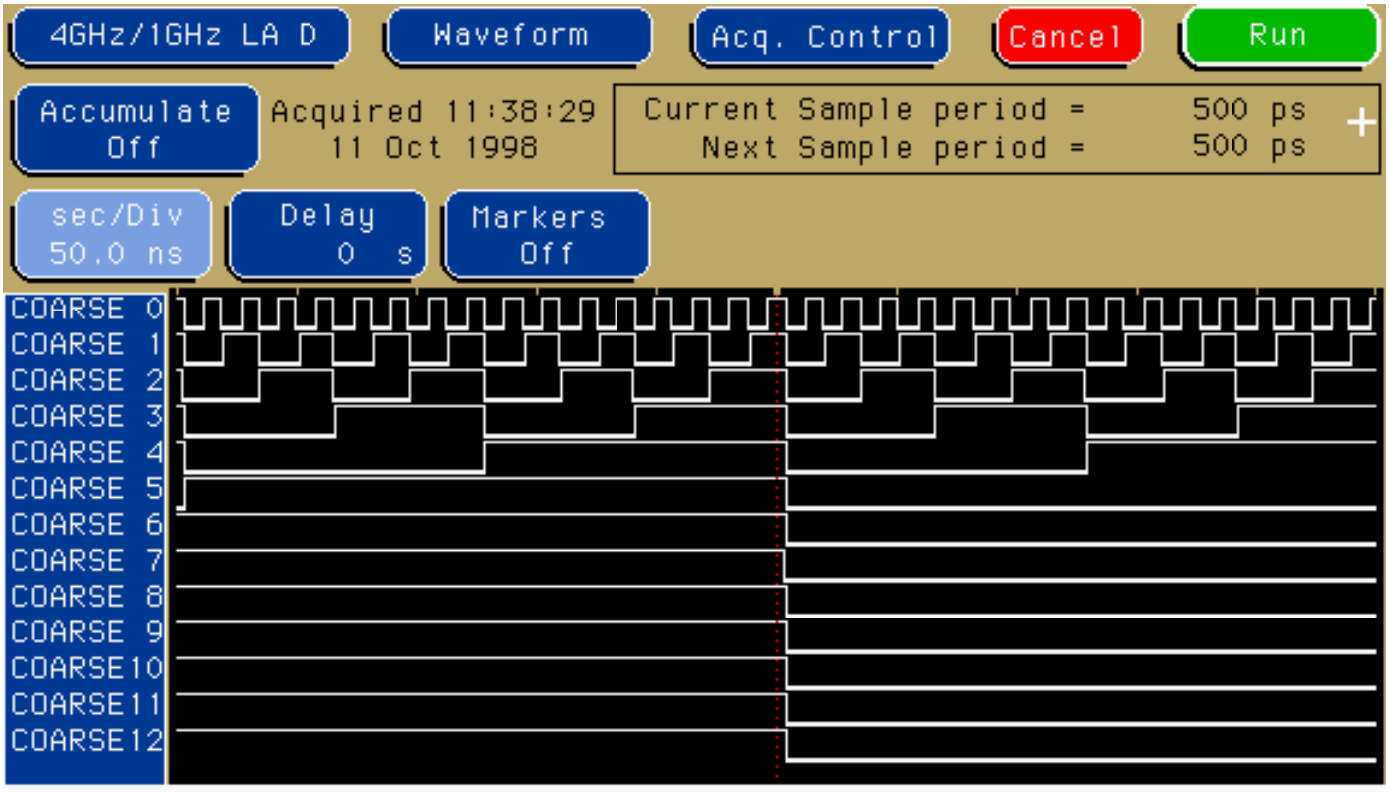

(b)
PLL Stability vs Vdd
250
200
150
100
50
2.6
2.8
3.0
3.2
3.4
3.6
3.8
4.0
σtpd[ps]
Vdd[V]
f(IN)=40MHz
f(PLL)=80MHz

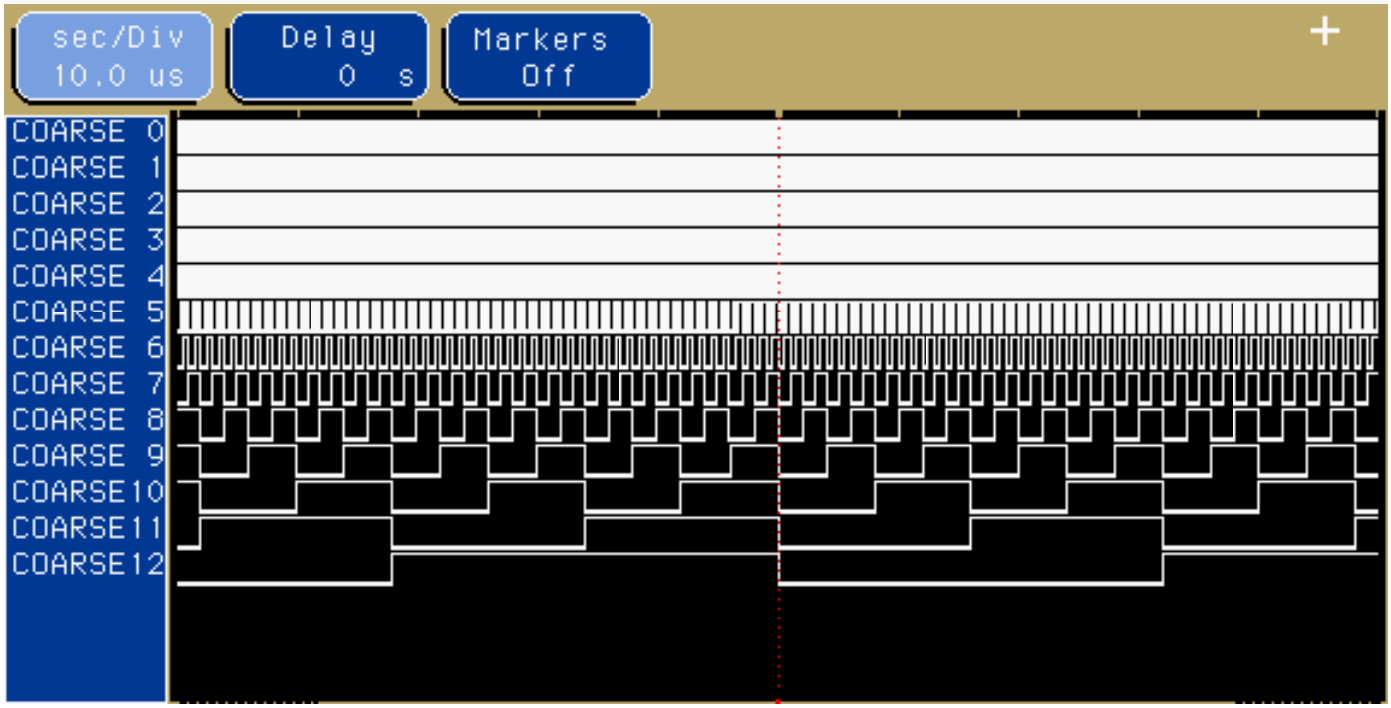


PLL Oscillation Jitter Histogram

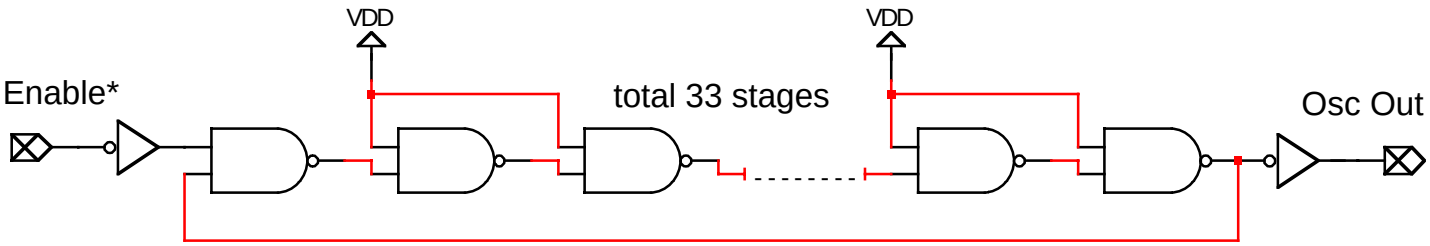
Coarse Time Counter

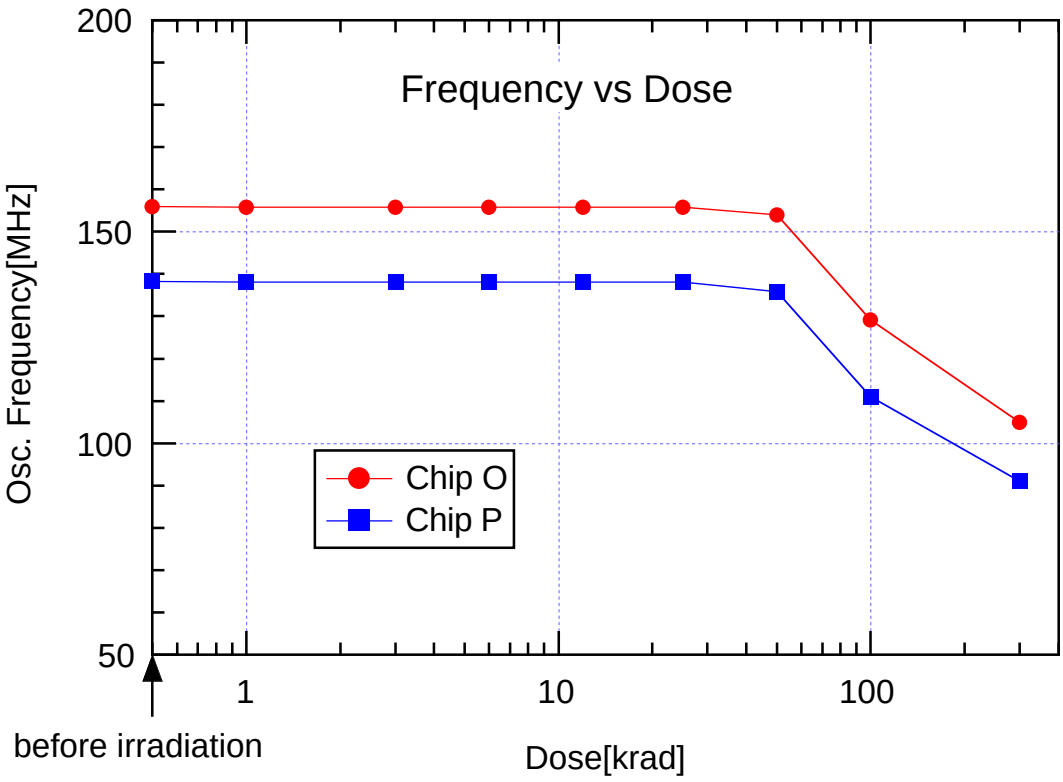


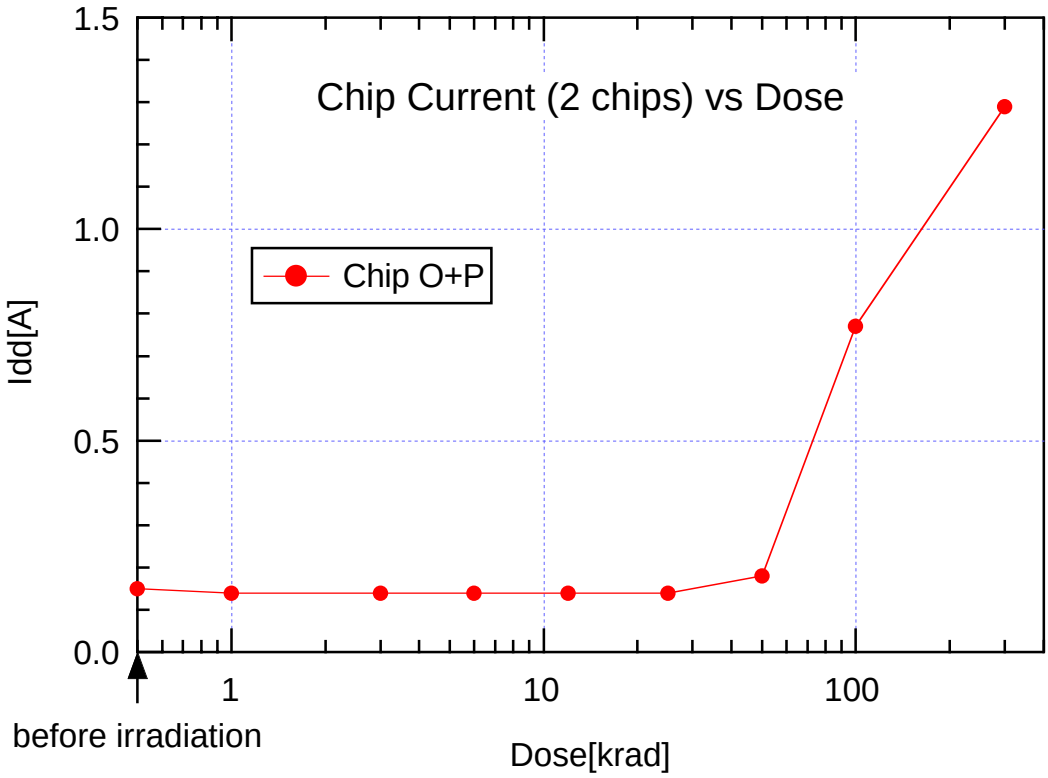




AMT-TEG1 Ring Oscillator







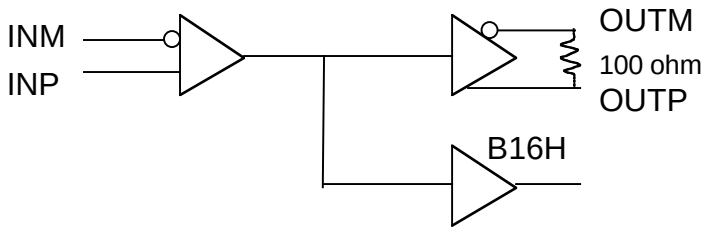
New Measurements

	measured value	operating point (target value)
LVDS receiver: ΔV Vcm	> 100 mV 0.2 ~ 2.2 V	> 100 mV 0.2 ~ 2.2V
LVDS driver (6.5m cable)	> 100 MHz	> 50MHz
Multiple edge resolution (double edge) (single edge)	 5 ns 9 ns	 30 ns 15 ns
L1B input speed	(2 + N) clocks	(4 + N) clocks
Time Resolution	305 ps RMS	< 500 ps RMS
Differential Nonlinearity	0.06 ns RMS	< 0.2 ns RMS
Integral Nonlinearity	0.07 ns RMS	< 0.2 ns RMS

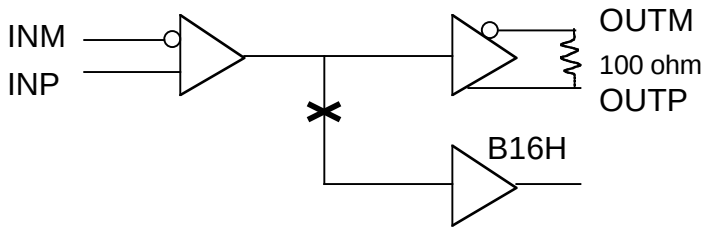
Apr. 15, 1999 Y.Arai (KEK)

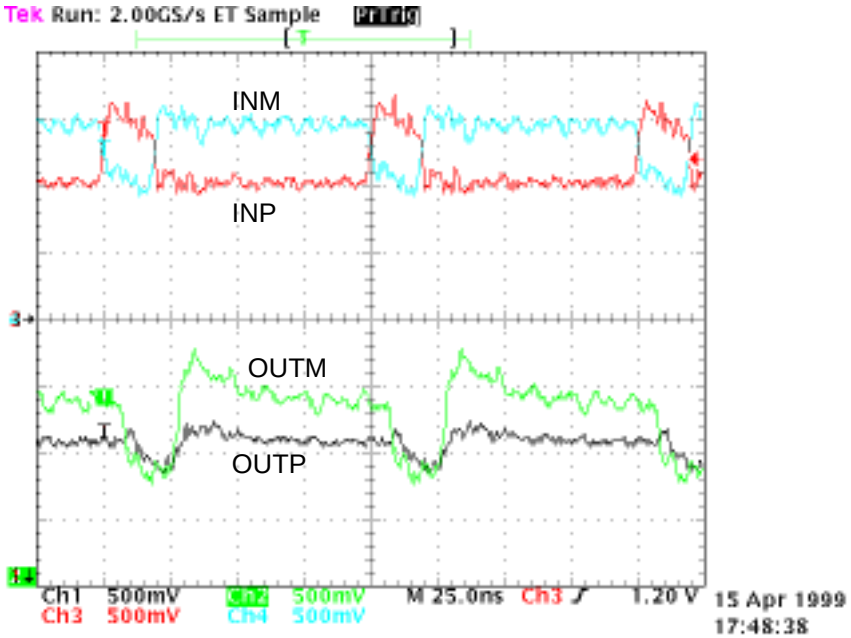
AMT-TEG1 LVDS Test

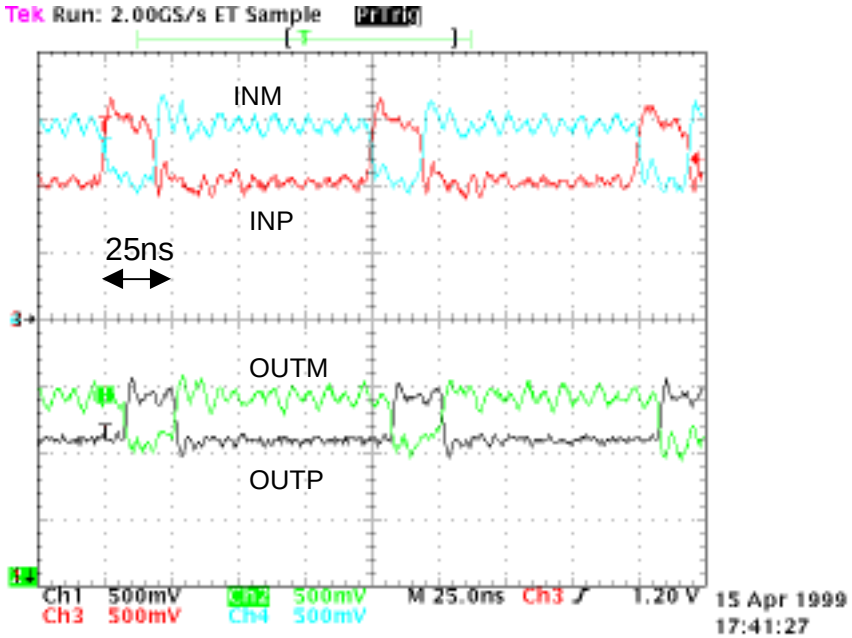
Chip0 (original)



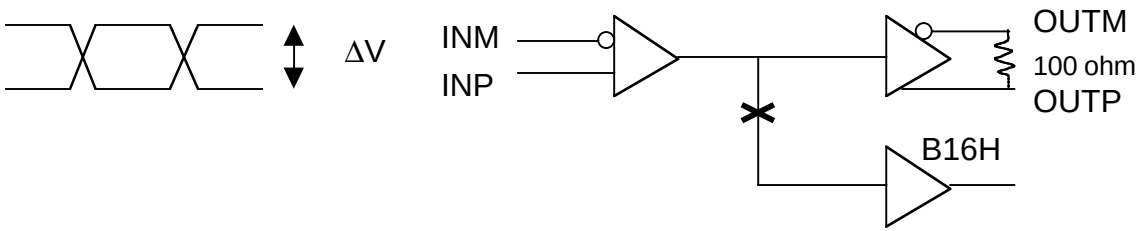
Chip1 (B16H cut)



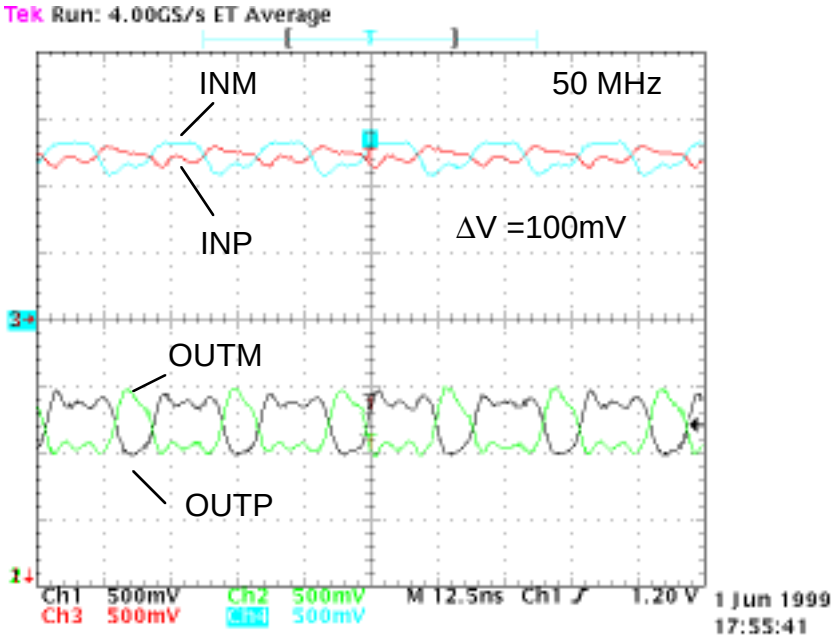




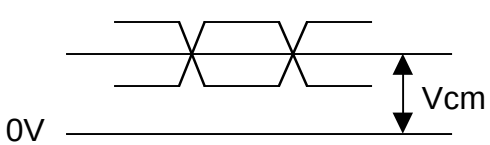
Receiver : Input Threshold (Vcm=1.2V)

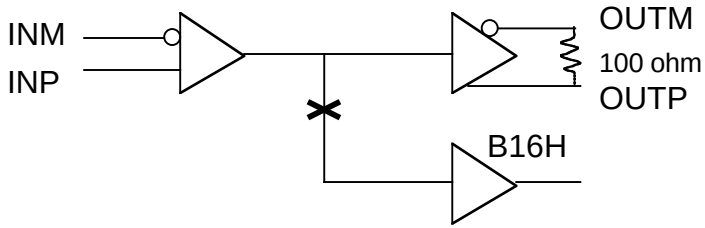


(IEEE 1596.3 spec : | ΔV | > 100 mV)

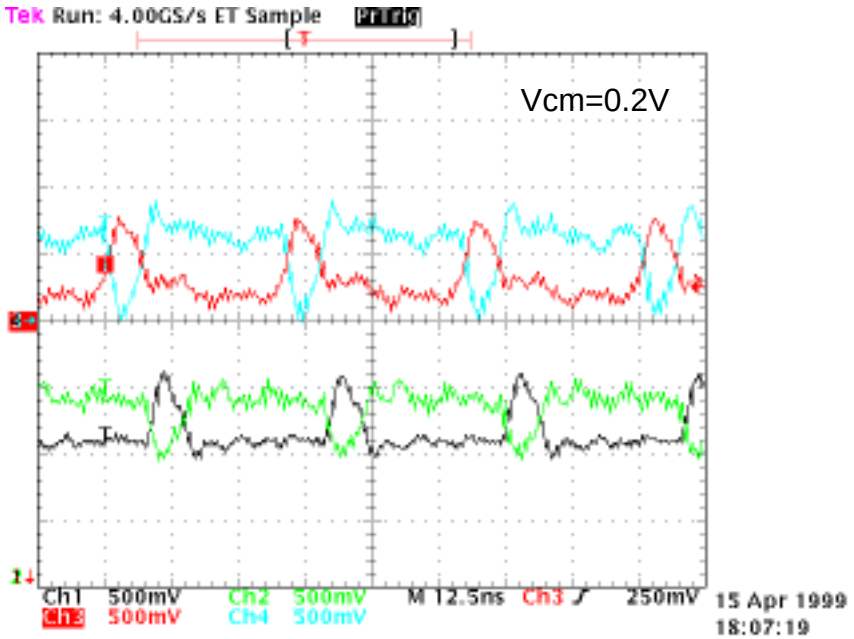


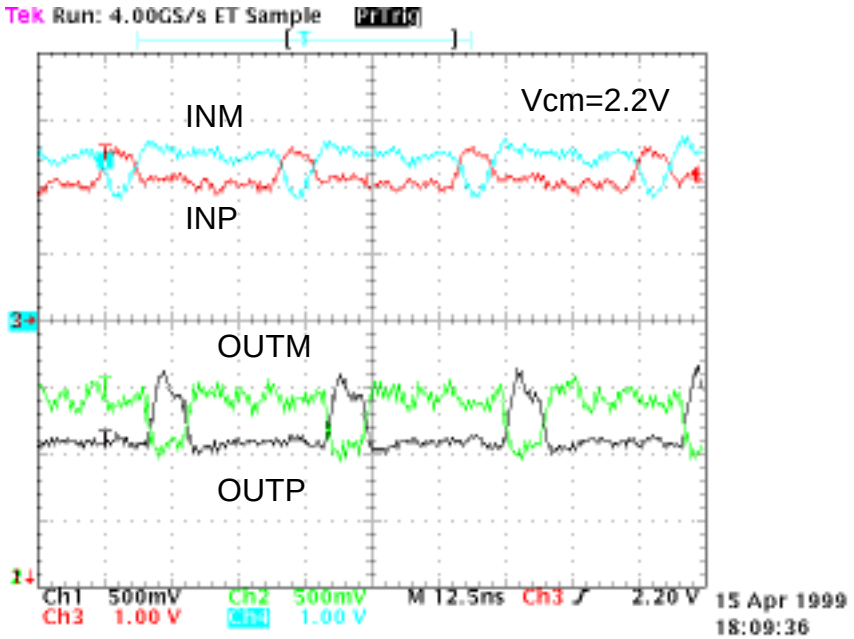
Central Voltage Dependence (Vid=400mV)



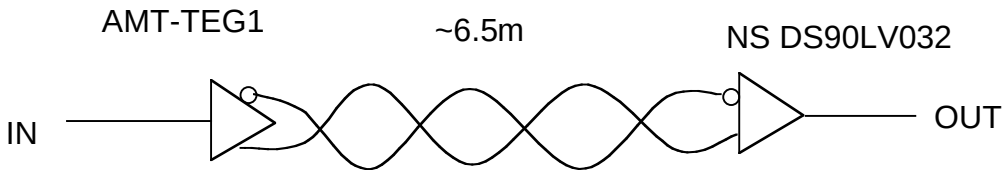


(IEEE 1596.3 spec : 0.2V < Vcm < 2.2V)



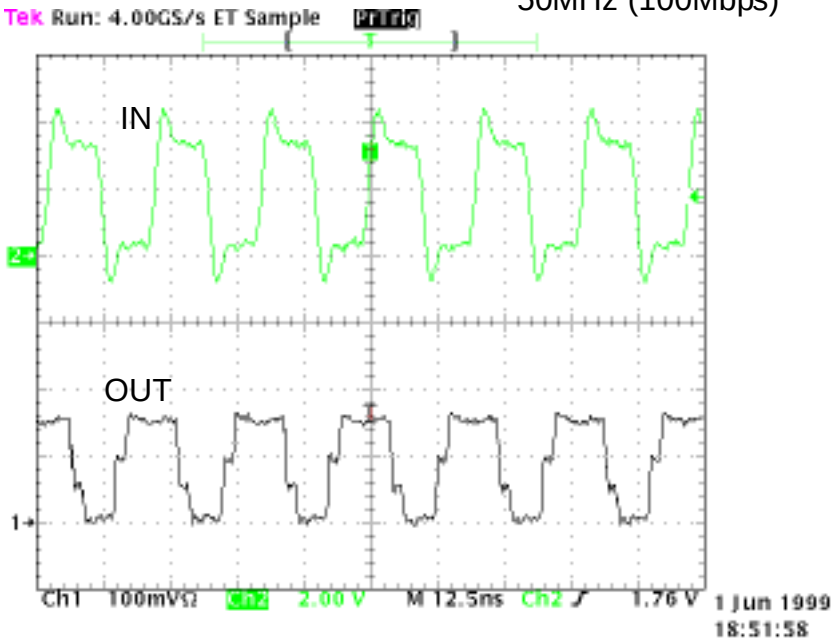


Long Cable Drive

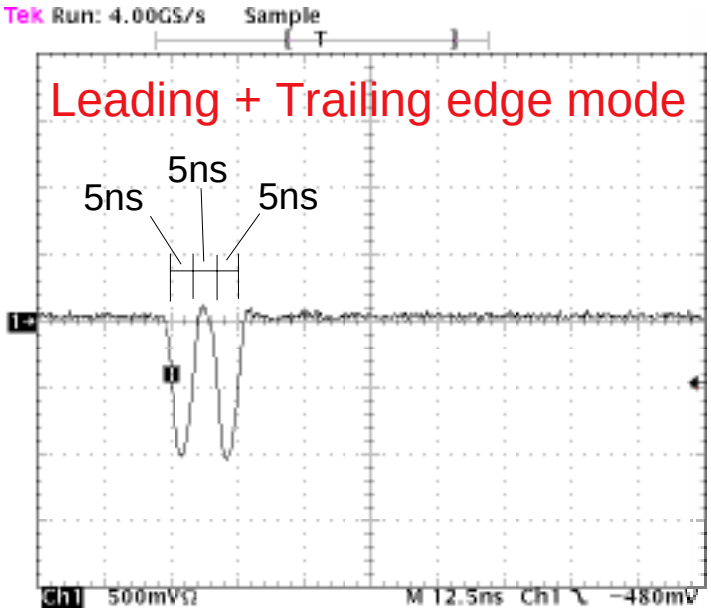


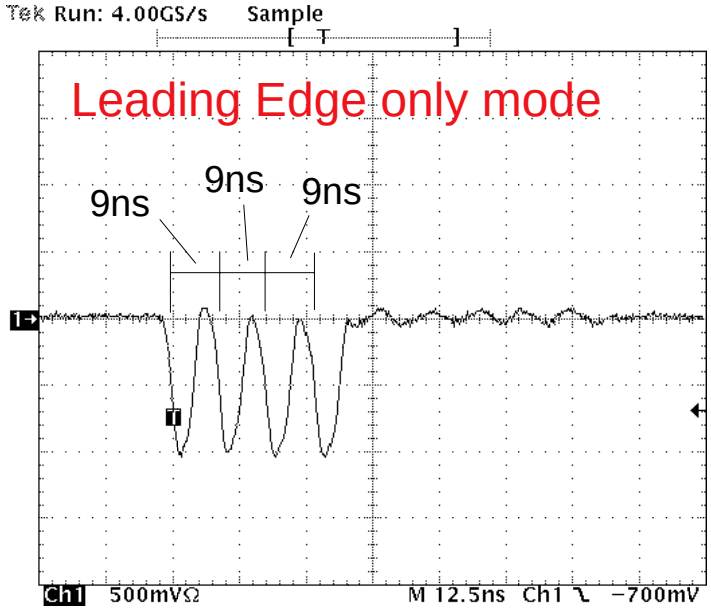
Maximum Frequency > 100MHz

50MHz (100Mbps)

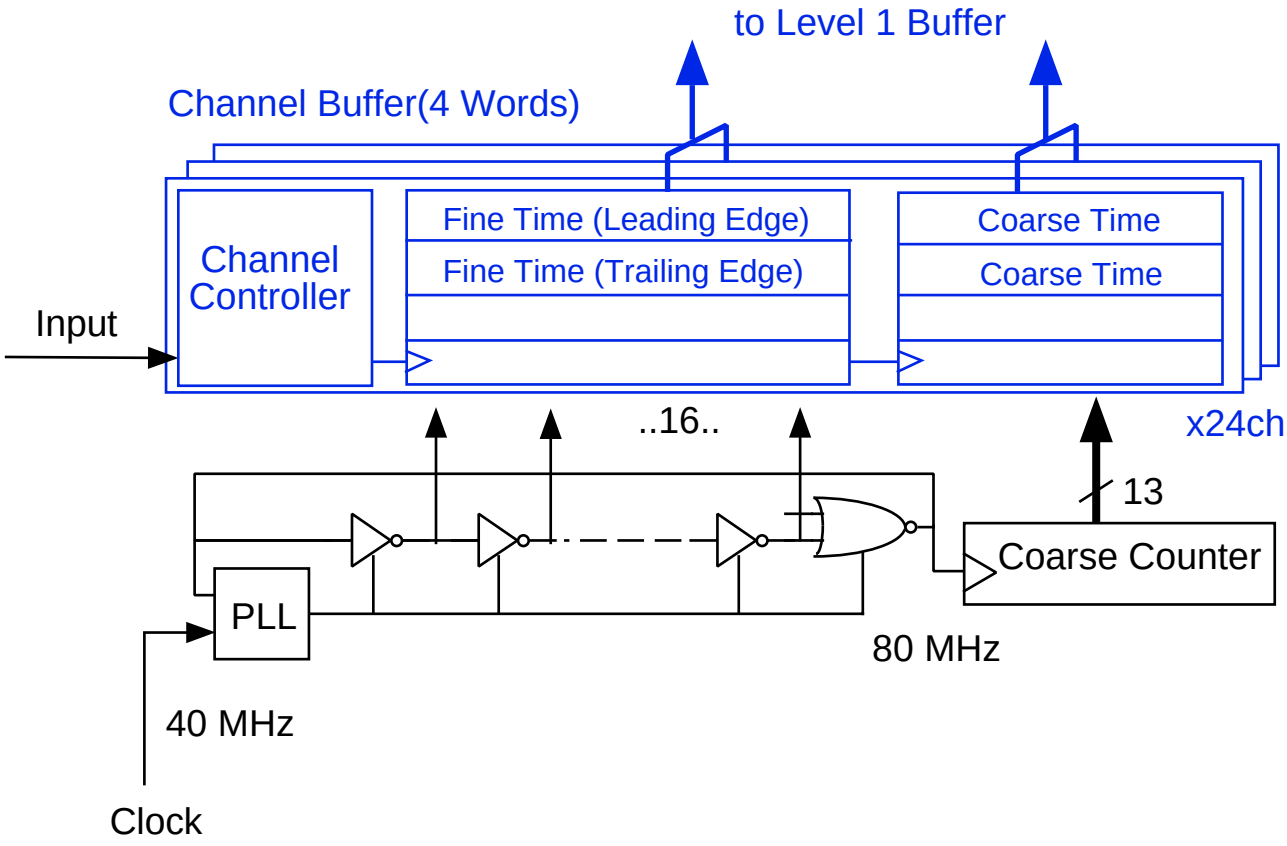


Channel Buffer Speed

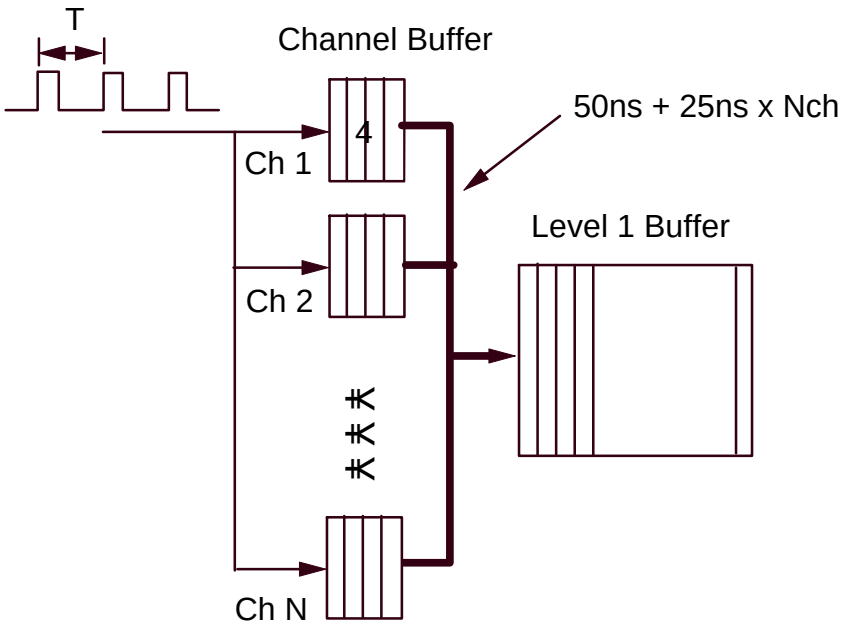


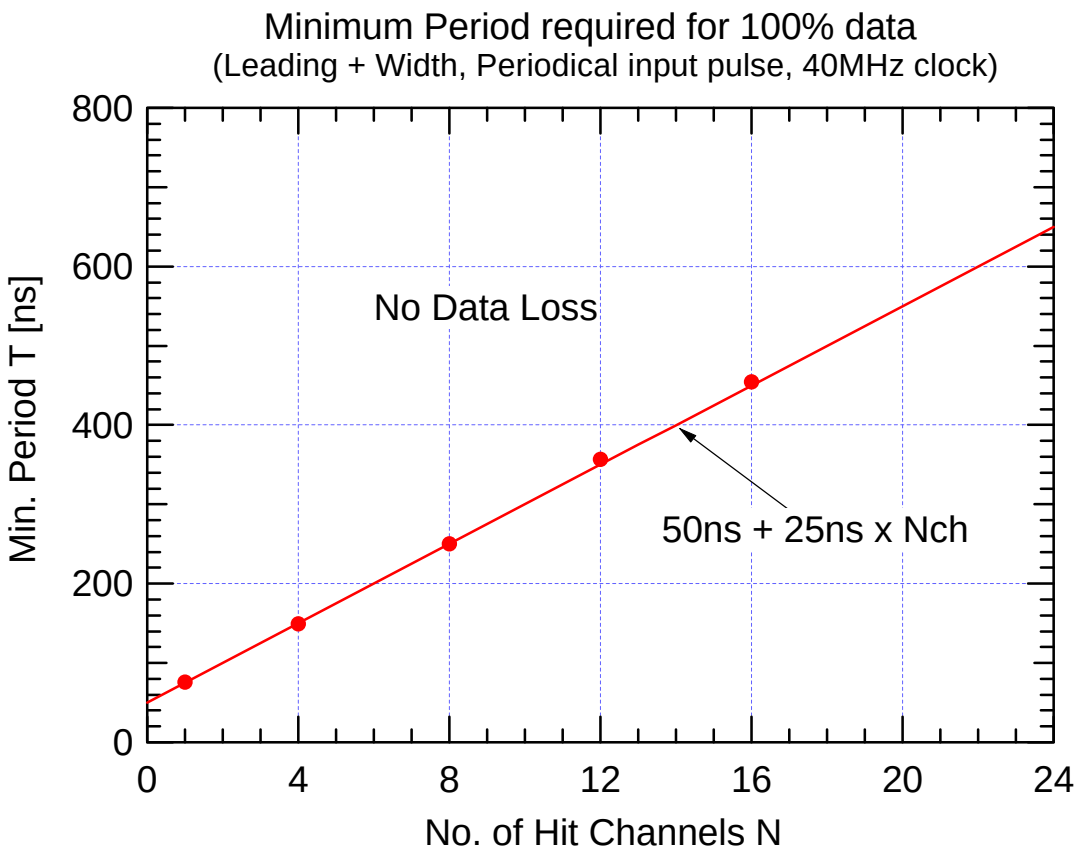


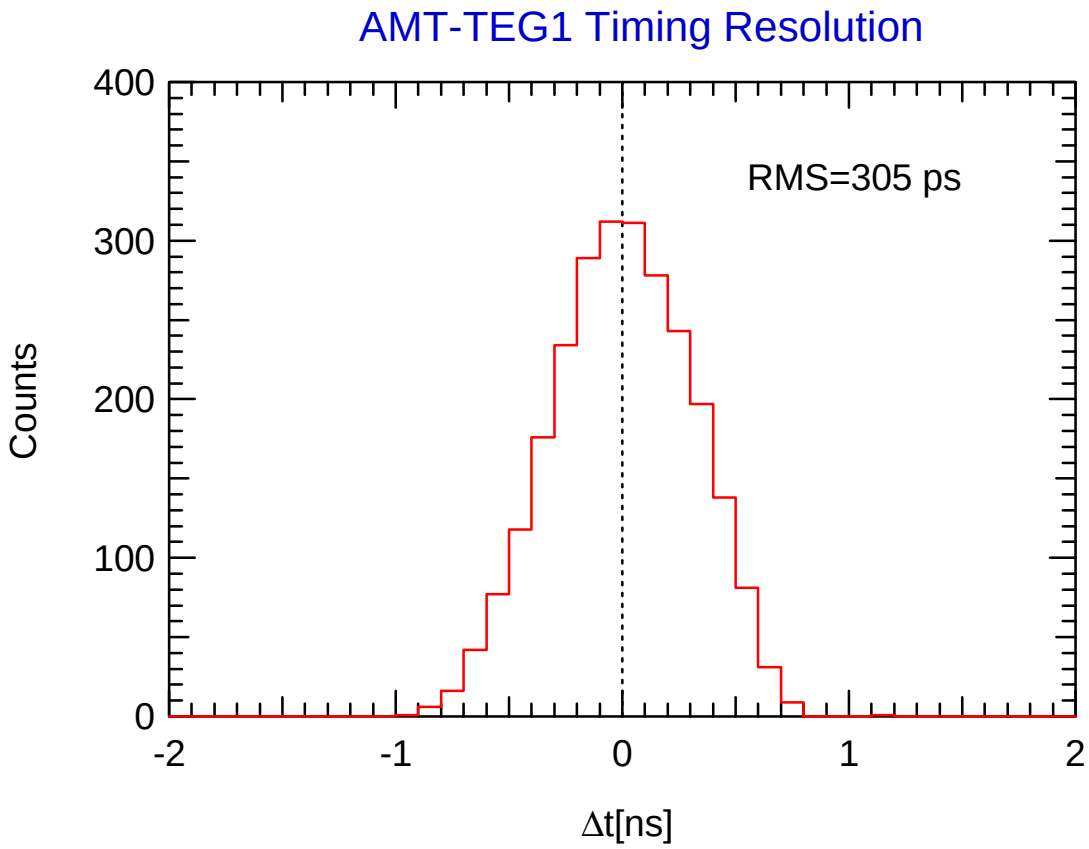
Multiple Edge Resolution = 5 ns (Double Edge)
= 9 ns (Single Edge)



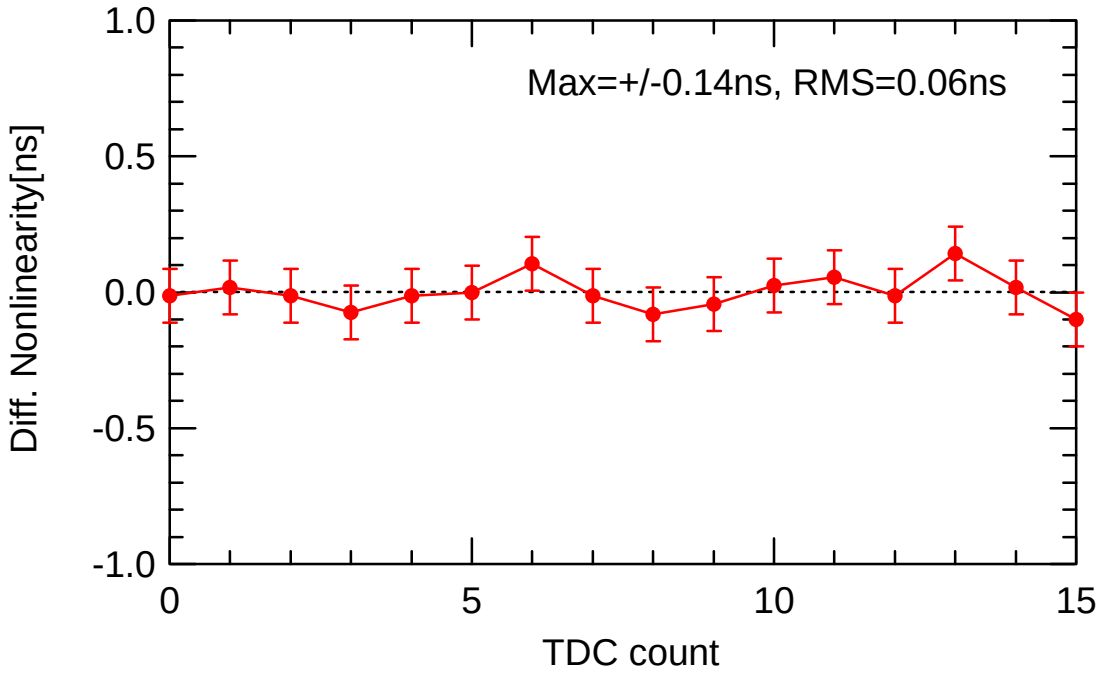
Data Transfer Rate to L1 Buffer



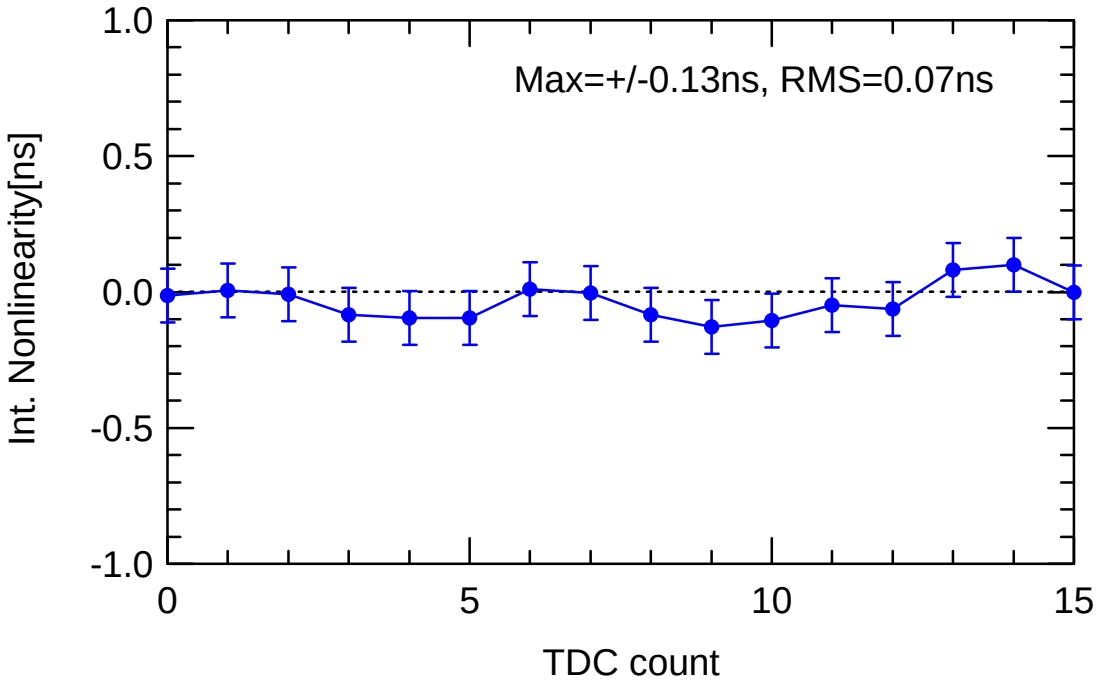



AMT-TEG1 Timing Resolution
RMS=305 ps
Counts
400
300
200
100
0
-2
-1
0
1
2
Δt[ns]

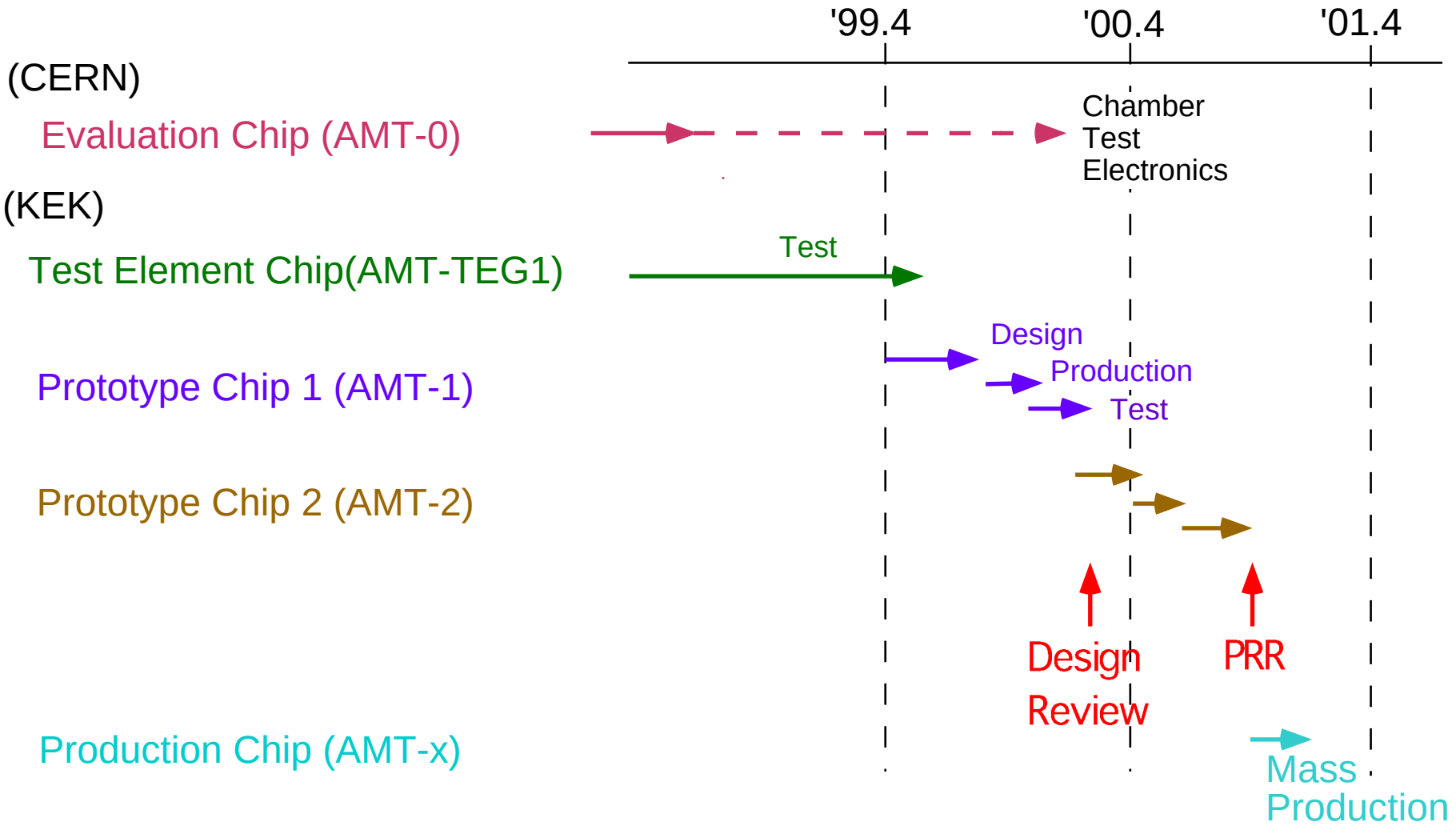
AMT-TEG1 Differential Nonlinearity



AMT-TEG1 Integral Nonlinearity



AMT Schedule



Summary

- ❏ Fundamental performance for the AMT was tested and found to fulfil the requirements.
- ❏ Neutron irradiation of the chip was done, and measurements will be done soon..
- ❏ AMT-1 design will be finished around this summer.