

-ray Irradiation Test of AMT-TEG1

Yasuo Arai *KEK, yasuo.arai@kek.jp*

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Introduction

- AMT-TEG1 chip was developed and fabricated last autumn. Main purpose of this chip is evaluating basic TDC elements (PLL, LVDS, JTAG ...).
- Many parts are designed from Verilog source codes which are imported from AMT-0 (Jorgen's design).
- AMT-TEG1 is processed in a new 0.3 µm CMOS process (Toshiba TC220G gate array).
- Basic circuit elements were tested successfully.
- The chip contains a Ring Oscillator and NMOS and PMOS transistors for radiation test.

Test Condition

- Irradiated chip : AMT-TEG1(Toshiba 0.3 µm CMOS).
- Source : ⁶⁰Co (~90 rad(Si)/sec, Total dose ~ 100 krad(Si))
- Follow MIL-STD-883 method 1019.4. After the irradiation, 100 ° C, 1 week annealing was done.
- Transistors were biased in worst condition during irradiation.



Worst Bias(P short, N On)

- ATLAS requirement : 1.1 krad/year (@MDT Endcap, Safety factor=4).
- Test transistors are directly connected to pins without protection diodes. We handled the chip with the greatest care, but some transistors were broken during the test.

AMT-TEG1 Ring Oscillator







Gm Variation (Vds=3V, Vgs=3V, Vsub=0V)



Threshold Variation



Drain Leak Current (Vds=3V, Vgs=0V, Vsub=0V)

Summary

- □ Gamma-ray irradiation was done for the AMT-TEG1 (0.3µm CMOS).
- □ Ring Oscillator shows no performance degradation up to 50 krad.
- \Box No visible change in G_m up tp 100 krad.
- Threshold shift (Vth) is less than 200mV at100 krad. However, there is no systematic tendency, so this might be caused mainly by ill-handling of the transistor.
- NMOS drain leak current starts increasing above 25 krad: Id < 2x10⁻⁶ A @100krad. There is no leak current increase in PMOS. (Current increase for 100 k gates ~100 mA @100krad)
- ❑ Conclusion: The 0.3 µm process has enough -radiation torelance for the ATLAS MDT.
- □ Neutron iradiation test will be scheduled.
- □ AMT-TEG2 design will be finished before the summer.