Radiation Qualification of Electronics Components Used for the ATLAS Level-1 Muon Endcap Trigger System

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***Abstract*—The ATLAS level-1 muon endcap trigger system is divided into three parts; one off-detector part and two on-detector parts. Application specific ICs (ASICs) and anti-fuse Field Programmable Gate Array (FPGAs) are actively used in the on-detector parts. A Low-Voltage Data Signaling (LVDS) serial link is used for the data transfer between the two on-detector parts (15 m apart) and G-Link (Hewlett-Packard 1.4 Gbaud high speed data link) with optical transmission (90 m) is used from one of the on-detector parts to the off-detector part. These components will be exposed to a radiation of approximately 200 Gy (including safety factors) for ten years corresponding to a total ionizing dose (TID) and a hadron fluence of $2\times10^{10}\ \mathrm{hadrons/cm^2}$. We have investigated systematically the radiation susceptibility to both the total ionizing dose and the single event effects for ASIC, FPGA, and Commercial Off The Shelf (COTS) serializer and deserializer chipsets for two types of LVDS serial link and one G-Link type. In this documentation we report the result of the irradiation tests for these devices and discuss their validity in the ATLAS system.**

***Index Terms*—Application specific integrated circuits, optical fiber radiation effects, semiconductor device radiation effects.**

I. Introduction

THREE types of ASICs are extensively used in the core part of the ATLAS level-1 muon endcap trigger system [1]. FPGA chips are also used for ancillary logics. The ASIC and FPGA chips are mounted on boards, which are just behind the endcap muon chamber discs (which consists of seven layers of Thin Gap Chambers (TGC) used to identify a muon with $\mathrm{p_T} > 6\ \mathrm{GeV/c}$ in the ATLAS endcap region) and the outer rim of a disc.

LVDS links are used for data transfer between the two on-detector parts (15 m) using category-6 shielded twisted pair (STP) cables. G-Link optical transmission lines are used from the on-detector part to the off-detector part over a distance of 90 m. Overall, we use about 1000 G-Link and 10 000 LVDS link lines in the ATLAS level-1 muon endcap trigger system. As both links are serial transmission, we need a serializer at the transmitter and a deserializer at the receiver side.

The on-detector parts will be exposed to the estimated radiation of 3 Gy resulting in a total ionizing dose and a hadron fluence of $2\times10^{10}\ \mathrm{hadrons/cm^2}$ after ten year of normal ATLAS operation [2]. According to the ATLAS internal rules for the radiation hardness issues, we have to demonstrate that all electronics components used in the on-detector part must work up to approximately 200 Gy total ionizing dose (TID), which is product of an actual dose simulated of 3 Gy times an overall safety factor of 70. We have to assume that the single event effect (SEE) rate for a component will be five (a safety factor) times more than σ_{SEE} (SEE cross section for the particular component) times the hadron fluence. We have carried out the irradiation tests using γ-rays from a $^{60}\mathrm{Co}$ for the TID measurements and a 70 MeV proton beam to derive σ_{SEE}. In the LHC environment, SEE will be induced mainly by secondarily produced low energy heavy ions or neutrons (<20 MeV) in hadronic interactions with materials constituting the integrated circuits. Thus the estimation of SEE cross sections using low energy protons will be reasonable to predict actual SEE rates of electronics in the ATLAS environment. We have made the SEE test using proton beam of slightly higher energy (70 MeV) than usual one of secondary hadrons (20 MeV). The SEE test with high energy proton enables us to estimate cross sections of more serious (destructive) SEEs.

We intend to use 0.35 μm standard CMOS technology of ROHM [3] for ASIC fabrication and Actel [4] anti-fuse based FPGA chips. For the LVDS data transfer, we have selected two COTS serializer and deserializer chipsets [one from Texas Instruments (TI) [5] and one from National Semiconductor (NS) [6]]. For the G-Link, we have uniquely selected one Agilent [7] chipset and an optical transceiver by Infineon [8].

In the following section, we discuss the setup and procedure of the radiation test for both TID and SEE level measurements. In Section III we list the results of the measurements. We discuss the characteristic similarities and differences for the irradiation of CMOS and the Actel anti-fuse FPGA chips and two candidates of the LVDS serializer and deserializer chipsets in detail. Finally in Section IV we give summaries of the results and conclusion.

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II. Radiation Test Setup and Procedure

To estimate the TID tolerance we have used the γ-ray irradiation facility of Research Center for Nuclear Science and Technology (RCNST) of University of Tokyo. To obtain σ_{SEE} we have used the proton irradiation facility of Cyclotron and Radio Isotope Center (CYRIC) of Tohoku University.

A. Facility and Procedure for TID Measurement

The γ-ray irradiation facility of RCNST is a two-story structure; an irradiation room on the downstairs and a storage for sources upstairs. 48 pencil type rods as radiation sources are filled in a cylindrical vessel, which moves between the upstairs and the downstairs levels via a remote control system. The maximum strength of the sources and the maximum dose rate are 22 TBq and 1000 Gy/hr in $\mathrm{H_2O}$, respectively. The irradiation rate can be controlled by changing the radiation source and the location of the Device Under Test (we call hereafter a target chip as DUT). We used $^{60}\mathrm{Co}$ as the source and the irradiation rate was set to 500 Gy/hr. As this irradiation facility is widely being used, the dose rate is periodically calibrated using a Fricke Radiation Meter. The irradiation and the annealing were done at room temperature, approximately 25 °C. During the irradiation and the annealing, DUTs were biased without clock and the current was monitored. The functionality was checked before and after the irradiation and the annealing. We intended to inject γ-rays vertically into a DUT, but the injected angle would be widely distributed due to the geometrical constraint of the experimental setup. We have not put any filters to sharpen the γ-ray flux in front of a DUT.

B. Facility and Procedure for SEE Measurement

From the cyclotron, 70 MeV proton beam was extracted through a Ti foil of 20 mm diameter and 100 μm thickness into air and was impinged vertically to a DUT. A target board and a ZnS fluorescence screen were mounted on an X-Y stage. The beam position was first monitored by the fluorescence screen and then the target board was moved to the beam position (The beam was stopped with a beam stopper while the X-Y stage was in motion.). The actual beam profile and beam intensity were measured, individually for each chip with dosimetry of a 100 μm thick Cu foil placed in front of the DUT. The beam intensity at the final beam stopper was approximately 0.5–4 nA. The beam was intentionally broadened up to the size of approximately 20 mm diameter.

III. Radiation Test Results

A. CMOS and Actel Anti-Fuse FPGA

1) CMOS: We have used a total of three different types of ASICs in the system. Two chips are made using ROHM 0.35 μm full custom CMOS technology. One is called Patch-Panel (PP) ASIC, and the other one is called Slave Board (SLB) ASIC. The detailed functionality of these chips has been discussed in [9]. While the SLB ASIC contains digital circuits only, the PP ASIC has some analog transistor circuits (for LVDS to TTL conversion and sub nano-second fine delay) in addition to digital ones.

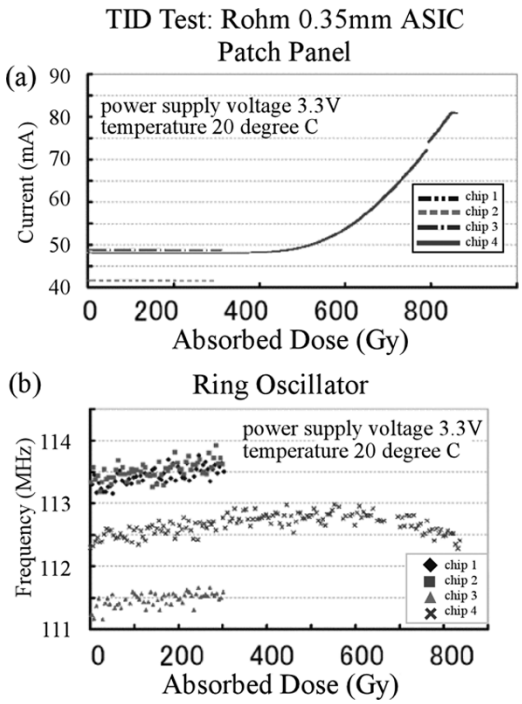

Fig. 1. TID level measurement of ROHM 0.35 μm ASIC chips. (a) The supply current of the chips versus dose for the patch panel ASIC chips which are actually used in the system (the data plot of chip 1 and chip 2 are over-wrapped). (b) The frequency versus dose for specially processed ring oscillator circuit in ROHM 0.35 μm ASIC(501 NAND).

In order to evaluate the TID condition of the 0.35 μm ROHM CMOS chips, we have tested four PP ASIC chips. Three chips were irradiated up to 300 Gy, and the other one was irradiated to 850 Gy. As shown in Fig. 1(a), for a dose of up to 300 Gy, we have observed no increase of the static current for all the chips. The current of the fourth one had increased from 49 to 81 mA monotonically as the irradiation level increased from 500 to 850 Gy.

In order to observe any characteristic change of a circuit caused by the irradiation in more detail, we have processed a ring-oscillator circuit in an independent chip with the same technology. The circuit is connected with 501 NAND gates to form a ring to make the oscillation frequency. We have also irradiated this chip under the same condition as the one for the PP ASIC. Fig. 1(b) shows the frequency change with the irradiation. We find that the frequency had increased up until a dose of 600 Gy and then had decreased. This means that the circuit response became once faster owing to irradiation, and then it became slower.

We have processed a four-bit 256 stage shift register in an independent ASIC in order to evaluate σ_{SEE} for ROHM 0.35 μm chips. We have produced four shift register chips. In the SEE test of this special ASIC, we have observed a total of 185 times a soft SEE [single event upset (SEU)] and no hard SEEs [single event latch-up (SEL)] for four chips with $6.3 \times 10^{12}\ \mathrm{protons/cm^2}$ of total integrated proton intensity injected (fluence). The σ_{SEU} is estimated as $2.8 \times 10^{-14}\ \mathrm{cm^2/bit}$.

2) Actel Anti-Fuse FPGA: Two different series of Actel anti-fuse FPGA (A54SX-A) and Axcelerator are used to implement various ancillary logic circuits in the system. Medium

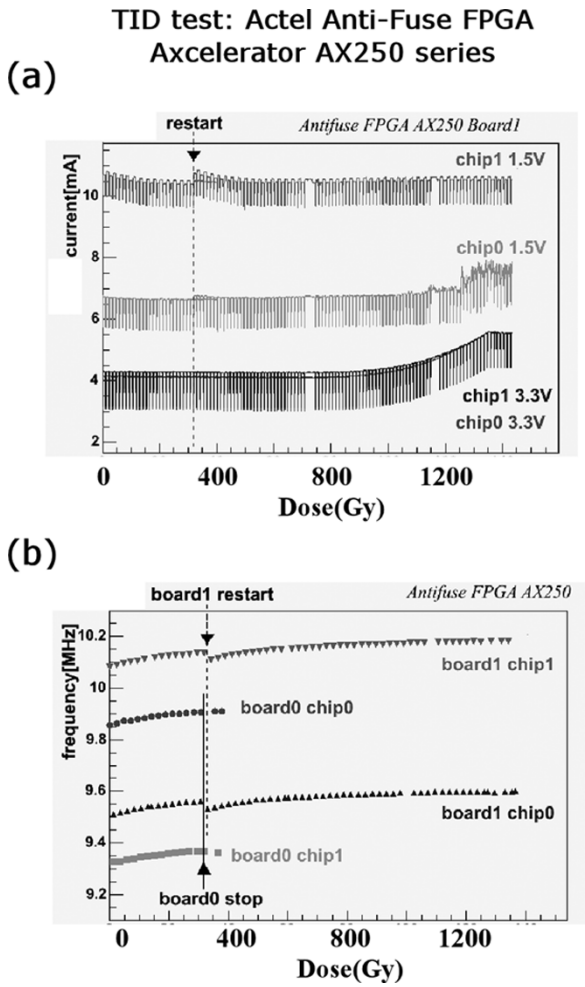

Fig. 2. TID results for Actel anti-fuse FPGA Axcelerator series chips. In an FPGA chip, a ring oscillator with 101 NAND gates has been implemented. (a) The supply current versus dose level for the chips which were irradiated up to 1,300 Gy. During the irradiation, the ring oscillator operation has been paused every minute for 10 s. This Axcelerator chips requires two power lines, one for the I/O cell (3.3 V) and the other one for the core logic part (1.5 V). (b) The ring oscillator frequency versus dose level.

scale FPGA A54SX-A is used for a JTAG routing controller (JRC) and a VME interface, which is commonly used for modules mounted in the on-detector VME crate. The Axcelerator chip is a large scale FPGA with an embedded memory. We use this chip for both transceiver and receiver in a readout data concentrator module. Both the transceiver and the receiver need FIFO in order to absorb the different rates for the data transmission.

The static current for four Axcelerator series FPGA chips versus the absorbed dose is shown in Fig. 2(a). During the measurement, the operation of the built-in circuit (a ring oscillator with 101 NAND gates) has been paused regularly for 10 s in every 1 min. This is the cause of the saw-toothed structure in the graph. The frequency of the ring oscillator versus the dose is shown in Fig. 2(b). We measured two different currents per chip, one is for the I/O cell which is operated with 3.3 V, and the other one is for the core logic part which is operated with 1.5 V.

From both figures, we found that neither significant current increase nor frequency change has been observed in all the four chips tested. We have done the same measurement for SX-A series chips. The dynamic range of the change with the dose for both the supply current and the frequency of the SX-A series chips were greater than ones of the Axcelerator series.

TABLE I
COMPILATION OF SEU (SOFT SEE) TESTS

Technology	Proton fluence (protons/cm^2)	σ_{SEU} (1/cm^2/bit)
ROHM CMOS 0.35μm	6.3x10^{12}	2.8x10^{-14}
Actel FPGA SX-A	2.6x10^{12}	<1.5x10^{-15}
Actel FPGA Axcelerator (R-cell)	1.4x10^{12}	1.6x10^{-14}
Actel FPGA Axcelerator (Memory)	1.4x10^{12}	4.9x10^{-14}

We find that the radiation susceptivity of the Axcelerator chips is comparable with the ROHM 0.35 μm ASIC. The Axcelerator chips were processed with more advanced technology of 0.15 μm CMOS anti-fuse than SX-A ones. This makes presumably the radiation tolerance of the Axcelerator stronger than SX-A and comparable with ROHM ASIC chips.

For the SEE level measurement of SX-A series chips, we have installed a four bit shift register of 256 stages (1024 bit) as we have done in the ASIC case, and read and verified the data outputted. No soft SEE (SEU) has been observed with the fluence of 2.6×10^{12} protons/cm^2. Therefore, σ_{SEU} is estimated as $< 1.5 \times 10^{15}$ cm^2/bit with 90% confidence level. We have also installed a four bit shift register in flip-flop cells (R-cells) of the Axcelerator chips. The length of the shift register was 345 stages (total 1,380 bit) in this case. We have applied the SEE test also to the embedded memory whose size is 54 kbit. Since the memory is configured as a dual port memory, regularly we inputted a bit pattern to the memory, and compared it with the output bit pattern from the memory for verification. We have observed 32 SEU in the R-cell and 3,869 in the embedded memory with 1.4×10^{12} protons/cm^2 of the proton fluence. σ_{SEU} for R-cell (Flip flop cells in FPGA) is estimated as 1.6×10^{-14} cm^2/bit, and σ_{SEU} for Memory is 4.9×10^{-14} cm^2/bit. No SEL has been observed in Actel anti-fuse FPGA chips. We have summarized the SEU level measurements for both CMOS and anti-fuse FPGA in Table I.

3) Mitigation of SEU: For both ASIC and FPGA chips, we have many registers to keep parameters necessary to drive the chips. In the case of the ASIC, we have installed a total of 3.4×10^6 bits (NCHAN) for the registers in the whole system. The number of SEUs anticipated for the ASIC chips operated in the system for ten years (10^8 s) is calculated as $\sigma_{\mathrm{SEU}} \times \mathrm{SRL} \times \mathrm{NCHAN}$, where SRL is the simulated radiation level for ten years, and the worst value in the region where our system is located in the ATLAS detector is estimated as 2.11×10^{10} hadrons/cm^2 for hadrons with the energy greater than 21 MeV [2]. Therefore, the number of upsets in all the ASIC chips for a day is estimated as 1.73. In order to improve the immunity of the system from SEUs further, we keep every bit in the registers of both the ASIC and FPGA with three

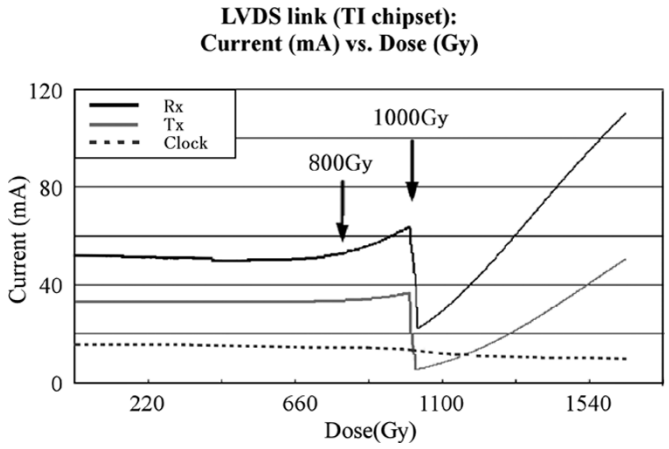

Fig. 3. Supply current versus dose level for LVDS link serializer (Tx) and deserializer (Rx) of TI product. The clock means a clock chip (40.08 MHz) irradiated together with the chipsets.

TABLE II
NUMBER OF OBSERVED FOR LVDS CHIPSETS OF TI AND NS

Vendor	Chip	SEU	Link failure	F (cm^{-2})
TI	Rx	6	2	$5.4x10^{12}$
	Tx	8	7	$7.6x10^{12}$
NS	Rx	55	36	$2.3x10^{12}$
	Tx	1	5	$3.7x10^{12}$

TABLE III
SEE CROSS SECTIONS FOR THE CHIPSETS OF TI AND NS

Chip	Vendor	σ_{SEU} (cm^2)	σ_{link} (cm^2)
Tx	NS	$1.3x10^{-13}$	$1.2x10^{-12}$
	TI	$2.5x10^{-12}$	$1.5x10^{-12}$
Rx	NS	$2.0x10^{-13}$	$1.2x10^{-11}$
	TI	$8.0x10^{-13}$	$6.3x10^{-13}$

redundant flip-flops. Outputs of the flip-chips are connected to a voter logic to select majority values among two different values if one of the flip-flops has suffered an SEU.

Although an error correction code (ECC) will be also a candidate for protection of the SEU, we have chosen the voter logic eventually because it is simpler to implement and has also a simpler error correction logic than ECC. The voter logic is implemented only for the registers in the ASICs to maintain the setup parameters. Total number of register bits in an ASIC is at most a few hundreds. We have enough resources to implement it to every bit of the registers.

Three flip-flops to hold the same bit data must be placed apart in an ASIC to keep damage from the cluster burst of high energy heavy particles minimum. We have not paid particular attention to this in the place and routing stage of the ASIC design.

B. Two LVDS Serializer and Deserializer Chipsets

LVDS links are used for data transfer from the front-end on-detector part to the second on-detector part over 15 m. While STP category 6 cables will be used in the ATLAS detector, STP category 5e cables have been used throughout the radiation tests. For the serial data transfer with the LVDS link, we have two selections for COTS serializer and deserializer chipsets (one from Texas Instruments (TI) [2]: SN65LV1023/1224 and one from National Semiconductor (NS) [3]: DS92LV1023/1224). Both chipsets have identical functionality and even the same pin allocation, though the frequency range is slightly different.

We have irradiated four samples from each LVDS chipset candidate with γ-rays up to a dose of 300 Gy. The supply current of all samples was stable during the irradiation, and kept pre-irradiation level up to 300 Gy. One sample among four from each candidate was exposed further to 1,600 Gy. Fig. 3 shows the dependence of the supply current on the absorbed dose up to 1,600 Gy for a TI sample. Both serializer (Tx) and deserializer (Rx) of the TI candidate showed an increase of current for doses from 800–1,000 Gy, and an abrupt current drop immediately above 1,000 Gy. An LVDS link could no longer be established after the current drop while the chipset of the NS candidate has no significant increase of the current even up to a dose of 1,600 Gy.

In the SEE test, the serializer and deserializer were mounted on a PC board, and these chips are connected to each other for the data transfer between them on the board. We have checked the functionality during the proton irradiation remotely by sending some bit patterns to Tx on the board and receiving them from Rx on the board. We have tested two pairs for each NS and TI candidate. The data taken in the test for two LVDS chipsets are summarized in Table II.

In Table II, we have classified the abnormalities observed during the irradiation into two classes. If the monitor board detects a different bit pattern rather than the pattern which it has sent, then it is regarded as an SEU error. The link failure means that Rx could not synchronize its clock with the clock embedded in the data sent, i.e. it could not phase-lock the clock with one sent from Tx. The value F given in the last column of the table is the total integrated proton intensity.

Based on Table II, we have estimated σ_{SEE} independently with two error categories and listed in Table III. The simulated radiation level (SRL) for Tx and Rx for ten years are estimated as 2.11×10^{11} and 1.42×10^{11} $\mathrm{hadrons/cm^2}$, respectively. The number of LVDS links we must install in the ATLAS detector will be 10^4. With these numbers we can estimate the total $(\mathrm{Tx}+\mathrm{Rx})$ failures rate in the system per day for both candidates as

- the number of SEU errors/day: 2.5 (NS) and 0.6 (TI);
- the number of link error/day: 1.7 (NS) and 0.4 (TI).

If, however, we compare the time dependence of the error incidence of Rx, for example, for both vendors, we find very different characteristics between two versions as shown in Fig. 4. All samples of NS Rx showed always SEU and link failures uniformly over the irradiation period while the ones of TI showed seldom SEU and link failures. All TI Rx showed, however, a significant increase of the source current above the proton dose of 300 Gy and up to 1,200 Gy where all the TI Rx had failed. The increase of the source current has been observed already in the TID test for TI samples as shown in Fig. 3.

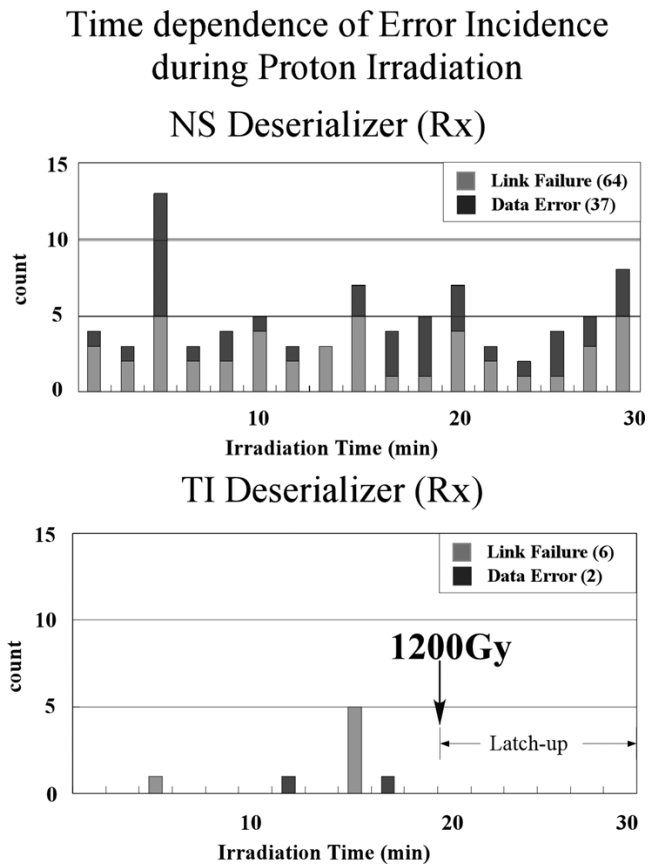

Fig. 4. Time dependence of error (link failure and bit failure) incidence for deserializer (Rx) chips of NS and TI. Although the TI chip has a very small rate for the error occurrence, it has failed (due to single event latch-up) after proton irradiation of 1,200 Gy.

As far as the SEE test results are concerned, the chipsets of both vendors fulfill the criteria required by the ATLAS radiation working group [2]. With the TI chipsets significant less SEUs and link failures have been observed than with NS while TI Rx failed at an irradiation level of approximately 1,200 Gy. However, for the ATLAS muon endcap electronics, we will eventually use TI chipsets since the 1,200 Gy radiation level is beyond the maximum limit for the region we are concerned.

C. G-Link Serializer and Deserializer Chipset

Four Agilent G-Link chipsets with Infineon optical transceivers were irradiated with γ-rays of up to 300 Gy in the TID measurement. During the irradiation, we maintained the data transfer between the G-Link Tx and Rx via the optical transceivers monitoring the bit transfer error. None has shown a distinct current increase up to a dose of 300 Gy, and no bit error has been observed in this test system setup.

In the SEE test, we have also measured data transfer errors and link failures as a similar way to the LVDS test. We have also made a qualification test of an optical transceiver for the proton irradiation in addition to Tx and Rx. A total of two samples for each chip have been tested. In Table IV, we summarized the aggregated sum for the number of SEUs detected and number of link-lock failures with the total integrated proton intensity (F) for all three G-Link chips.

TABLE IV
NUMBER OF SEE OBSERVED FOR G-LINK CHIPSET AND THE OPTICAL TRANSCEIVER

Chip	SEU	Link failure	F (cm^{-2})
Tx	4991	77	$2.3x10^{11}$
Rx	2802	162	$2.4x10^{11}$
Opt. Trans	69	0	$8.1x10^{11}$

TABLE V
SEE CROSS SECTIONS FOR G-LINK CHIPSET AND THE OPTICAL TRANSCEIVER

Chip	σ_{SEU} (cm^2)	σ_{link} (cm^2)
Tx	$2.2x10^{-8}$	$3.3x10^{-10}$
Rx	$1.2x10^{-8}$	$6.7x10^{-10}$
Opt.Trans.	$8.5x10^{-11}$	$< 3.0x10^{-12}$

Even after the link failure observed in Tx, synchronization was recovered autonomously for all 77 cases. The recovery time was 8 μs in average, and it never exceeded 10 μs as the longest time. Three out of a total of 162 link failures observed in Rx could not be re-locked autonomously but recovered Rx by sending a synchronization pattern from the Tx side. In this case the recovery for a phase loop lock took 38.4 μs.

We have estimated separately the cross sections σ_{SEE} for SEU and link failure and summarized them in Table V.

With the simulated radiation level (SRL) of Tx and Optical Transmitter for 10 years as 6.54 $\mathrm{hadrons/cm^2}$ and the number of chips for both Tx and the optical transceivers as 1,000 we can estimate the number of errors of Tx per day as 1.9 for SEU and 120 for link error, and of the optical transceiver as 0.5 for SEU and $<$0.02 for link error.

IV. SUMMARY

The radiation tolerance of ROHM 0.35 $\mu\mathrm{m}$ CMOS ASIC chips as well as two Actel Anti-fuse FPGA chips have been examined with the TID and SEE measurements. From the estimations based on the measurements, we found that both ASIC and FPGA chips can be used in the ATLAS level-1 muon endcap trigger system without introducing serious degradation for the performance. We have found that Actel SX-A chips are more susceptive to radiation than the Axcelerator chips, and that the susceptibility of the Axcelerator chips is more-or-less the same as that of the ROHM CMOS 0.35 $\mu\mathrm{m}$ ASIC chips. Although there are several drawbacks in anti-fuse FPGAs like its one-time programmability or low logic density, we extend actively the usage of the anti-fuse FPGA chips even in the radiation condition rather than ASIC.

We have found very different radiation characteristics for two types of LVDS chipsets (NS and TI) both in TID and SEE measurements. The NS ones have many SEUs or link failures but immune to TID while the TI ones are relatively insusceptible to SEE if the absorbed dose is less than 1,000 Gy. From the TID measurement, we find that the TI chips have a structure also at around 1,000 Gy as seen in Fig. 3. TI chips are more qualified than NS chips if the dose is less than 1,000 Gy.

TI chipsets will have a small number of errors for both SEU and link failures (less than 1) than NS ($\sim$ a few) per day. From the SEE test, the G-Link chipset has shown no problem for our usage either, though the number of link errors per day will be greater than 100.

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