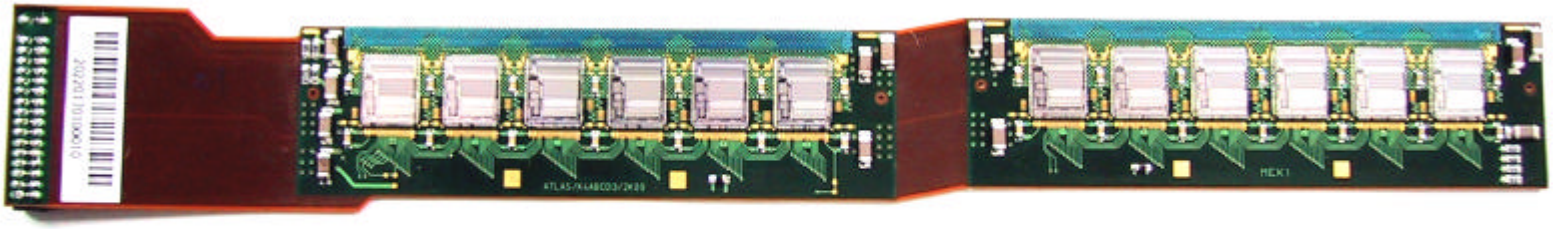
Electrical QA at Japan Site

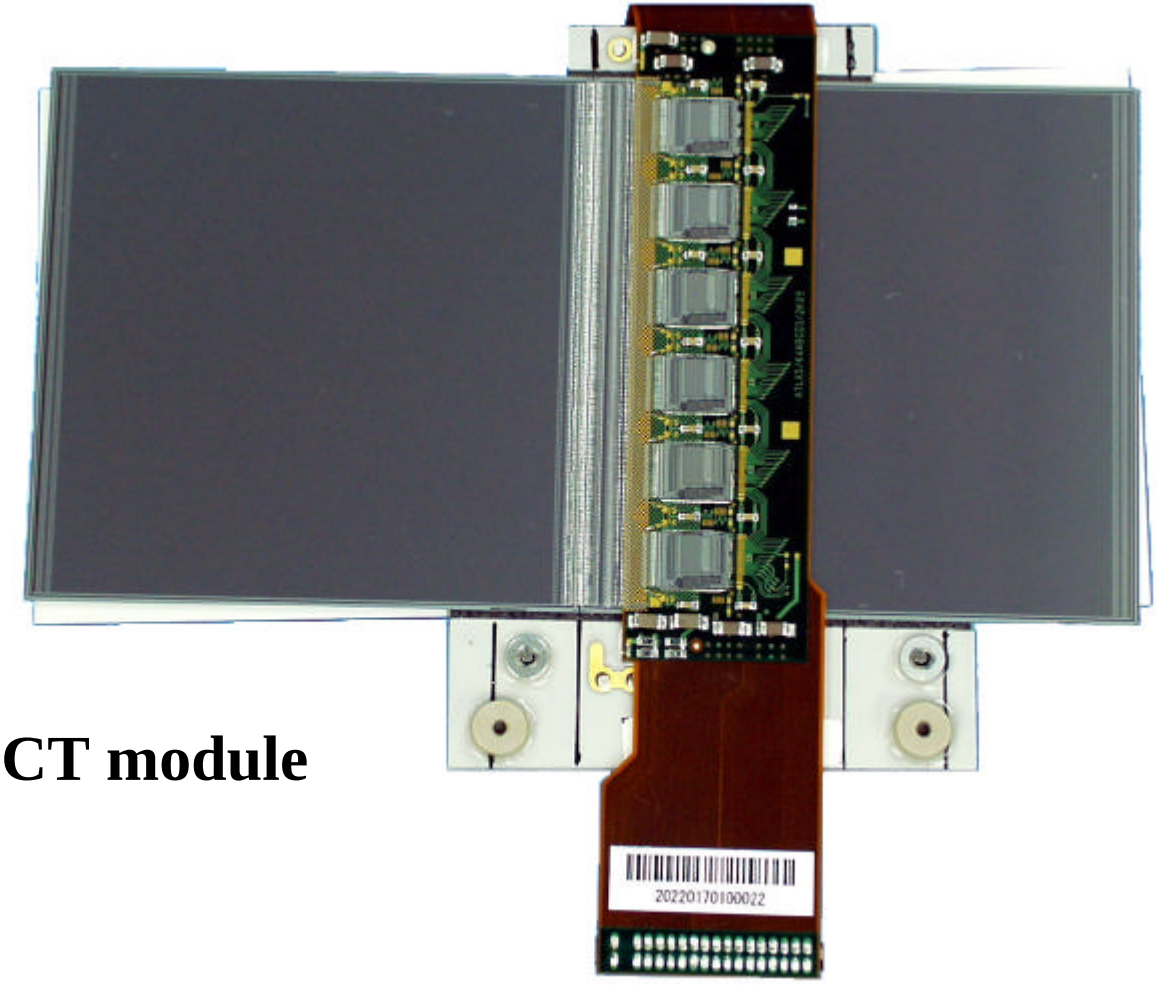
December 11, 2001 SCT week @CERN

Presented by T. Kondo (KEK)

- Completed modules for site qualification
  - 20220170200001 (shipped to CERN and returned)
  - 20220170200002 (shipped to CERN and returned)
  - 20220170200003
  - 20220170200004
  - 20220170200005 (chip #2 was replaced)

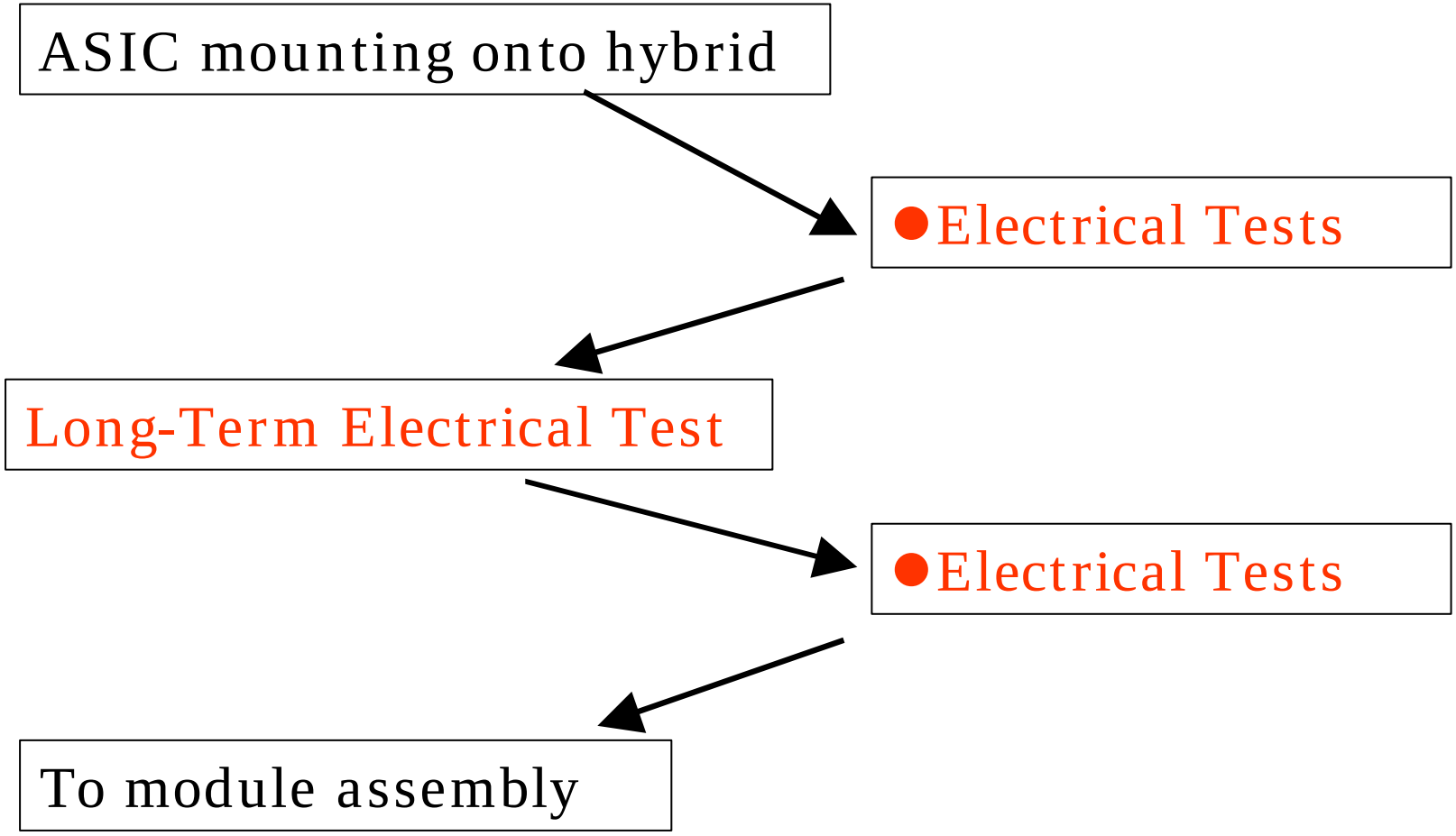


Hybrid

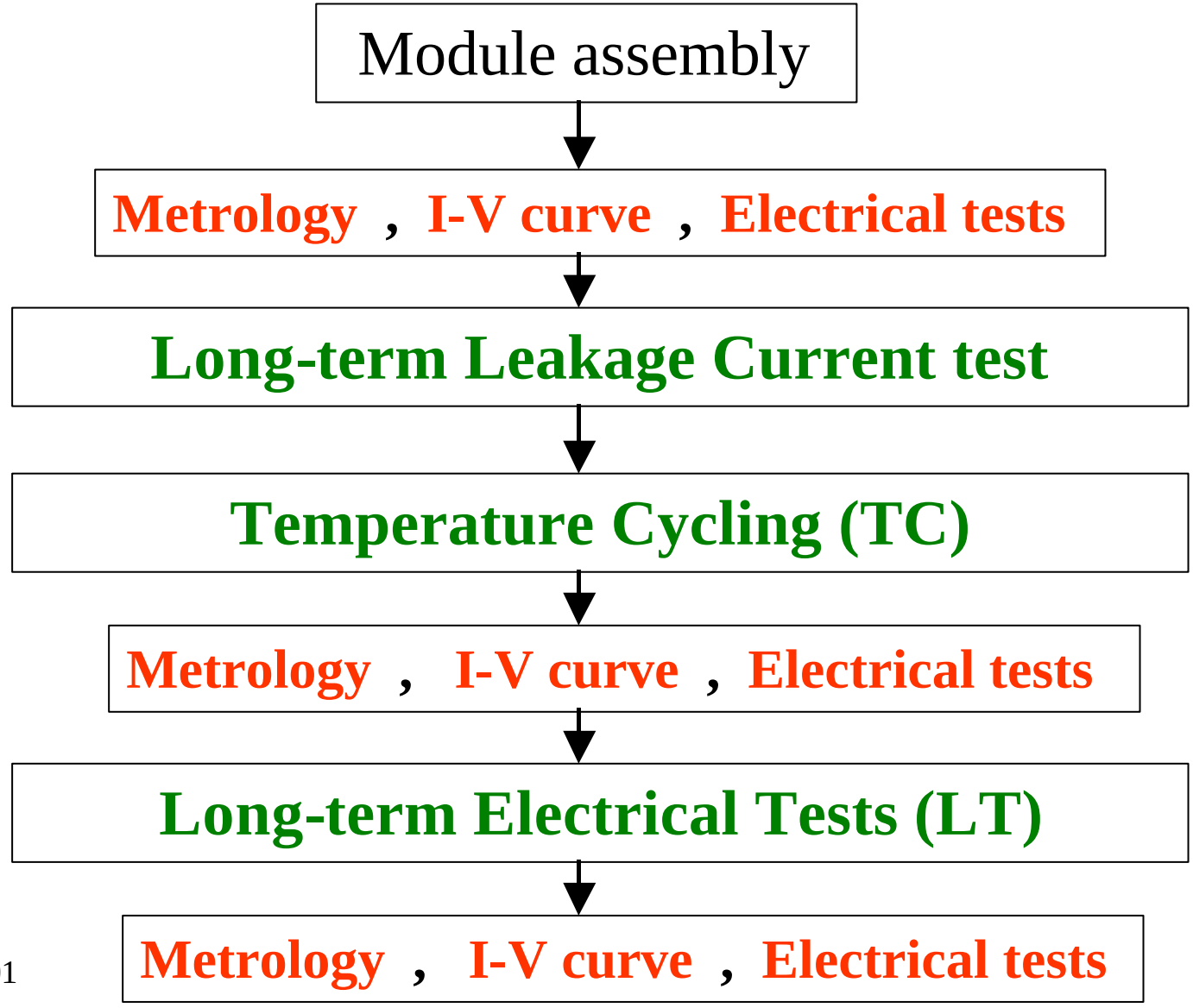


Barrel SCT module

1. QA for hybrid production



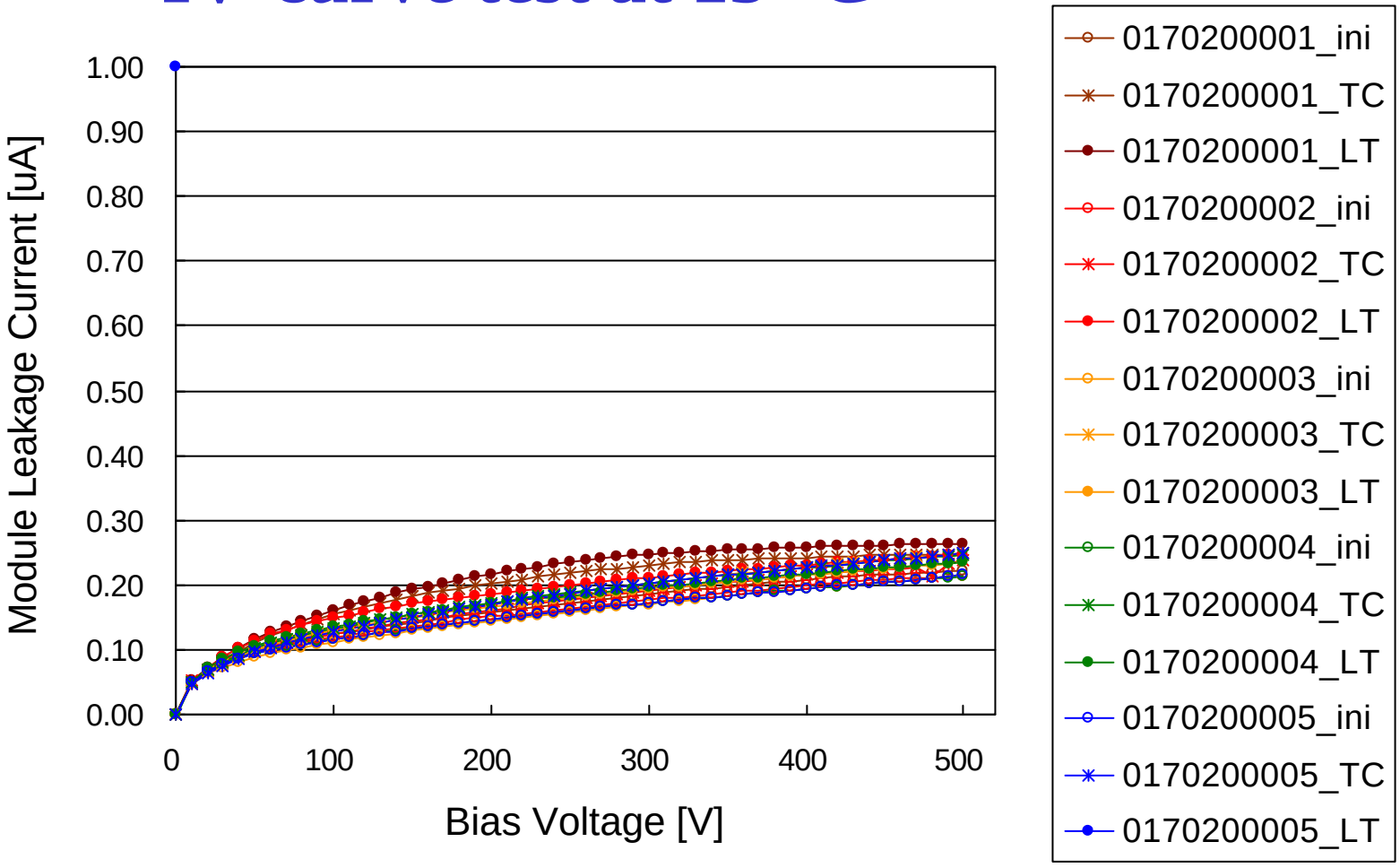
2. QA for module production



3. I-V Curve Test

- Temperature is adjusted to keep 15 °C in Pt100 on the facing.
- V_{bias} ramps up every 10 V from 0 to 500 V.
- I_{leak} measured 5 seconds after V_{bias} setting.
- ASICs are not powered.

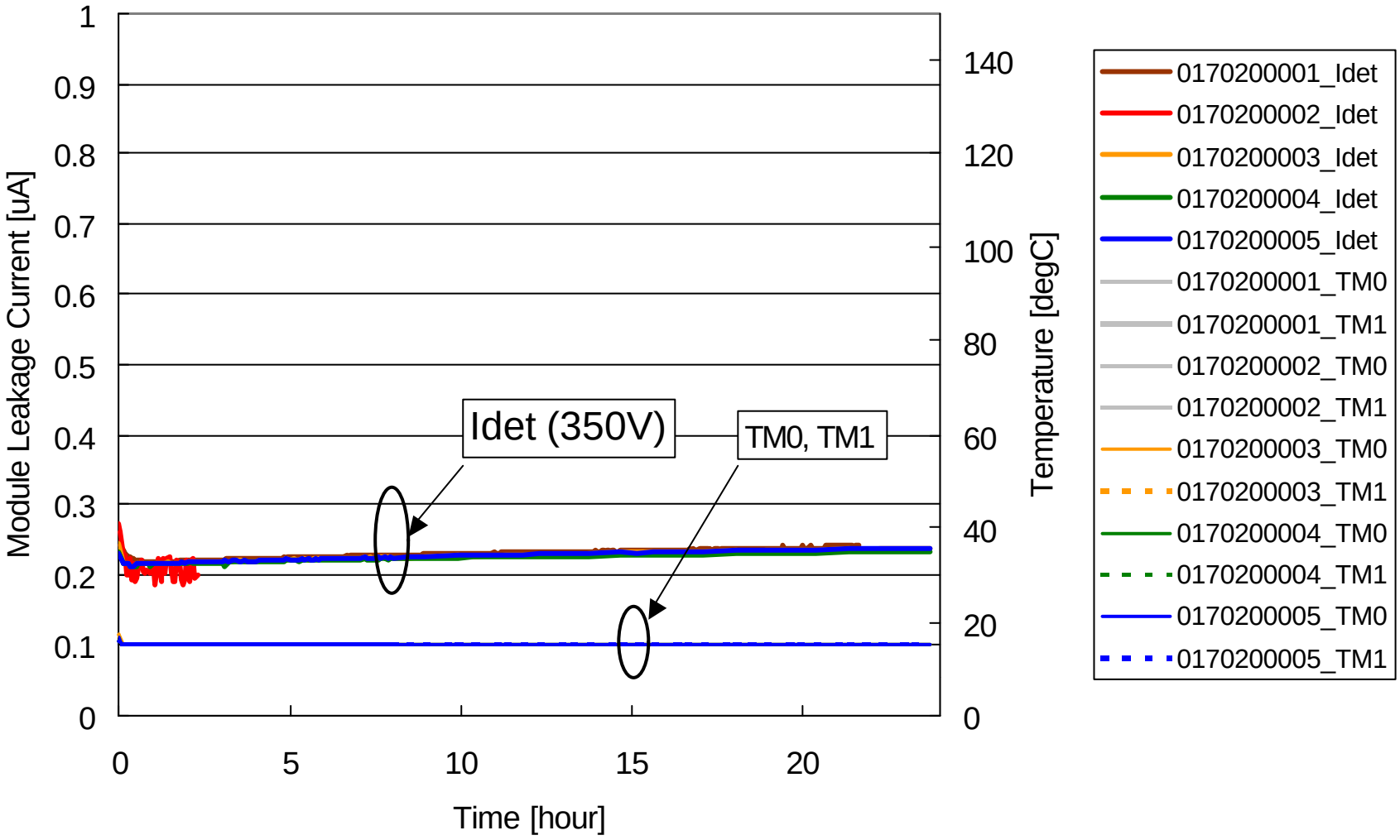
● IV-curve test at 15 °C



4. Long-term Leakage Current Test

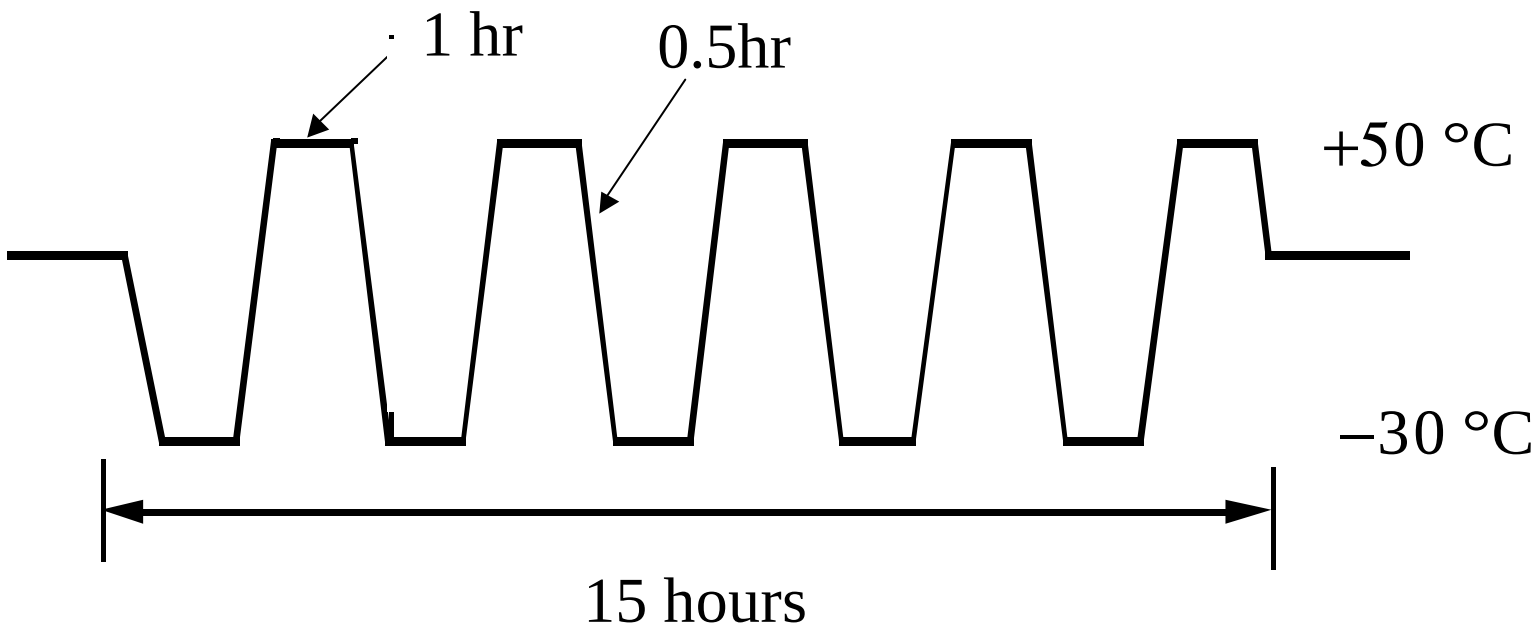
- Measurement of leakage current stability at 350V over 24 hours.
- T_{env} = 15 °C
- Leakage current, thermistors and Pt100 on facing are measured every 5 min.
- ASICs are not powered.

Long-term Leakage Current test at 350 V



5. Temperature Cycling

Cycle : –30 °C to 50 °C, 5 times

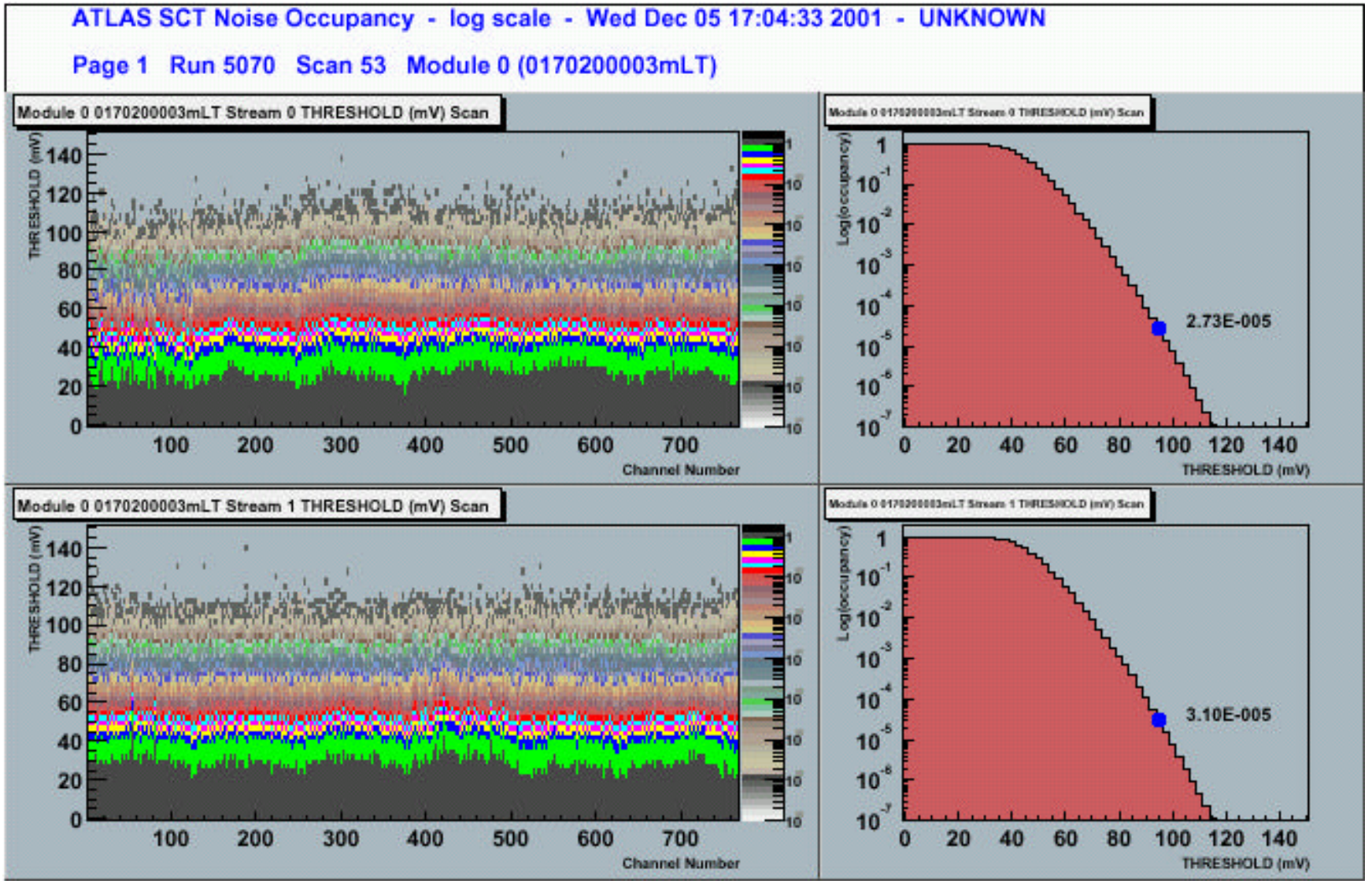


- N_2 flow in module box.
- ASICs are not powered.

6. Electrical Tests

- The bias voltage is set at 150 V.
- Standard characterization sequence is performed.

● Noise Occupancy Scan (02022017020000 3mLT)

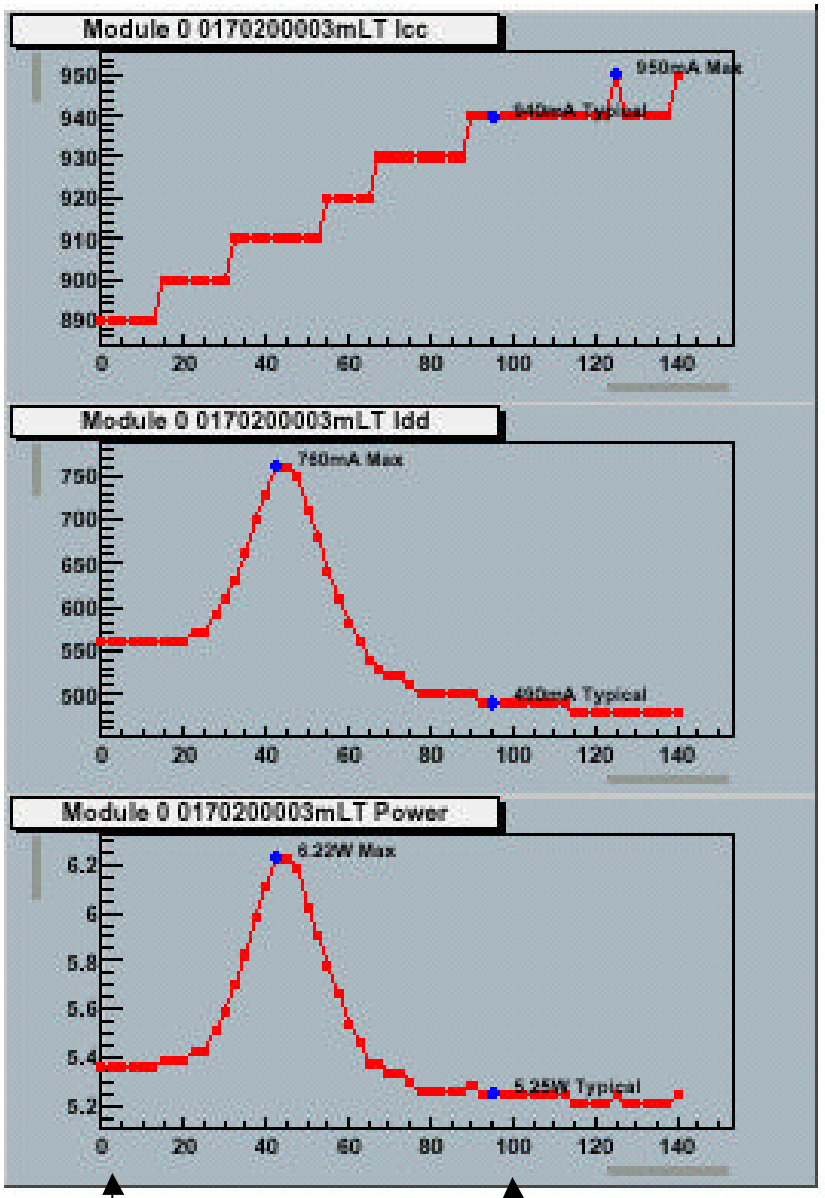


Threshold scan

I_{CC}

I_{DD}

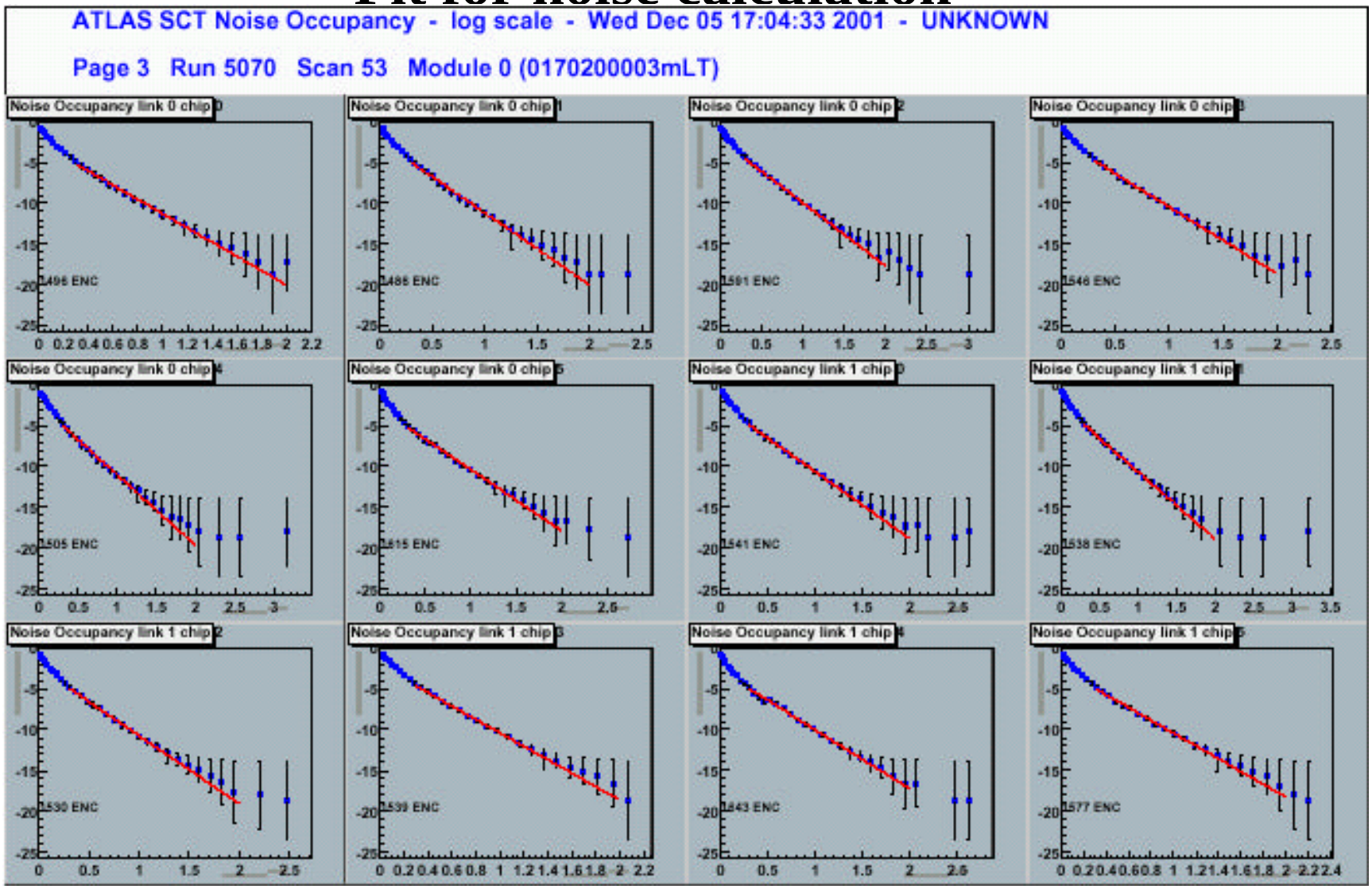
Power



0

100 mV

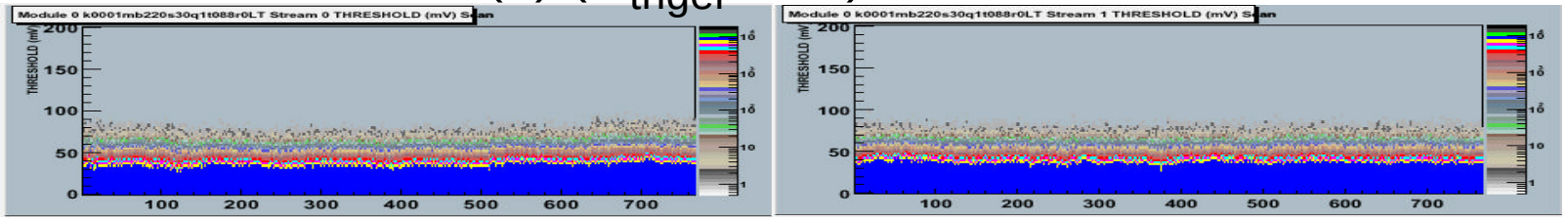
Fit for noise calculation



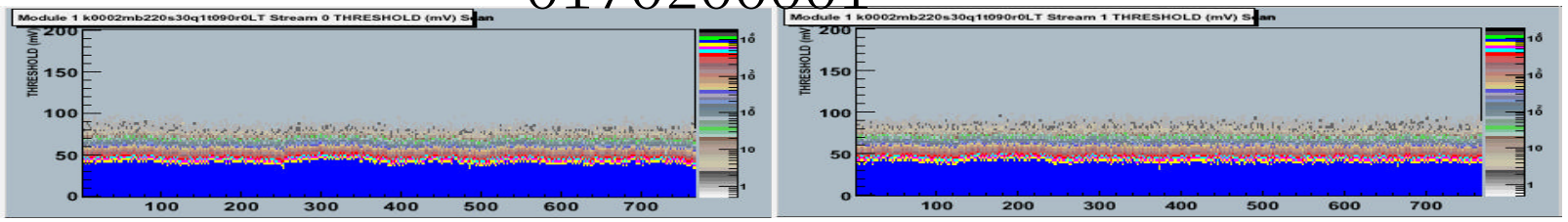
ln (occupancy)

(Threshold [fC]) ^{2}

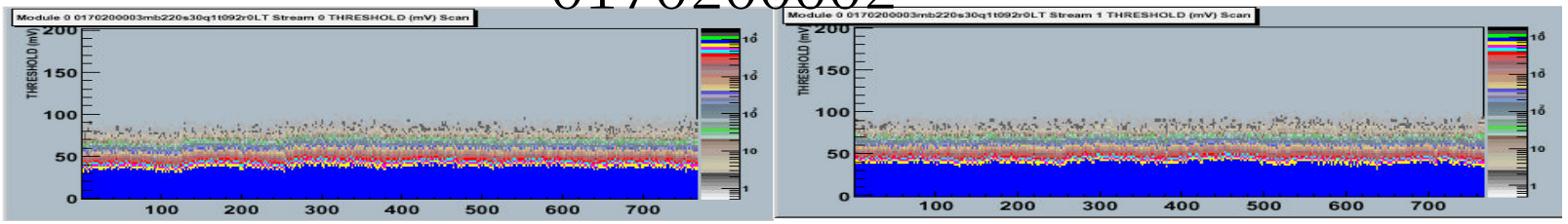
S curves(1) ($N_{triger}=10^4$)



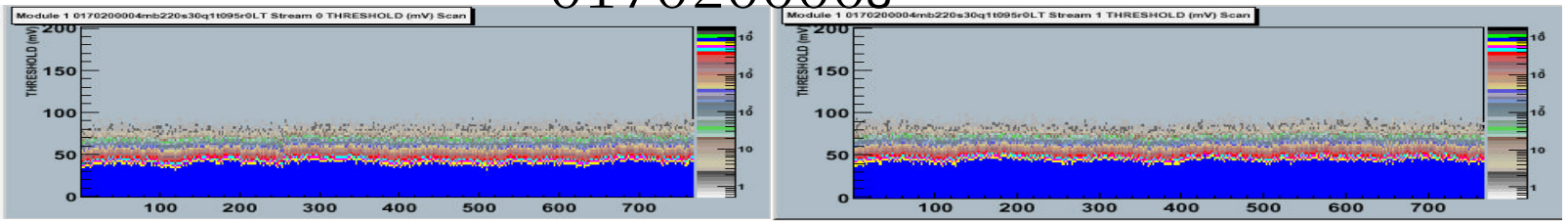
0170200001



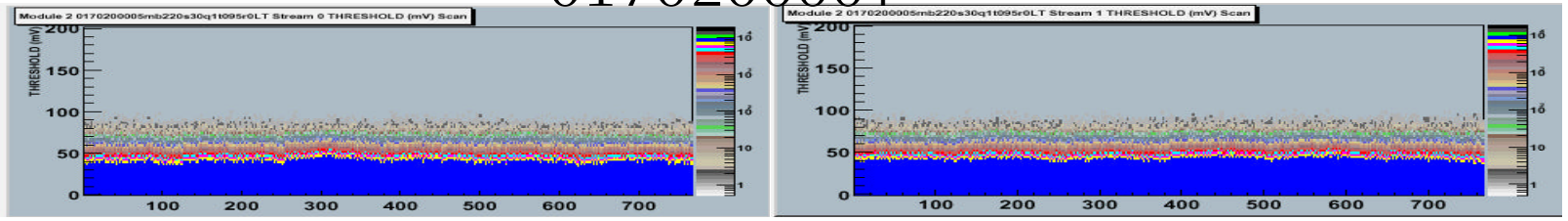
0170200002



0170200003

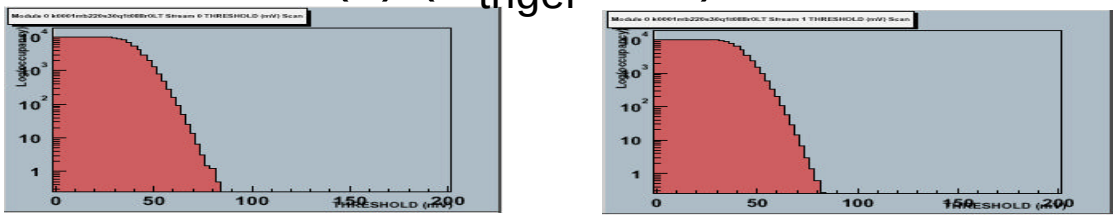


0170200004

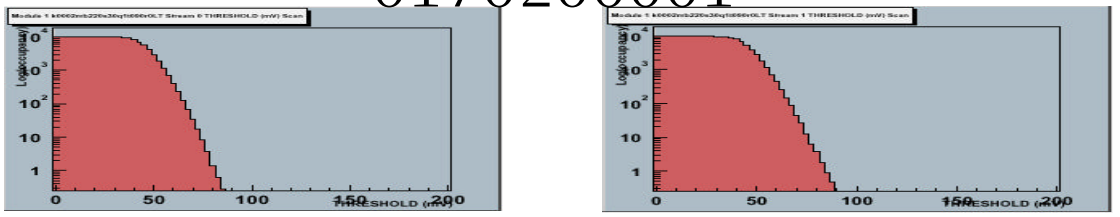


0170200005

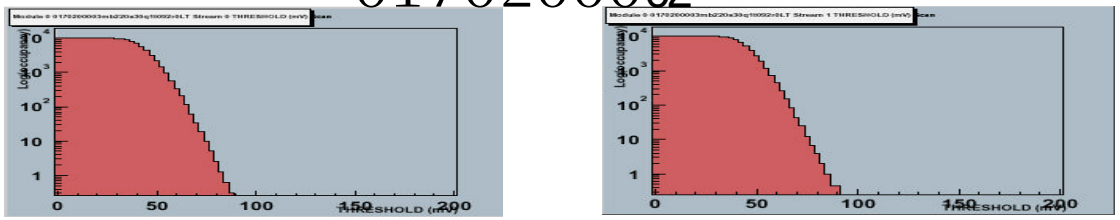
S curves(2) ($N_{triger}=10^4$)



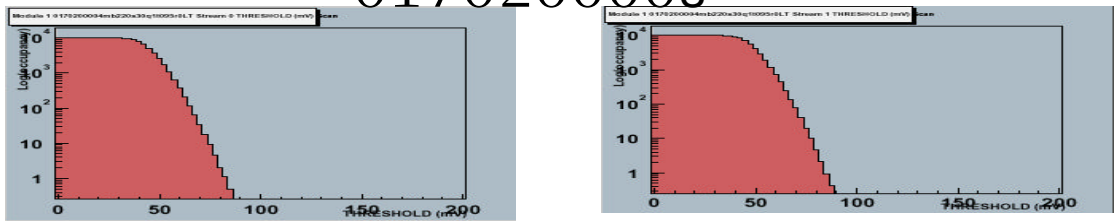
0170200001



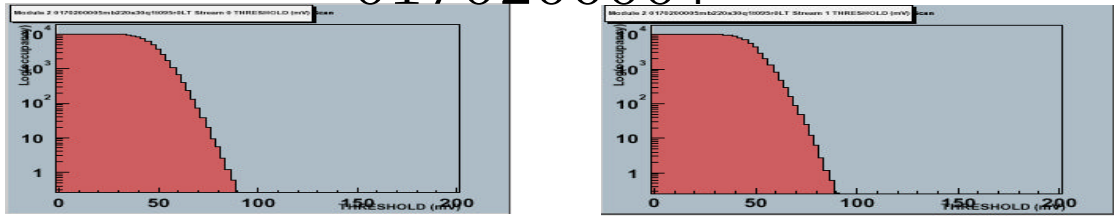
0170200002



0170200003



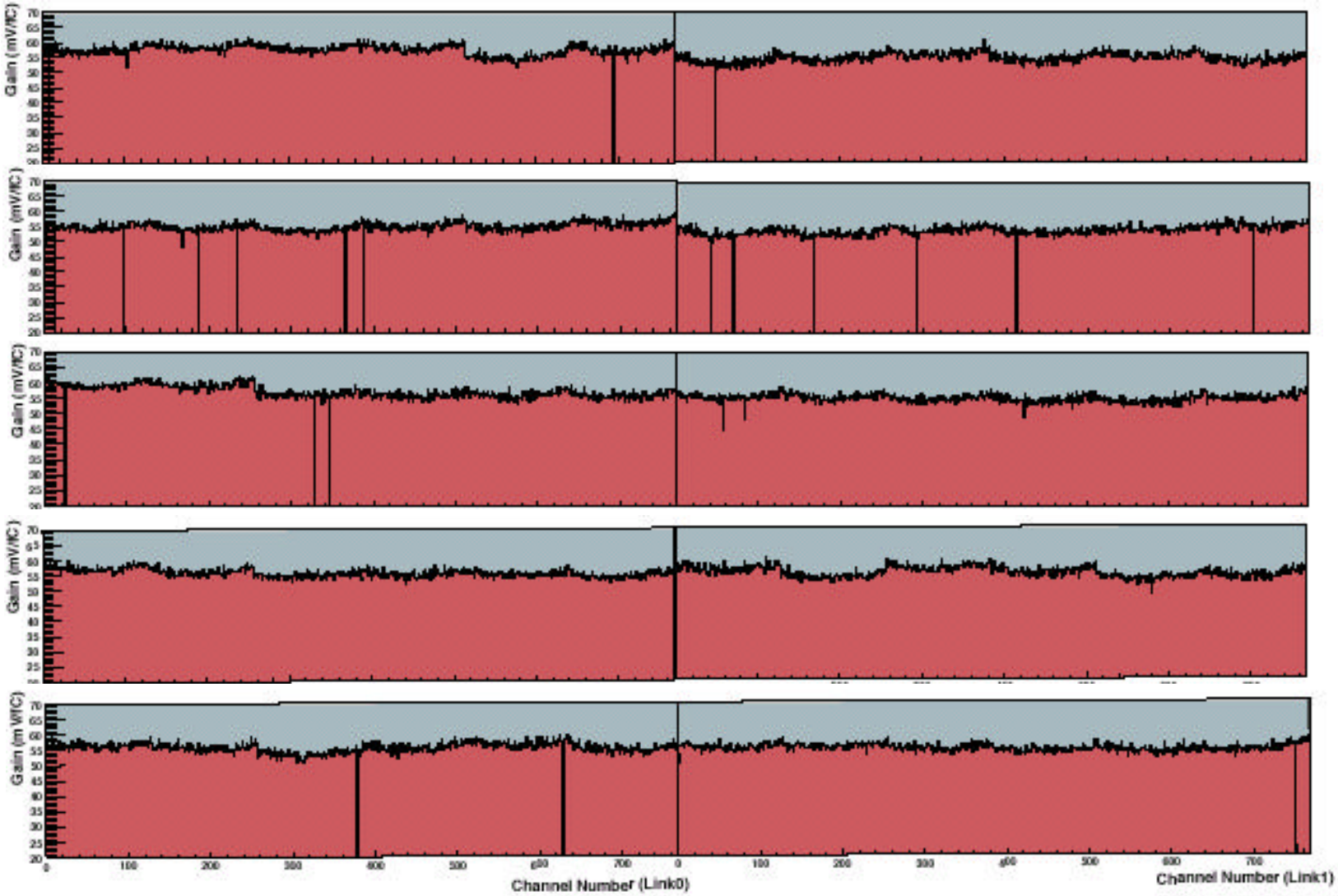
0170200004



0170200005

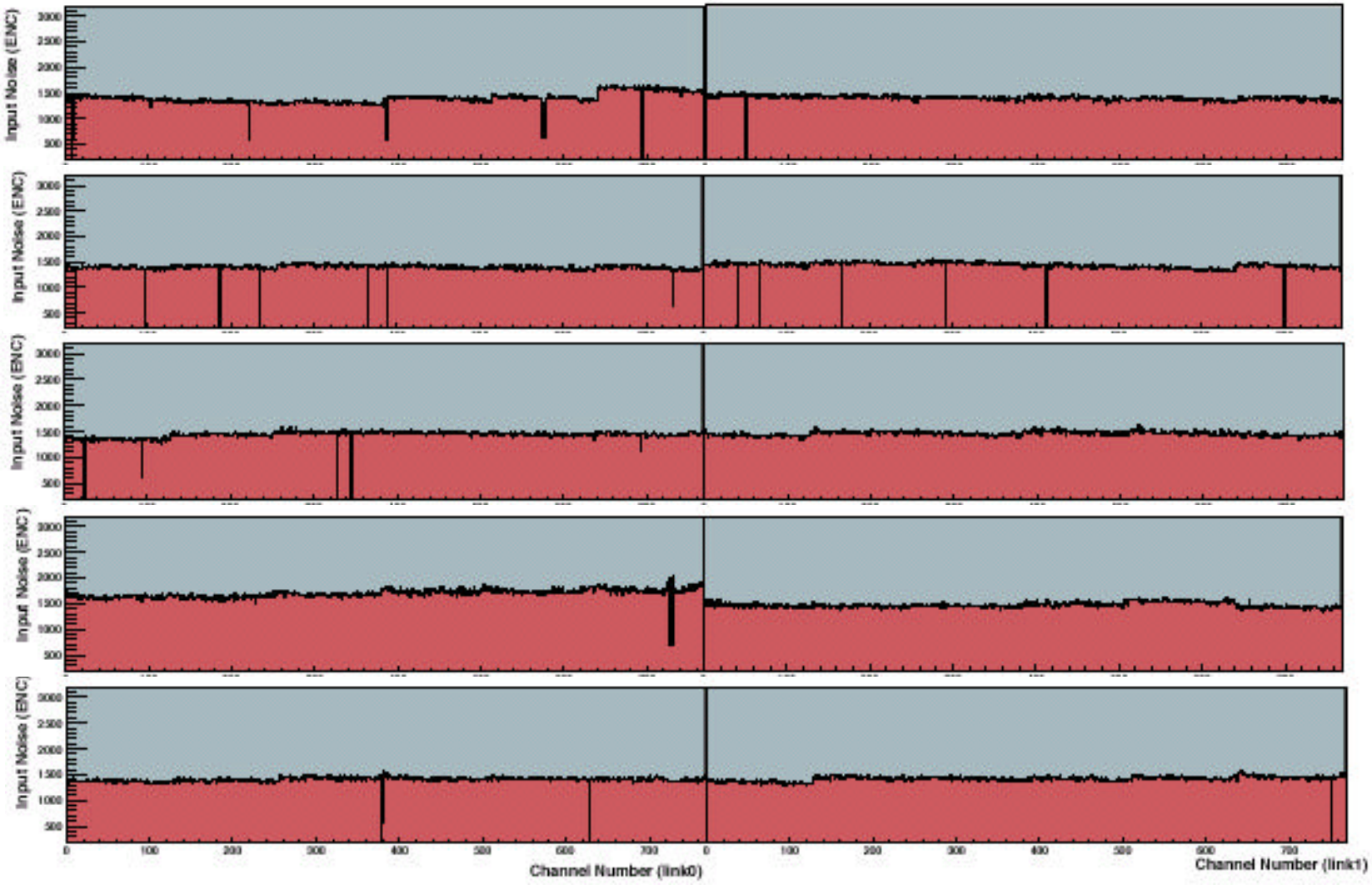
● Gain at 2 fC

0170200001
0170200002
0170200003
0170200004
0170200005



● ENC at 2 fC

0170200001
0170200002
0170200003
0170200004
0170200005



Gain and Noise by the response curves

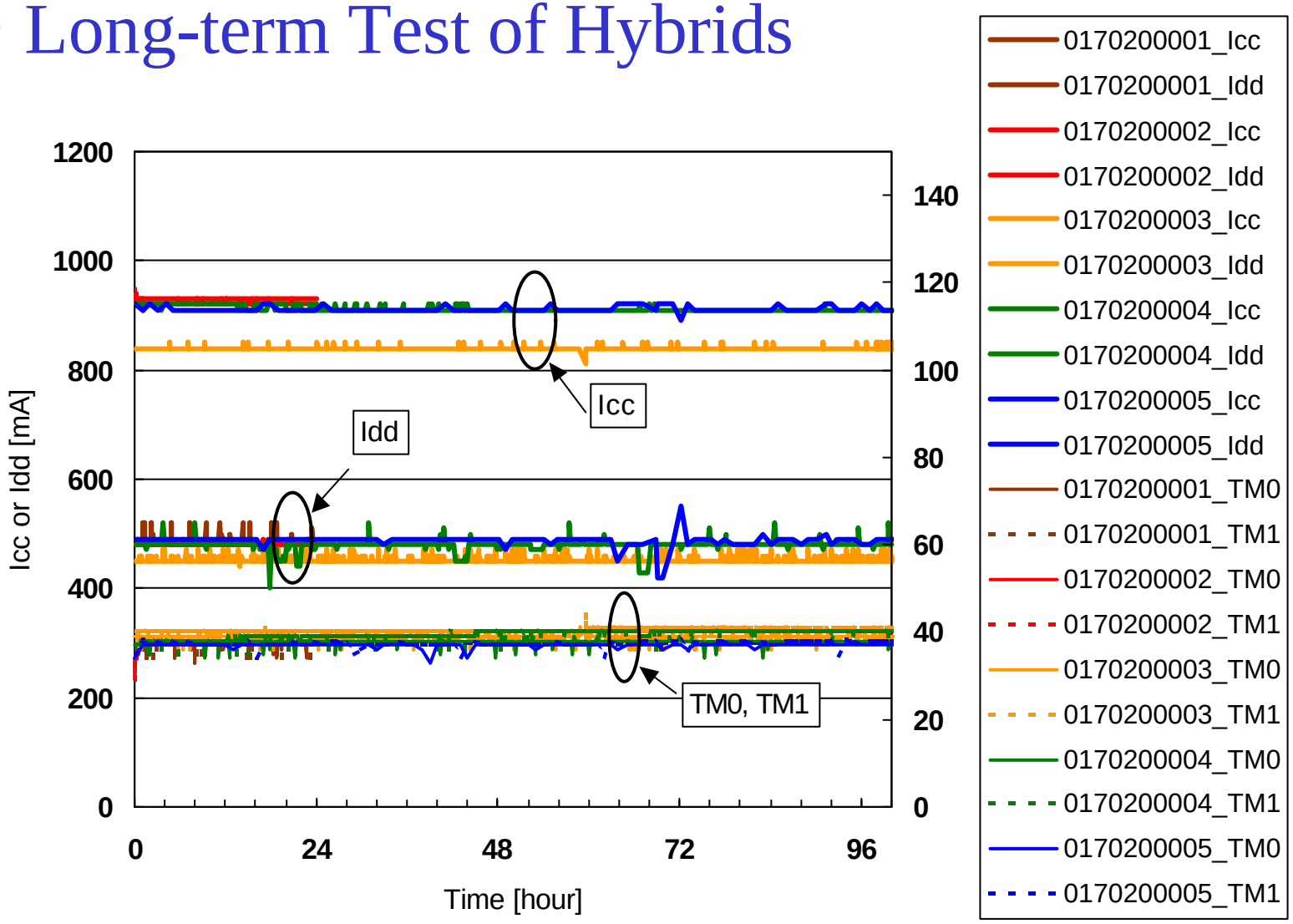
	Hybrid	ASIC wafer	status	Gain[mv/fC]	RMS[mV/fC]	Input Noise[e]	RMS [e]
2022 0170200001	K5		initial	55.92	1.20	1446	65
			after TC	56.49	1.22	1412	63
			after LT	56.23	1.22	1395	62
2022 0170200002	K5		initial	55.20	1.11	1493	40
			after TC	54.33	1.12	1481	38
			after LT	54.51	1.09	1419	36
2022 0170200003	K5		initial	55.69	1.11	1492	38
			after TC	56.42	1.15	1498	37
			after LT	56.28	1.13	1455	36
2022 0170200004	K5		initial	55.56	1.13	1530	45
			after TC	55.28	1.15	1504	44
			after LT	55.43	1.11	1546	48
2022 0170200005	K5		initial	54.99	1.09	1532	46
			after TC	55.24	1.09	1445	43
			after LT	55.10	1.08	1417	42

=> Typical gain : 55 mV/fC, typical noise: 1450e

7. Long-Term Electrical Test (Hybrid)

- Temperature is kept at 37°C* at thermistors on hybrid.
- Total test time is 100 hours.
- N_2 gas flow in temporary boxes.
- ASICs are powered.
- Every hour, 3 point estimation of Gain, Noise and Offset measurement are performed. *
- Thermisters and ASIC currents (I_{CC} and I_{DD}) are measured every 10 min.

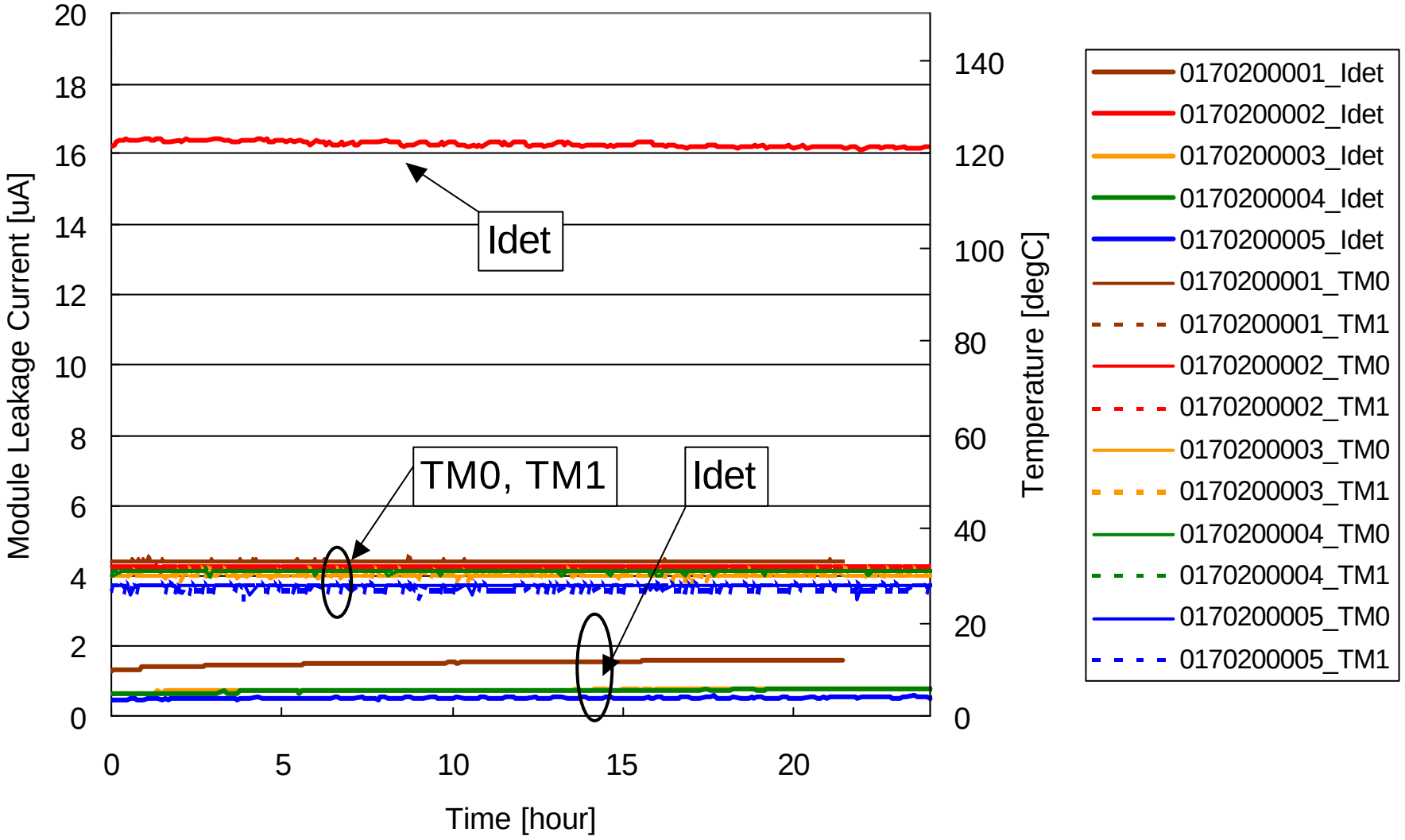
Long-term Test of Hybrids



8. Long-term Electrical Test (Module)

- T_{env} ~ 15°C in environmental chamber.
- Total test time is 24 hours.
- N_2 flow in module boxes.
- ASICs are powered.
- Every 1 hour, a Confirmation Sequence is performed.
- The thermistor, ASIC currents (I_{CC} and I_{DD}) and I_{leak} are measured every few minutes.

Long-term Test of Module at 150 V



9. Difference of Temperature Test*

		TM[degC]	Facing[degC]	Delta[degC]	Generation of Heat[W]
0170200001	initial	30.5	26.1	4.4	5.18
	after Temp Cycle	30.5	25.4	5.1	5.18
	after Long Term	31.5	27.4	4.1	5.25
0170200002	initial	31	26.3	4.7	5.39
	after Temp Cycle	31	28.7	2.3	5.26
	after Long Term	32	25.4	6.6	5.50
0170200003	initial	30	26.9	3.1	5.20
	after Temp Cycle	30.5	27.1	3.4	5.18
	after Long Term	30	26.9	3.1	5.16
0170200004	initial	30	27.1	2.9	5.32
	after Temp Cycle	31	27.6	3.4	5.33
	after Long Term	30	27.1	2.9	5.28
0170200005	initial	28	24.7	3.3	5.28
	after Temp Cycle	28	24.4	3.6	5.26
	after Long Term	27	24.3	2.7	5.14

Thermistor on hybrid Pt100 on facing

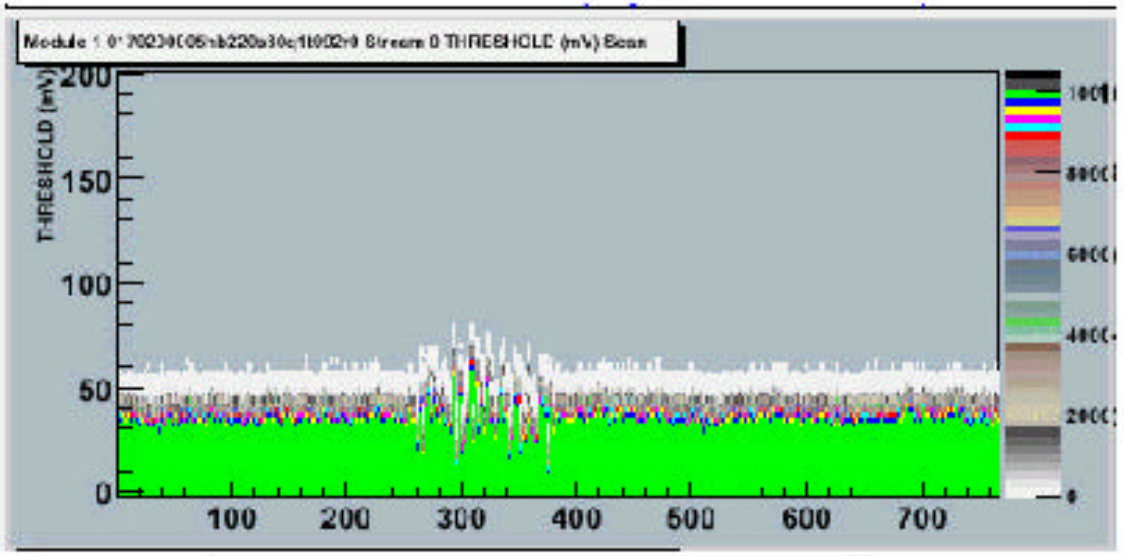
● Chip address confusion on 0170200005

VT50 RMS (0170200005 Link0)

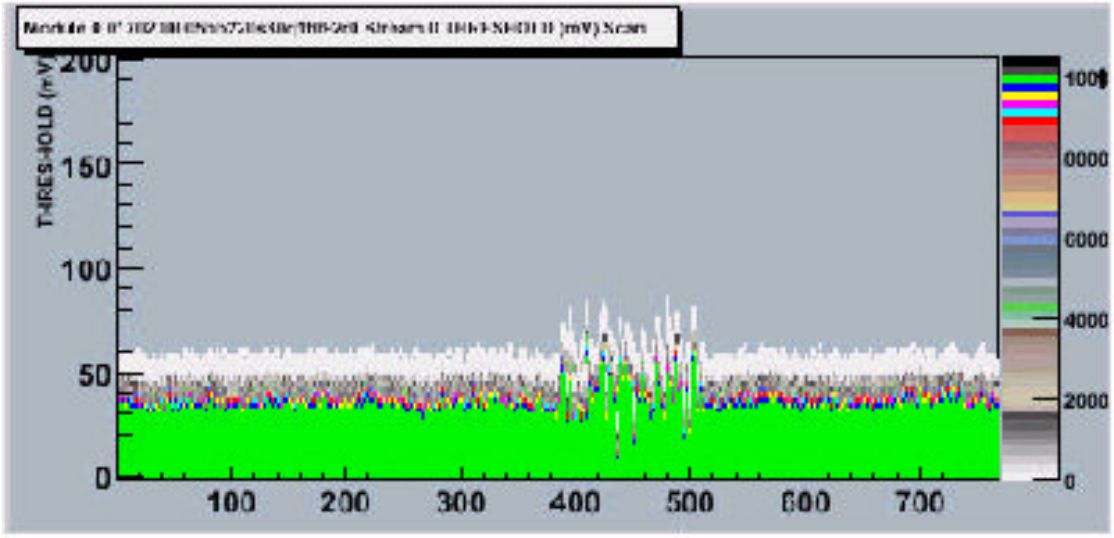
Trim File	chip0	chip1	chip2	chip3	chip4	chip5
0 trim	7.56	7.55	7.98	7.53	7.85	8.26
normal trim	1.53	1.47	9.48	1.74	1.57	1.41
chip2 -> 0 tirm	1.52	1.42	9.44	1.69	1.55	1.34
chip3 -> 0 trim	1.51	1.48	7.83	7.48	1.52	1.38
chip2 -> 0 trim chip3 -> **chip2**	1.5	1.48	1.56	10.53	1.52	1.4

unit:[mV]

- ◆ **There seems an interference between chips #2 and #3.**
- ◆ **Chip #3 works well when chip #2 is detached.**
- ◆ **The module becomes normal after chip#2 replacement.**



Normal Trim



chip2 -> 0 trim
chip3 -> chip2trim

Summary of bad channels

(trim-range=-1)

		mask	unbonded	noisy	total	diff	
0170200001	initial	2	7	0	9		
	after Temp Cycle	2	7	1	10	1	
	after Long Term	3	7	0	10	0	7
0170200002	initial	12	1	1	14		
	after Temp Cycle	12	1	1	14	0	
	after Long Term	12	1	0	13	1	2
0170200003	initial	3	1	2	6		
	after Temp Cycle	3	1	0	4	-2	
	after Long Term	3	1	0	4	0	3
0170200004	initial	0	2	4	6		
	after Temp Cycle	0	2	0	2	-4	
	after Long Term	0	2	1	3	0	4
0170200005	initial	4	2	0	6		
	after Temp Cycle	4	2	0	6	0	
	after Long Term	4	2	0	6	0	4

mask = rejected by trimming (trim-range=0)

=> **Bad channels / all = 35 / 7680 = 0.46 % < 1%**

Summary of Electrical QA

- The electrical QA for hybrid and module production were established including thermal cycling and long-term tests.
- Five modules were completed and passed the electrical QA.
- Fraction of bad channels was 0.46%.
- One chip showed address confusion and was successfully replaced.