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Thermal simulation of ATLAS barrel SCT modules - I

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Abstract

A finite element thermal analysis is performed for the various configurations of the ATLAS barrel SCT module. The design of the module are based on the recent proposal by RAL to reduce the overall radiation thickness of the module. Its several variations are also evaluated. The main goal of the present calculation is to estimate the safety margin for the thermal runaway.

1. Module models

Eight different module geometries as listed in Table 1 are evaluated. Figure 1 shows the mod-

Table 1 Module models

model	description
model-RAL	Original model given by RAL in mid March, 1997
model-1	BeO picture-frame baseboard
model-2	model-1 but with a longer PG basebaord
model-3	model-1 but the baseboard is all made of PG
model-4	model-3 with no thermal connection on the other bridge side
model-5	model-3 added by BeO stiffeners on both sides of PG tongues.
model-6	suggested by Y. Unno
model-8	model-6 but PG extended to the cooling-side edge

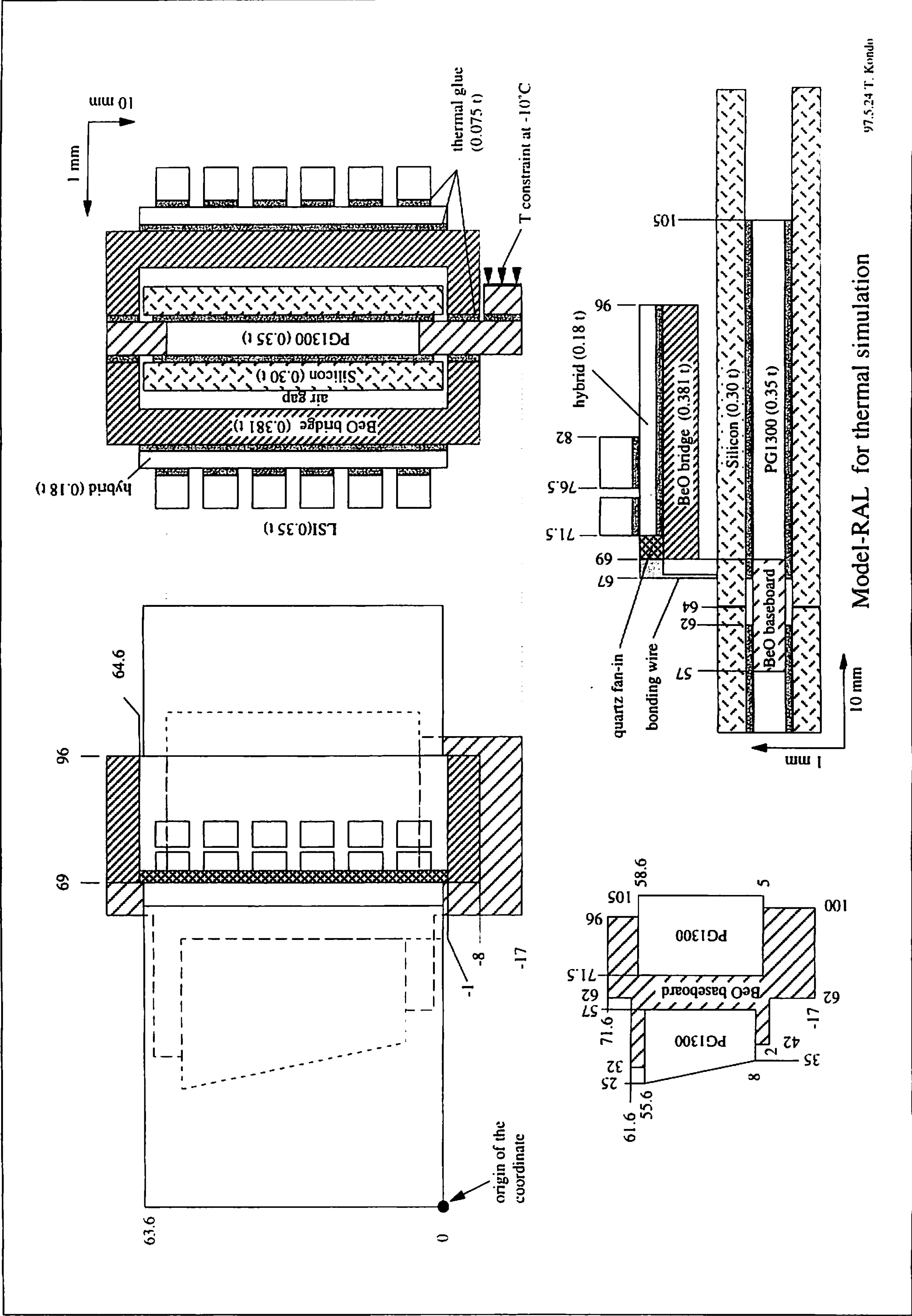

Figure 1 Model-RAL proposed by RAL in mid-March 1997.

el-RAL proposed by RAL in mid-March 1997. This design is a new attempt in order to reduce the effective material thickness of the ATLAS barrel SCT module.

Triggered by this attempt, variations of the design are proposed at KEK from models 1 to 8. Essential change is the shape and configuration of the baseboard on which both silicon microstrip detectors are attached. The baseboard provides not only the mechanical stiffness for support but also the thermal path from the detector to the cooling channel.

Figure 2 shows the configuration of the baseboard.

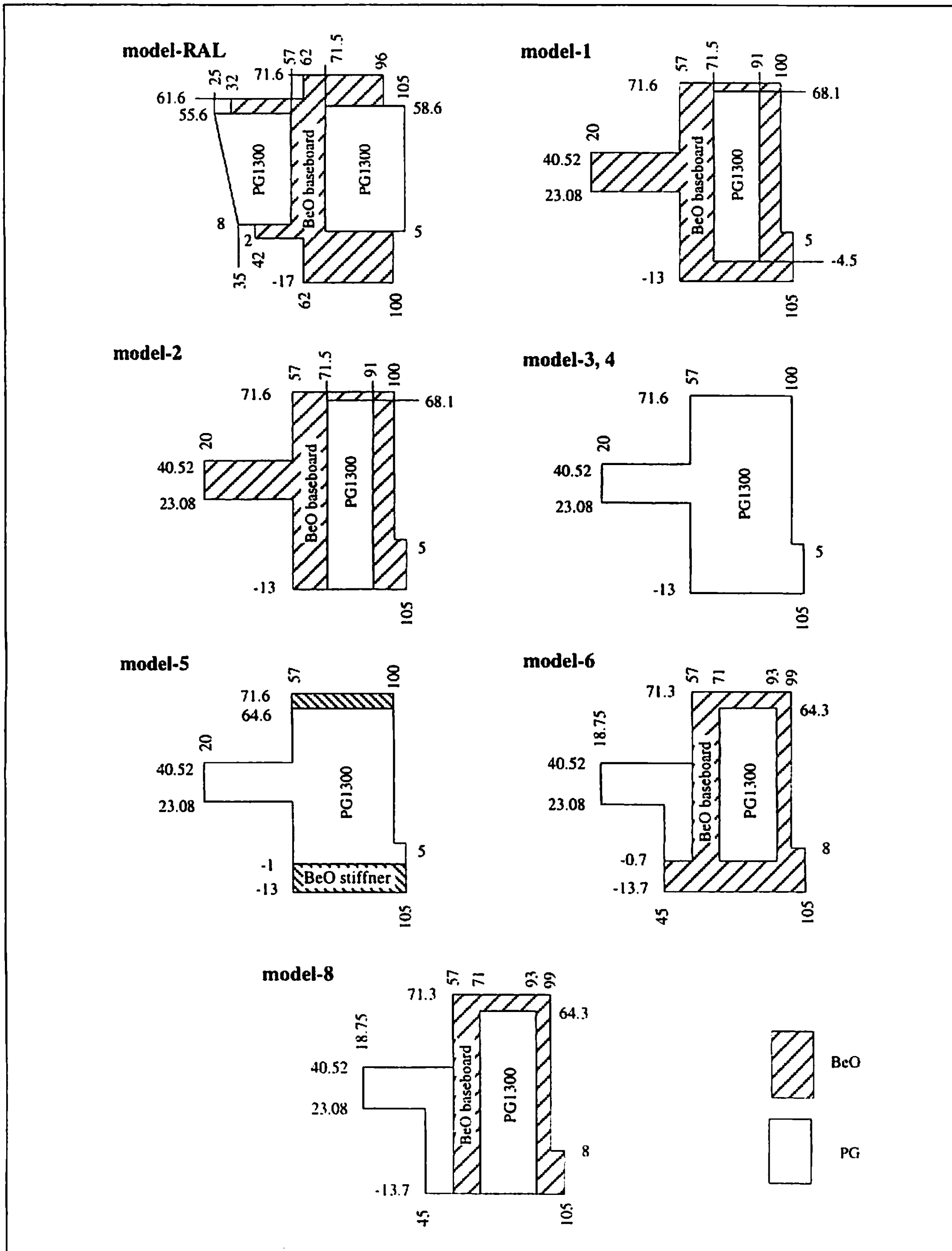

Figure 2 Design on the baseboard.

2. Thermal simulation

A finite-element thermal simulation is done using program ANSYS 5.1. A 3-D thermal and electrical solid elements is used. The thermal conductivity used in the program is listed in Table 2.

Table 2 Thermal conductivity of material used in the ANSYS simulation

material	conductivity (W/m·K)	material	conductivity (W/m·K)
silicon	130	BeO	280
PG1300	1300 (tangential) 3.5 (normal)	PG700	700 (tangential) 3.5 (normal)
thermal glue	0.5	Kapton hybrid	0.25
air	0.0245	BeO hybrid	280
quartz (fan-in)	0.15	bonding wire	150

For simplicity, the effects of surface convection and radiation emission are not included.

The cooling pipe is not included in the simulation. Instead, the temperature constraint is imposed at the contact of the cooling channel. The open triangle marks in the design figures show the location of this external constraint.

Heat generation in the electronics is simulated by usual bulk heat generation provided in ANSYS. The total heat generation in electronics is 3 or 4 Watts, corresponding to 1.5 or 2 W per side. 87% of the heat is assumed to be generated in the 1st chips (l x w x h = 7.2 x 4.0 x 0.35 mm^3) and the rest is generated in the 2nd chip (l x w x h = 7.2 x 5.5 x 0.35 mm^3).

The heat generation in the bulk of the radiation-damaged silicon detector is due to the bulk leakage current. The leakage current is known to have a strong temperature dependence:

$$I_{leak} \propto T^2 \cdot e^{-\frac{E_g}{2k_B T}}$$

where E_g is the effective gap energy of about 1.23 eV and k_B is the Boltzmann constant. In ANSYS program, the electrical resistance of material can be made temperature dependent. An electro-thermal element is assigned for the bulk part of the silicon detector and it is assumed to carry an electrical conductance with the same temperature dependence as that of the leakage current. With this trick, one manages to simulate the temperature dependence of heat generation by the leakage current [1].

The thermal simulation has been demonstrated to work very well when it is compared with the thermal experiments using heater as well as actual radiation damaged detectors [1,2].

3. Results of thermal simulation

3-1. Thermal runaway point

Thermal simulation is performed for various models by varying the heat generation in the detector bulk. Since the heat generation strongly depends on temperature, it is decided to use the heat generation per mm^2 (of 300 μm thick silicon detector) at 0°C as a standard parameter. Actual heat generation is calculated using the T-dependence give above.

Figure 3 shows the summary of the simulation result using PG1300 and with Q_{amp}=3 W. One can see clear model dependence. It is noted that, after 10 year operation at LHC, the bulk heat generation at 0°C is in the range of 40~80 μW/mm².

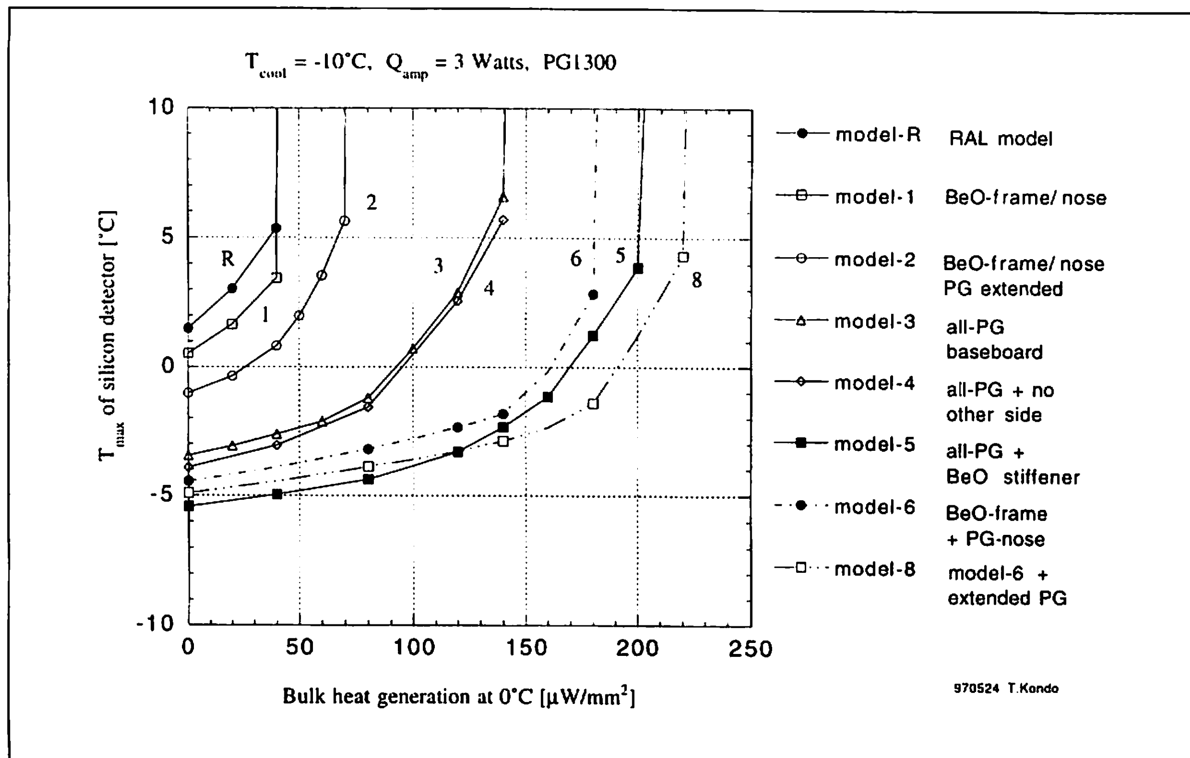

Figure 3 Dependence of the maximum temperate of the silicon on the bulk heat generation.

Number of conclusions can be extracted from Figure 3:

1. Both model-RAL and #1 encounter the thermal runaway below 50 μW/mm² and thus not satisfactory.
2. Extension of PG to the cooling edge (model 1 → 2, also 6 → 8) helps but the effect is not large.
3. Replacing all BeO baseboard by PG1300 (model 1 → 3) improves fairly well.
4. The thermal connection between the BeO bridge and baseboard at the other end does not contribute (model 3 → 4).
5. Additional BeO stiffener improves considerably (model 3 → 5).
6. Model 5, 6 and 8 satisfy the goal (> 40 ~ 80 μW/mm²) with enough safety margin.
7. In general, the maximum temperature at 0 μW/mm² (no bulk heat generation) is a good index of the thermal runaway (except one case of cross over between models 5 and 8).

3-2. Dependence on the thermal conductivity of PG

The thermal conductivity of PG is changed from 1300 to 700 in order to see how effective the PG contribution is in the thermal properties of the module. Figures 4 and 5 show its dependence for model-6 and 8. PG1300 shows better performance as expected, but the improvement is relatively larger in the case of model-8.

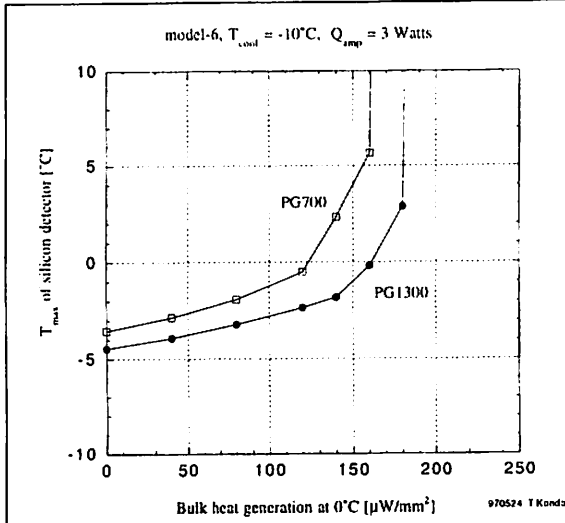

Figure 4 PG700 vs PG1300 (model-6, 3W).

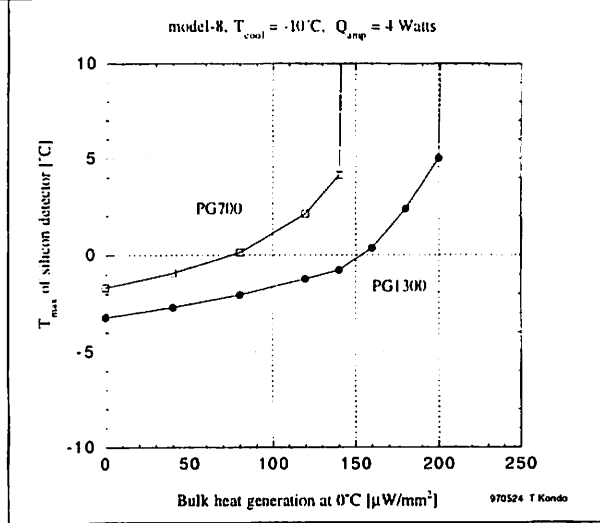

Figure 5 PG700 vs PG1300 (model-8, 4 W).

3-3. Dependence on Q_{amp}

The total power consumption in the electronics might be 4 W instead of 3 W. Figure 6 shows its dependence. It is noted that the runaway point does not change so much although the zero-point changes almost 2 degrees. This is probably due to the fact that runaway point is at the far edge of the silicon wafer, not near the location of electronics, and therefore the effect of power consumption in electronics is not direct but secondary.

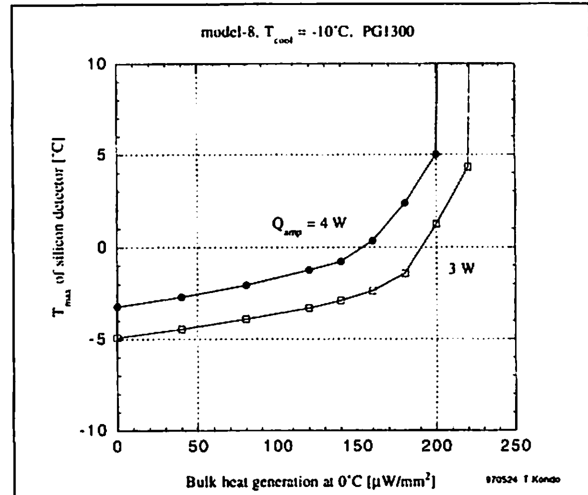

Figure 6 Comparision of 3 W vs 4 W in Q_{amp}.

3-4. Temperature of electronics chips

The temperature of the electronics chips strongly depends on the convection and/or radiation from the surface of the chips. In this simulation, these two effects are not included and therefore the present result may be far from reality. Anyhow, in such a (unrealistic) case, the chip temperature strongly depends on the thermal conductivity of the hybrid as shown in Figure 7.

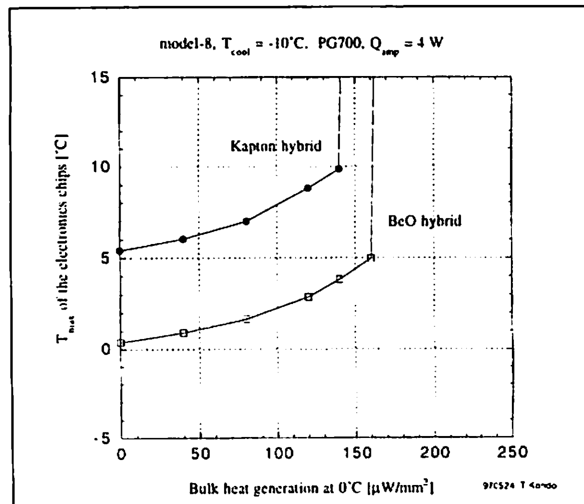

Figure 7 T_{chip}max for Kapton and BeO hybrids.

4. Tentative conclusion and points for further study

One can draw an interesting conclusions from these simulation results, though they are still tentative. In order to simplify the situation, let's take a view of thermal resistance as shown in Figure 8, in which three types of thermal resistances are introduced.

The biggest and most important thermal resistance seems to be R1. This is because quite an improvement in thermal behavior is observed in the changes of

- model-1 → model-2,
- model-3 → model-5,
- model-6 → model-8.

The apparent improvement from model-2 to model-3 is due to the reduction in both R1 and R2. But it is felt that the contribution of R1 is the main factor.

Among others, the improvement from model-3 → model-5 is dramatic. As shown in Figure 9, the configuration near the cooling point is quite different between model-3 and model-5. It seems that the BeO stiffener lowers the thermal resistance R1 substantially.

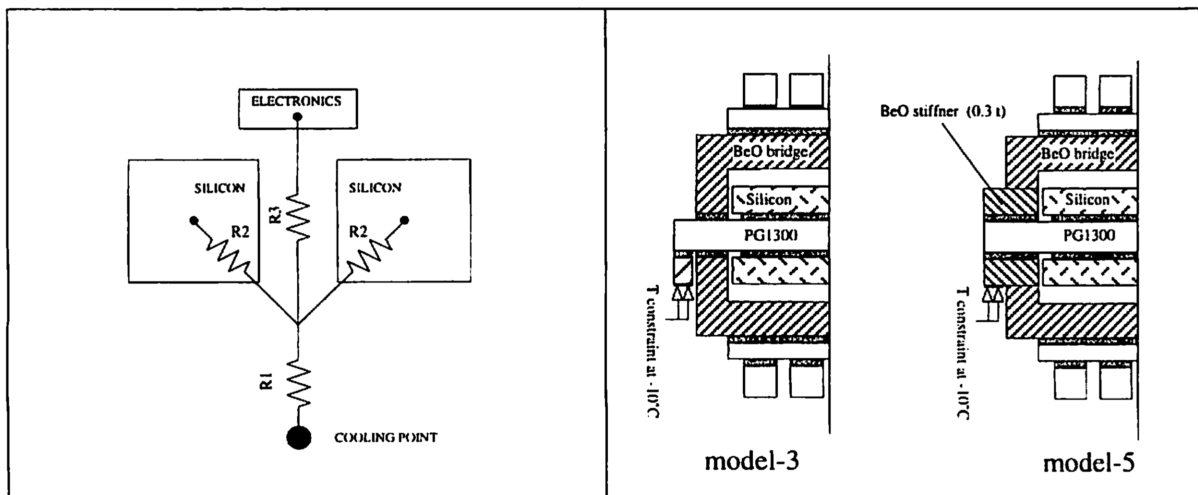

Figure 8 Thermal resistances in the SCT module

Figure 9 Details near the cooling channel.

In model-RAL and model-1, rather high starting values of T(Si) in Figure 3 are caused by the high thermal resistance R1. This is seen in Table 3 in which the minimum temperature of the silicon is listed. Model-RAL and -1 show relatively high T(Si)min, indicating high thermal resistance R1 between cooling point and silicon detector. Both models have the near-cooling configuration similar to that of model-3 (Figure 9) with worse conductivities due to BeO (relative to PG in model-3). The difference between model-RAL and -1 in T(Si)min is probably due to the difference in length along the cooling contact (see Figure 2).

Tentative conclusion is that the key point is how to lower the thermal resistance R1, where all the heat flux get concentrated. Compared with this major problem, it seems that the design of the baseboard under the silicon detector is rather insensitive to the overall thermal performance

Table 3 Min and max of the $T_{silicon}$ at no bulk heat generation

model	T_{Si}min.(°C)	T_{Si}max.(°C)
model-RAL	-1.63	1.50
model-1	-3.37	0.53
model-2	-4.79	-1.03
model-3	-6.36	-3.47
model-4	-6.35	-3.91
model-5	-8.18	-5.42
model-6	-7.65	-4.45
model-8	-8.17	-4.91

including safety from the runaway point.

This view is noticed after all the calculation was finished. New series of simulation is of necessity in order to verify the present (tentative) conclusion as well as to find better module design.

References

[1] T. Kohriki et al., Cooling Test and Thermal Simulation of Silicon Microstrip Detectors for High Luminosity Operation, ATLAS Internal Note INDENT-NO-094.

[2] T. Kohriki et al., First Observation of Thermal Runaway in the Radiation Damaged Silicon Detector, IEEE Trans. Nucl. Sci. 43 (1996) 1200-1202